

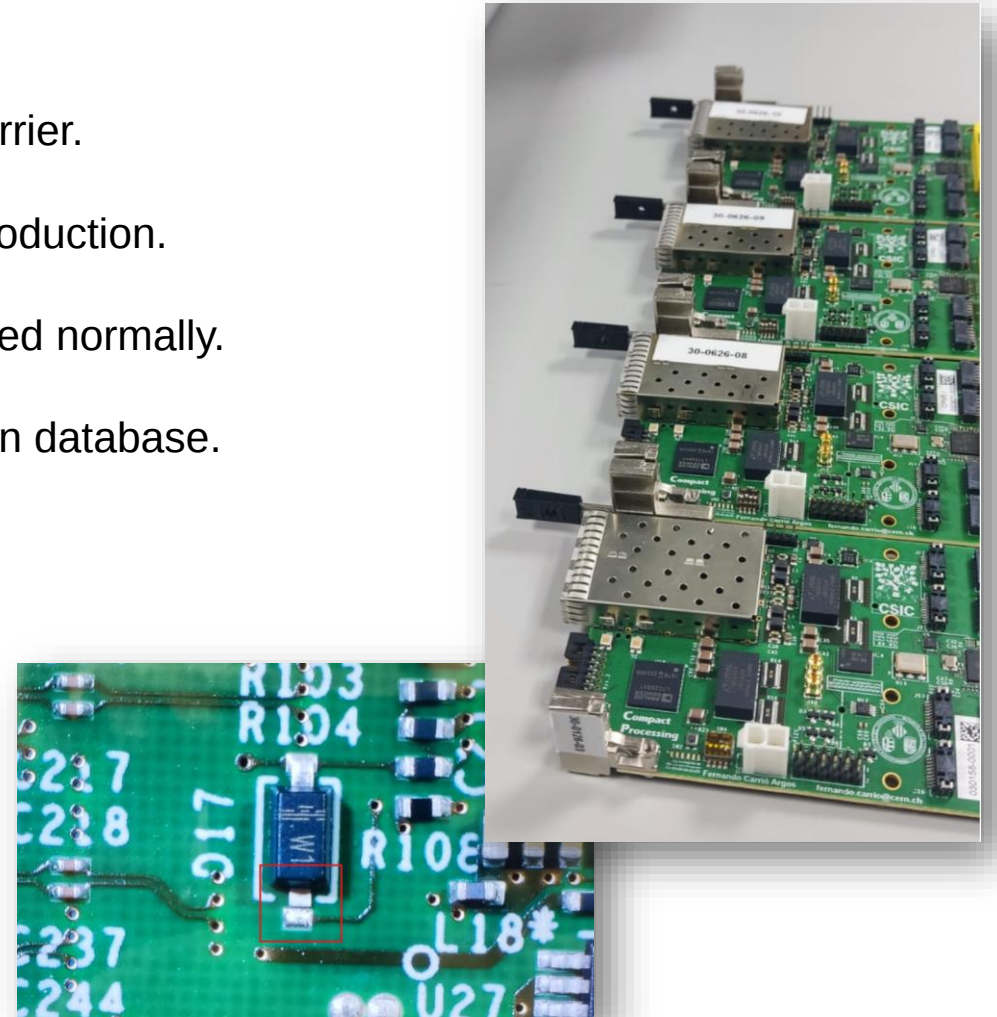
TileCal-IFIC Upgrade Project Meeting

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CPM validation

- I validated four CPMs before sending them to CERN.
- One CPM did not receive payload power when I inserted it into the carrier.
 - I found that diode *D17* had been **incorrectly soldered** during production.
 - ✓ • After resoldering it, the CPM received payload power and operated normally.
- I also registered the CPMs and their current locations in the production database.
- Finally, the four CPMs were prepared and sent to CERN for the **PRR**.
 - CPM-30-0626-08
 - CPM-30-0626-09
 - CPM-30-0626-10
 - CPM-30-0126-03



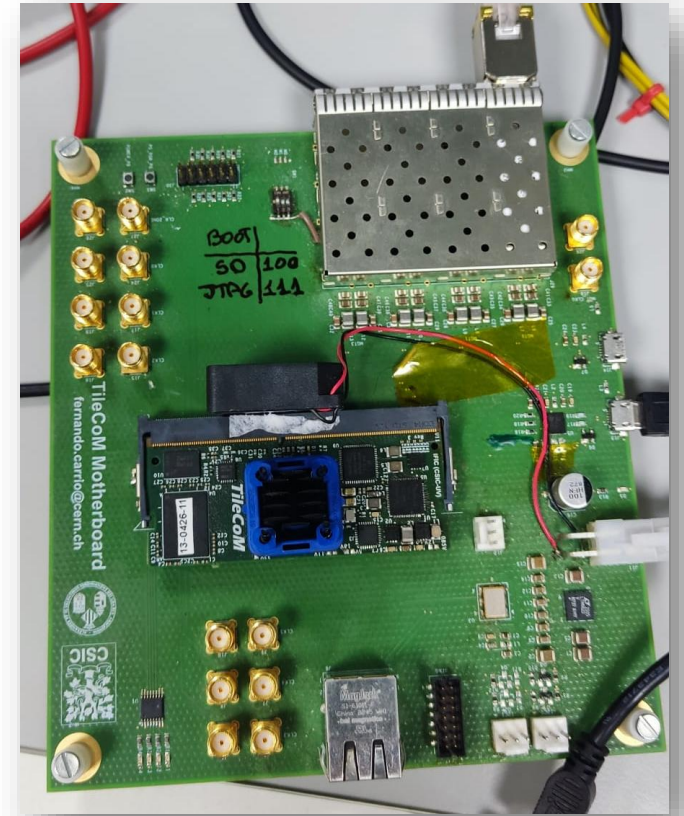
TDAQi power lost Debug

- I prepared patched version of the TDAQi MMC firmware to prevent Carrier power lost.
 - The objective was to correct a possible problem in the *ipmb_send()* function.
 - This function could modify the transmission buffer while a previous transmission was still active.
- During the first long test, the CPM changed from M4 to M7 after 20 hours.
 - The payload remained active. 
 - The IBERT test continued running without errors. 
 - We lost management communication with the CPM. 
- For the next test, I applied the same type of communication patch to the CPM.
 - The objective was to apply correcting IPMB communication in the CPM and the TDAQi would prevent the communication loss.
 - However, the result was worse than in the previous test. 
 - The UART showed IPMB-L errors from both the CPM and the TDAQi.
- A more serious failure occurred during this test.
 - The carrier then restarted because of a **watchdog** timeout.
 - The CPM, the Carrier and the TDAQi changed to M0.
 - This time, we lost the payload and the IBERT test stopped.
- For future work: we focus on the shared IPMB-L bus and the carrier recovery mechanism.

```
[titalca@tical46 fix_comm_lost]$ sudo !!  
sudo cat /dev/ttyUSB0 | tee uart.log  
<E> iface_ipmb_send_message_ipmb: i2c NACK  
<L>: IPMB-L error: IPMC EA: timeout  
<L>: IPMB-L error: IPMC EA: timeout  
<L>: IPMB-L error: IPMC 78: timeout  
<L>: IPMB-L error: IPMC EA: timeout  
<L>: IPMB-L error: IPMC EA: timeout  
<L>: IPMB-L error: IPMC EA: timeout  
<L>: IPMB-L error: IPMC EA: timeout  
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<L>: IPMB-L error: IPMC EA: timeout  
  
BMR-A2F Boot Loader v1.3.0 (c) Pentair Technical Products, Inc.  
boot_first_time: 00  
boot_type: 12  
wdt_reset_type: 23  
fw_version: 02  
wdt_reset_occurred implemented: false  
bl_hdr:00000000  
fw_version: 02  
boot_flag: 5F  
Active partition is #01  
active status:07  
wdt_reset_occurred:01  
reset_type:23  
Firmware address:00006000  
Firmware size: 00027380  
Firmware image (END-START = 00040000) - checksum: 00  
Active partition successfully checked: 07  
boot_flag: 5A  
active status:02  
Booting at address #00006000  
  
<->: BMR-A2F Firmware (v1.3.0), AMC carrier edition.  
<->: Pentair Technical Products, Inc. (c) Copyright 2004-2016.  
<->: Reset type: cold, reset cause: watchdog  
<->: Perform Power-on-Self Testing.  
<->: Device type: A2F200M3F-CS288  
<->: MSS clock frequency: 80 MHz  
<->: Fabric clock frequency: 20 MHz
```

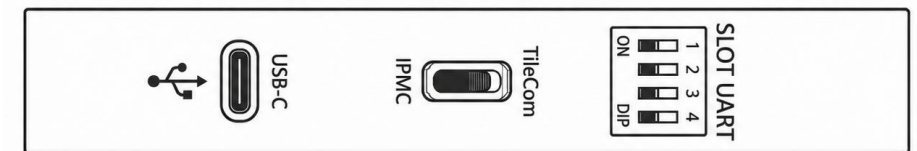
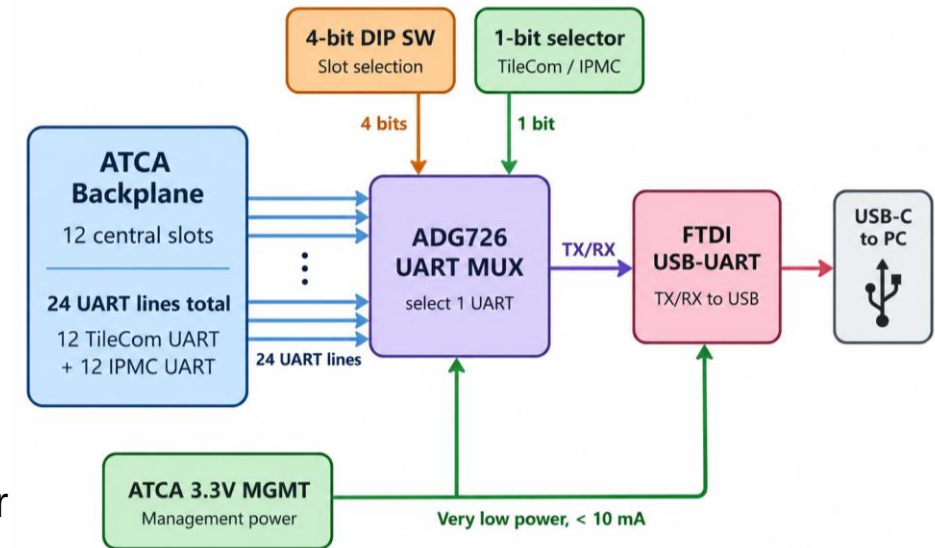
TILECOM Clermont Debug

- Clermont sent us TileCom (TCO-13-0426-09) because it sometimes failed to boot correctly.
 - The problem appeared after configuring the clocks.
 - They had to restart the TileCom several times before it booted correctly.
 - Following our recommendation, they separated the decoupling capacitors from the TPS thermal pad -> but the problem continued.
- I tested the TileCom with two different configurations.
 - Our usual SD card image.
 - The SD card image provided by Clermont.
- I also tested different power and connection conditions.
 - A laboratory power supply between 11 and 13 volts.
 - The TileCom connected to a carrier on the laboratory bench.
- The TileCom booted correctly in all our tests.
 - We could not reproduce the problem observed in Clermont.
 - I am currently analysing the Ilana motherboard schematics and comparing the connections to find a solution.



ATCA UART debug board

- I would like to design a board to access the UARTs of the 12 slots from the front of the ATCA shelf.
 - Each slot has one TileCom UART and one IPMC UART.
 - This means that the board will provide access to 24 UARTs in total.
- The UART selection will be completely manual.
 - A 4-bit DIP switch for select the slot.
 - A two-position switch for select either TileCom or IPMC.
- A multiplexer system, will connect the data signals to an FTDI USB converter with a USB-C connector.
- The board will use the management 3.3 V.
 - The board will not negotiate or enable payload power.
 - The initial target is to keep the current consumption below 10 mA.
- The next step is to validate architecture and discuss the design.



Sensor readout through IPMB-L

- At present, TileCom reads the carrier sensors through the I²C bus shared with the IPMC.
 - TileCom publishes these sensor values to the OPC server.
 - During the PRR, the reviewers warned that having two masters on the same bus could cause collisions and recommended avoiding this configuration.
- The proposed solution is to connect TileCom to IPMB-L.
 - TileCom would request the sensor values from the IPMC using IPMI commands.
 - This would be cleaner than reading the IPMC UART and parsing its text output.
- Only a few changes would be required on the carrier.
 - Connect the two IPMB-L lines and add an I²C buffer.
 - Implement the `ipmb_send()` routine in TileCom.
- TileCom would appear on IPMB-L as a device or FRU, without implementing power management with the Shelf Manager.
 - An FPGA enable pin would tell the IPMC that TileCom is present.
- We would like to discuss this proposal with Fernando and Albert to confirm that he considers it viable and agrees with this solution.

