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Computing challenges for present and future experiments: pushing FPGA timing

FPGAs have long been used in HEP experiments, but over the last decade their role has shifted from digital logic delivery platforms to high-performance computing engines, offering unparalleled computational throughput and flexibility. Yet harnessing this power requires operating at higher frequencies, making timing closure a critical challenge. While current implementation tools perform remarkably well for small-to-medium designs, placement becomes the critical bottleneck at the million-flip-flop scale, leaving a significant fraction of the computing potential of next-generation FPGAs untapped. In this talk, we present a set of placement-driven tools we have developed to address this bottleneck, enabling the CMS Muon Barrel Trigger algorithm to be implemented on the largest UltraScale+ devices at 480 MHz. The tools will be made available to the community, providing a practical approach to pushing the performance limits of large FPGA designs.

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