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High Low: High-Performance Algorithms for Low Power Sustainable Hardware

Measurements of processing power, power consumption and efficiency are an imperative for the the high luminosity LHC collider and future colliders.

Several studies have been conducted to understand how to optimize the

energy usage in terms of the computing architectures and the efficiency of the running algorithms.

Several architectures (CPUs, GPUs, and FPGAs) are evaluated to assess their performance, energy efficiency, cost, and potential for sustainable high-performance computing.

They include in particular signal processing, tracking reconstruction algorithms running in real time at 30 MHz, and physics event generators.

Recent results have been published in Front. Phys. 14:1868616 (2026) [arXiv:2604.27523] and Computer Physics Communications, 329 (2026), 110394 [arxiv:2605.23785].

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