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FORGE: Framework for Orchestrated RTL Generation and Evaluation

Integrating FPGA modules requires consistent structural connections, interface descriptions, and verification files. These descriptions can diverge when modules or synthesis-generated ports change. We present FORGE (Framework for Orchestrated RTL Generation and Evaluation), a Python framework that resolves module interface contracts and a declarative topology into a shared intermediate representation. Contracts map physical ports to common or consumer-defined roles and are checked against available port metadata. The resolved model supports structural generation, SystemVerilog testbench scaffolding, static latency and throughput analysis, and reporting. Consumers supply module implementations, datasets, golden models, and scoreboards. The workflow includes HLS orchestration, HLS C simulation, single-module RTL simulation, and integrated-payload RTL simulation. Three reference consumers illustrate a trigger pipeline, a multi-clock image-processing pipeline, and a minimal passthrough design. The largest contains 12 module instances and 119 connections. The archived record includes 17 successful simulation flows, one expected diagnostic failure, a separate structural rejection test, and software-test results. It also demonstrates limits of the current implementation, including reused per-flow metadata and single-clock runtime probe sampling. Static latency results concern declared metadata, and the reported design validation is simulation-level. FORGE provides a common description for integration and verification infrastructure while leaving algorithm-specific correctness checks to the consumer.

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