



Summary of activities

(mainly Compact Processing Module...)



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Instituto de Física Corpuscular (CSIC-UV)

March 21th 2026

Valencia Tile meeting

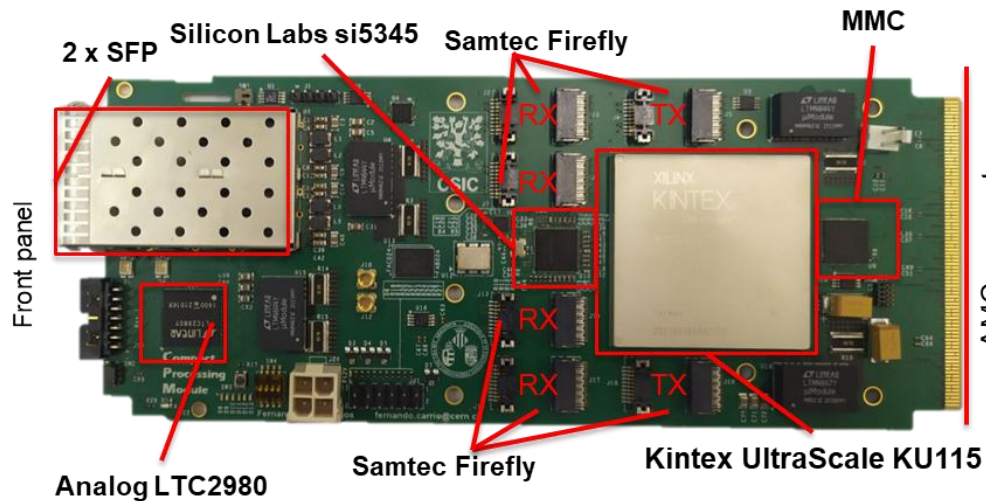


Compact Processing Module - Production



- **Single AMC board** with full-size factor
 - **32 RX channels** via 4 Samtec Firefly
 - **16 TX channels** via 2 Samtec Firefly
 - **Up to 14 channels** via AMC connector
 - **Kintex UltraScale: XCKU115-2FLVA1517E**
- Procurement status @ Valencia
 - All active components and mechanics for 128 CPMs are on hand (except for a few for v2.3)
 - Received 60% FPGAs for production + 40% procured by South Africa
 - **80% of Firefly modules received**

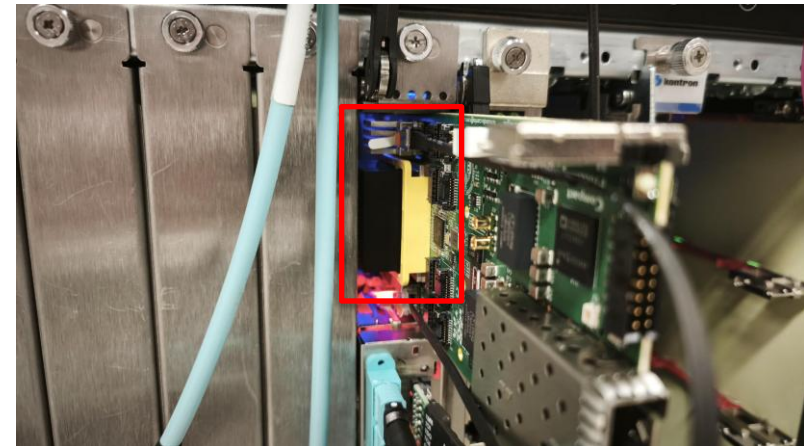
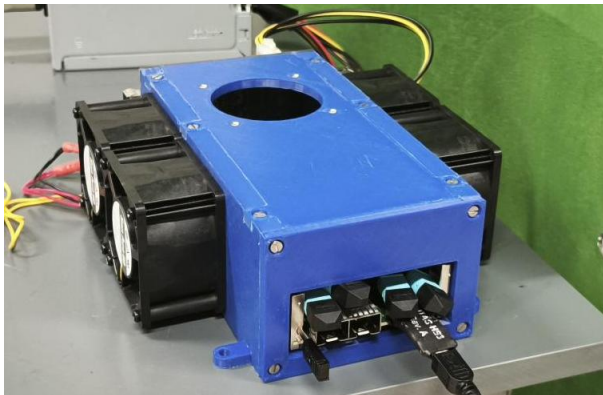
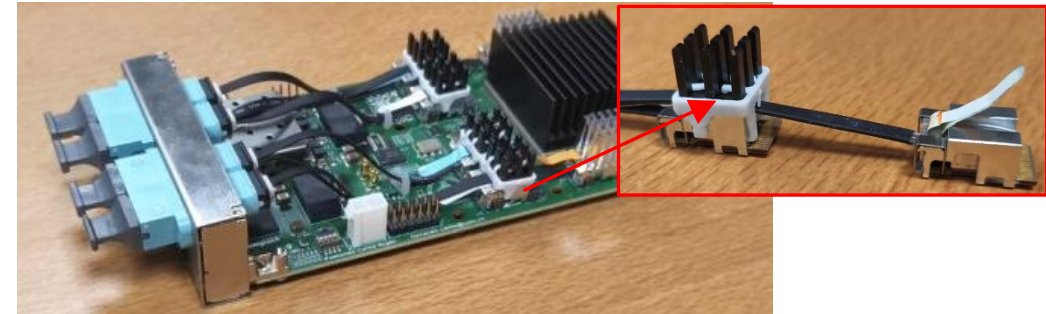
- 2 x Preproduction (v2.3) CPM boards partially tested
 - Few components had to be reworked
 - Produced 20 PCBs with Panasonic Megtron 6 Halogen Free
 - Additional batch of 9 CPMs **launched** in April after initial validation
 - Rompal didn't reply, so started iterating with them during the past weeks
 - Factory is stopped for at least 1 month due software migration and inventory
 - Announced that if boards cannot be assembled on 15th June as latest, production is moved to another company (as for Carrier and TileCoM)
 - Asked for quotation to ProDesign to assemble them ASAP



- Results from the boards:
 - Main components already tested within the "CPM box"
 - FPGA, Firefly modules (access via I2C), Flash memory, backplane
 - Atmega in one board damaged because incorrect fw - some inputs were set as output by mistake (no FPGA damage!)
 - Completing the full test coverage for all the components
 - EEPROMs, IO pins, etc
 - Required some fw and hw development for "validation tests"
 - Tropper libraries extended with lots of new functionalities
 - Vivado firmware project with several IPbus, IBERT, etc.
 - Tests to be replicated in Valencia for the other 2 CPMs + the upcoming 9
 - To be integrated in the VST to tests with 2 full modules.

Compact Processing Module - Mechanics

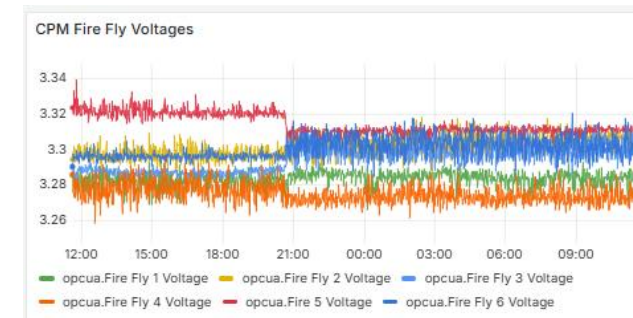
- Front panel design with minor modifications ✓
- COTS heatsinks for Firefly TXs(640/640) and FPGA (70/160)
 - One heatsink covering the 4 Firefly RXs (Demonstrator)
 - Still some risk of applying stress on the PCB + maintenance remains complex
 - Custom plastic clip for independent heatsinks (Bld 175)
 - No mechanical stress, easy maintenance
 - Under tested in 175, preliminary similar results than with the big heatsink
- New heatsinks + plastic clip for the FPGA
 - Larger fins possible to fit in the carrier
 - Thermal tests in SR1 to be redone with new configuration
- New box for preliminary tests + backplane board



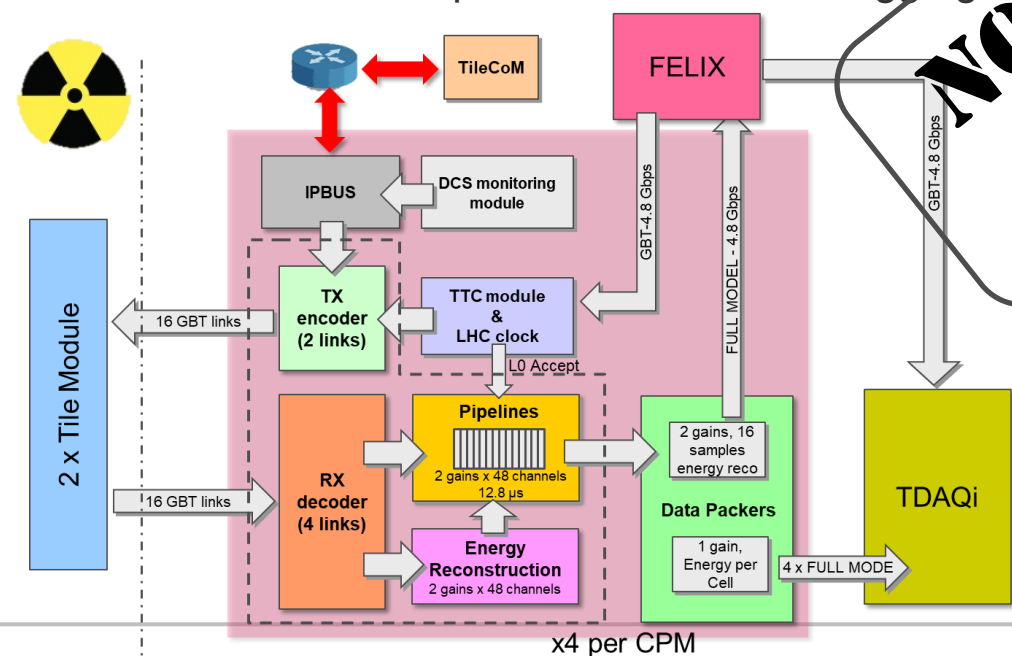
FW: Compact Processing Module



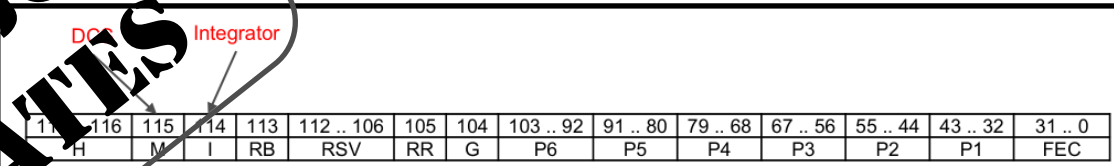
- Most functionalities in place and validated during test beams, VST and Demonstrator
 - 2 link @ 4.8 Gbps to FELIX: TTC and Readout + 1 GbE for IPbus communication
 - LTI - FULL MODE (9.6 Gbps) implemented -> **tested with BNL-155!**
 - 28 x links to DaughterBoards (4.8/9.6Gbps): **GBT with FEC and new data format**
 - 4 x links @ 9.6 Gbps to TDAQi: **FULL mode**
 - Remote programming via IPbus for both CPM and DaughterBoards
 - Block to detect corruption in the data samples to be added (stop bits, spikes, etc)
 - Firmware updates for the DCS readings → Brenton as part of his Master thesis
 - Deployment in P1 by Brenton: Ipbus → IS → pBeast
 - Several firmware updates to extend debugging capabilities



DCS readings via IPbus



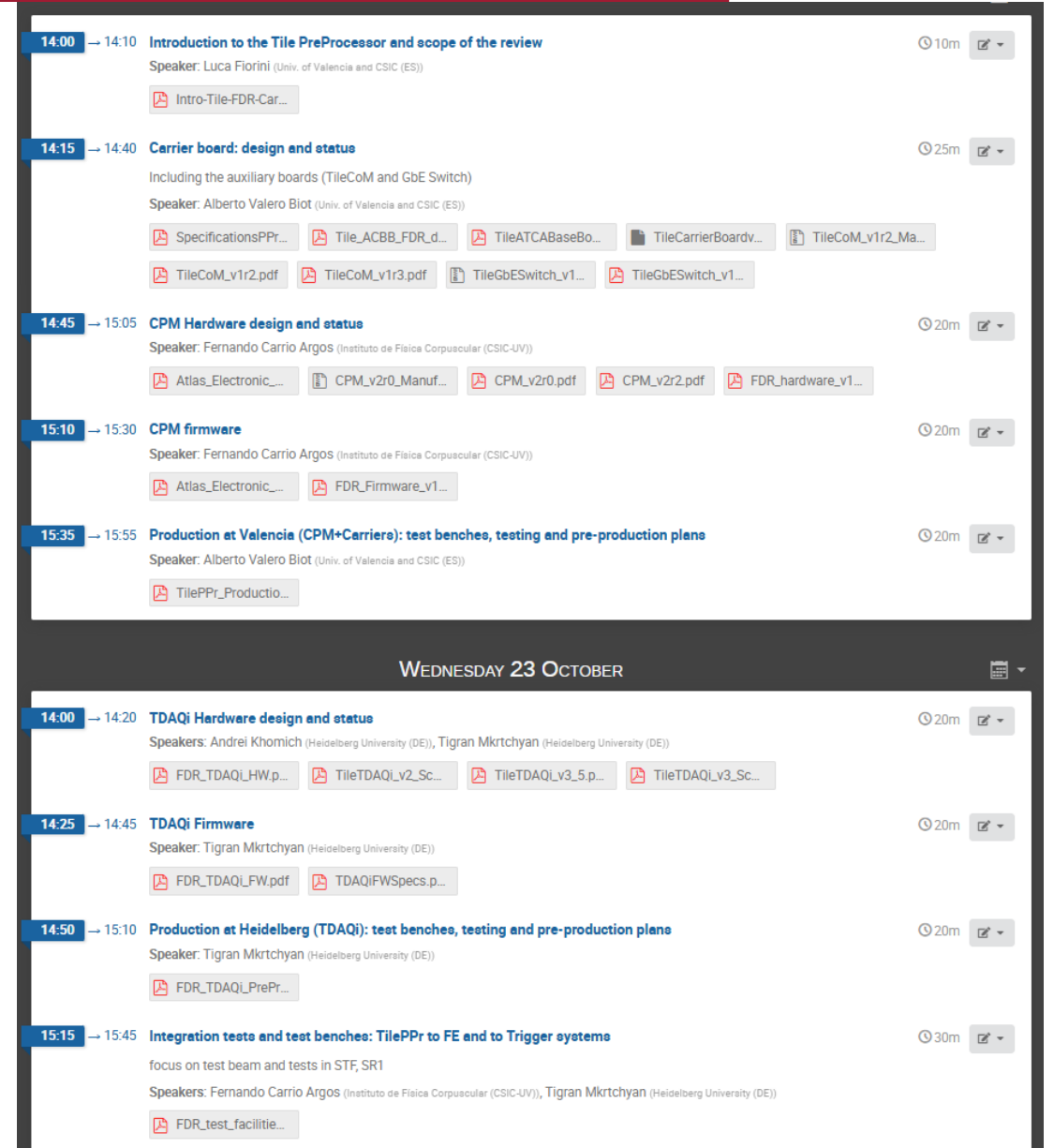
NO MAJOR UPDATES



- Where:
- H: GBT header.
 - M: DCS & monitoring data.
 - I: Integrator data.
 - RB: Read back commands.
 - RSV: Reserved bits.
 - RR: Reset Request from the Daughterboard.
 - G: FEB gain. 0 is low gain and 1 high gain.
 - Px: PMT samples.
 - FEC: Forward Error Correction.

BW assigned	Assigned bits	Description/ max requirement
80 Mbps	4	GBT header → Used as returned BCR
80 Mbps	1	DCS monitoring data. It includes a maximum of 100 sensors * 10 Hz * 32-bit words for monitoring of temperature sensors, voltages and currents.
80 Mbps	1	Integrator data. It includes a maximum of 6 PMTs * 200 Hz * 32-bit words
80 Mbps	1	Read back of MB and DB registers
80 Mbps	1	Reset Request from the DB
80 Mbps	1	High and Low gain identifier
5.760 Gbps	72	PMT readout data
2.56 Gbps	32	Forward Error Correction

- Preparing tentative agenda with Giulio
- Review splitted in two days:
 - 29th (PPr) and 30th (TDAQi) of June
- Similar topics as in the FDR but focus on
 - Latest changes in the designs + software and firmware capabilities/status
 - No need to present the full design again
 - No deep review of the firmware (probably will come as a separate review)
 - Compact Processing Module, Carrier + mezzanine boards → Fernando/David/Alberto
 - Results from preproduction boards and highlights
 - Fernando/David/Alberto
 - Installations validation procedures, database, and production schedules
 - Alberto/Luca/Arantxa
 - Integration test results with DB, TDAQi, FELIX
 - Fernando/Thomas



The screenshot displays a meeting agenda for Wednesday, 23 October. The sessions are as follows:

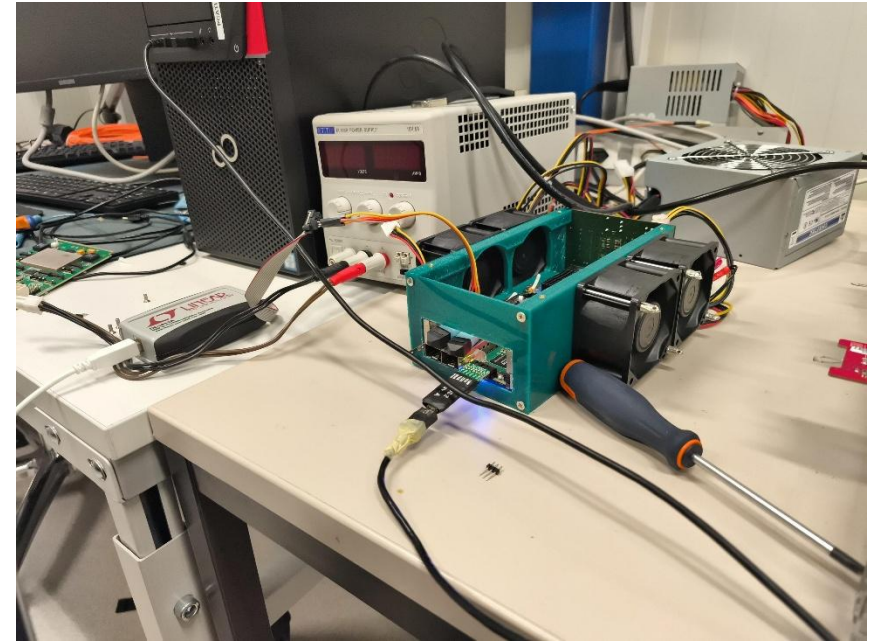
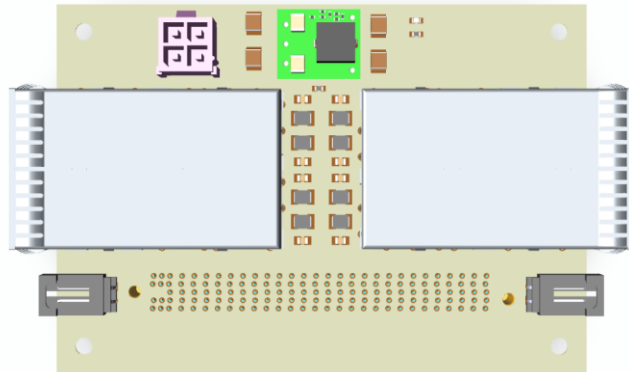
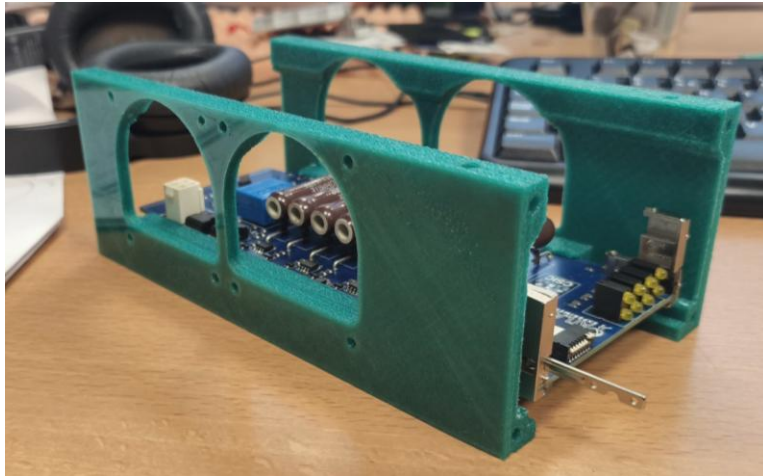
- 14:00 → 14:10 Introduction to the Tile PreProcessor and scope of the review**
Speaker: Luca Fiorini (Univ. of Valencia and CSIC (ES))
Intro-Tile-FDR-Car...
- 14:15 → 14:40 Carrier board: design and status**
Including the auxiliary boards (TileCoM and GbE Switch)
Speaker: Alberto Valero Biot (Univ. of Valencia and CSIC (ES))
SpecificationsPPr..., Tile_ACBB_FDR_d..., TileATCABaseBo..., TileCarrierBoardv..., TileCoM_v1r2_Ma..., TileCoM_v1r2.pdf, TileCoM_v1r3.pdf, TileGbESwitch_v1..., TileGbESwitch_v1...
- 14:45 → 15:05 CPM Hardware design and status**
Speaker: Fernando Carrio Argos (Instituto de Fisica Corpuscular (CSIC-UV))
Atlas_Electronic..., CPM_v2r0_Manuf..., CPM_v2r0.pdf, CPM_v2r2.pdf, FDR_hardware_v1...
- 15:10 → 15:30 CPM firmware**
Speaker: Fernando Carrio Argos (Instituto de Fisica Corpuscular (CSIC-UV))
Atlas_Electronic..., FDR_Firmware_v1...
- 15:35 → 15:55 Production at Valencia (CPM+Carriers): test benches, testing and pre-production plans**
Speaker: Alberto Valero Biot (Univ. of Valencia and CSIC (ES))
TilePPr_Productio...

WEDNESDAY 23 OCTOBER

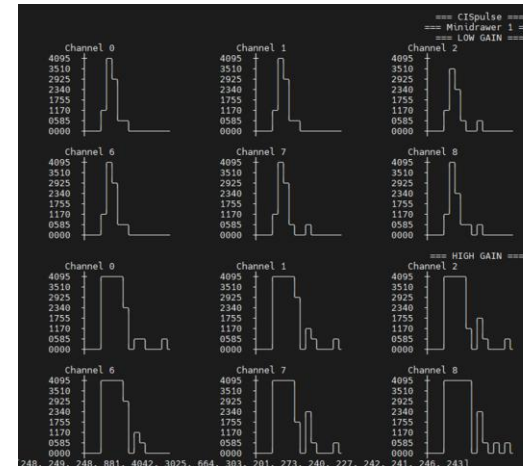
- 14:00 → 14:20 TDAQi Hardware design and status**
Speakers: Andrei Khomich (Heidelberg University (DE)), Tigran Mkrtchyan (Heidelberg University (DE))
FDR_TDAQiLHW.p..., TileTDAQiL_v2_Sc..., TileTDAQiL_v3_5.p..., TileTDAQiL_v3_Sc...
- 14:25 → 14:45 TDAQi Firmware**
Speaker: Tigran Mkrtchyan (Heidelberg University (DE))
FDR_TDAQiLFW.pdf, TDAQiFWSpecs.p...
- 14:50 → 15:10 Production at Heidelberg (TDAQi): test benches, testing and pre-production plans**
Speaker: Tigran Mkrtchyan (Heidelberg University (DE))
FDR_TDAQiLPrePr...
- 15:15 → 15:45 Integration tests and test benches: TilePPr to FE and to Trigger systems**
focus on test beam and tests in STF, SR1
Speakers: Fernando Carrio Argos (Instituto de Fisica Corpuscular (CSIC-UV)), Tigran Mkrtchyan (Heidelberg University (DE))
FDR_test_facilitie...

BACKUP

- 3D support for on-table test benches + Ethernet backplane -> Fully working
 - Support with built-in guidelines
 - Four 60 mm x 60 mm fans screwed into the support
 - Backplane with 4 SFP and providing power to CPM and fans



- Software ecosystem continuously evolving and growing up: Demonstrator, Prometeo, Vertical Slice Tests
- Online libraries for the CPM: TROOPER libraries
<https://gitlab.cern.ch/fcarrio/trooper-libraries/-/tree/master>
 - C++ libraries for TDAQ, also compiled as .so python libraries. Cmake, Make
- PrometeoPy application using them:
<https://gitlab.cern.ch/fcarrio/prometeopy>



PrometeoASCII with Trooper libraries



Grafana@ testbeam using pBeast + IS

- Preliminary software for DCS monitoring for the Demonstrator (Filipe, Brenton, Mpho)
 - Publishing into ATLAS IS -> pBEAST -> Grafana
 - OPC UA developments in parallel for Phase -II
- Control Prometeo Web panel
 - Control and monitoring of links
 - Fw loading and initialization

PROMETEO Control Panel

API connection OK

Configuration

Auto-refresh: 2 s | Address: prometeo | Updated: 10/03/2026, 08:15:33

DaughterBoard

Side A: Fw version "0x9fca2025" | Jump FW | reset FW | Config

Side B: Fw version "0x9fca2025" | Jump FW | reset FW | Config

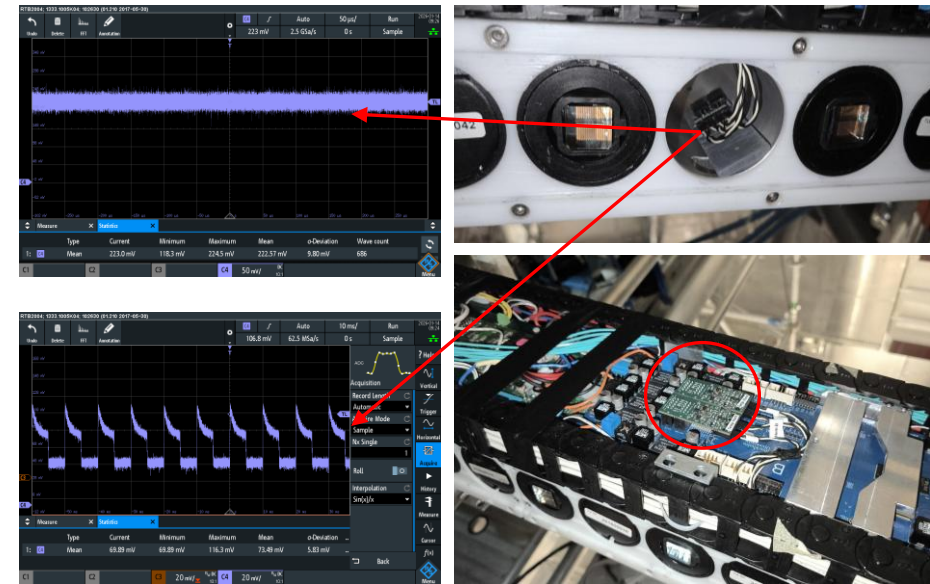
Compact Processing Module

resetRX | resetCounters

MD	Link	MGT TX RDY	MGT RX RDY	GBT HEADER	GBT RX RDY	Errors	BER	Effective	Frames	RTT
1	A0	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	A1	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	B0	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	B1	1	1	1	1	0	6.86e-15	0	3641491715490	49

Control Prometeo Web panel

- Environmental sensors installed in the Demonstrator as a candidate system for Phase-II
 - System controlled from Daughterboard GPIO pins and readout using XADC
 - Analog signal conditioning for temperature (PT100) and humidity (polymer) using INA333
 - Sealicon FGDOS for TID + Dickson bridge to charge it (20V)
 - Two sensors: 0-10 Gy and 0-50 Gy with 8-bit resolution
 - 2 sensor boards equipped in MD4, where probes has been installed in PMT hole 44
- Control of I2C and SPI lines from remote CPM via IPbus
 - Propagation signals via GBT protocol over fiber at 4.8 Gbps
 - 2 × SPI interfaces and 2 × I2C interfaces
 - LED trigger with LEMO
 - Fully working now

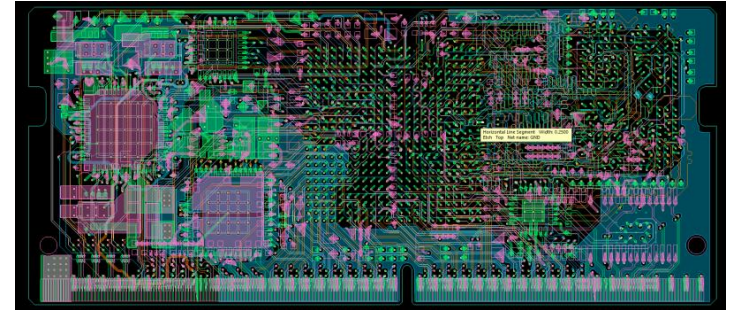


TileSensor board v1.0

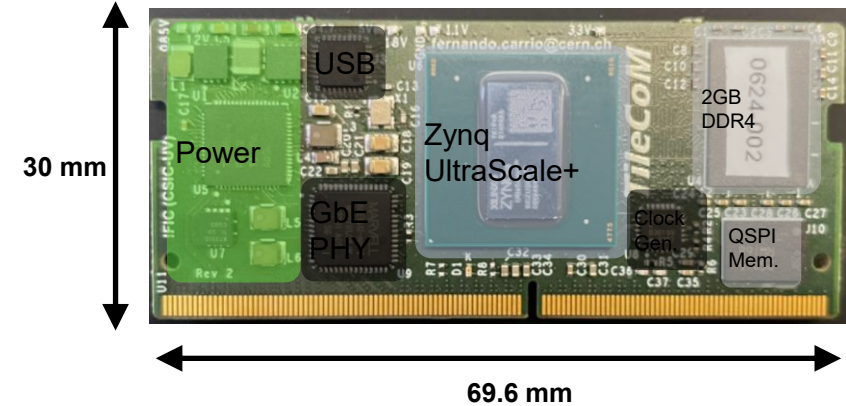


Tile GBTx board

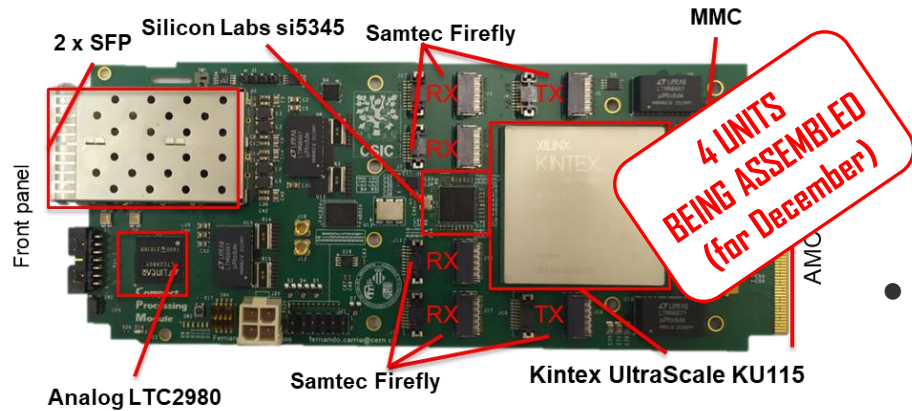
- Custom SoM based on AMD Zynq UltraScale+ ZU2CG device
 - OPC servers for Detector Control System sensors reading
 - Remote front-end FPGA programming
 - CPM and TDAQi JTAG programming and debugging using Virtual Xilinx Cable
 - Acting similar to a SBC, configuration of CPM and front-end electronics
- 4 units of the Preproduction version (v1.3) being/or assembled
 - Expected for this week
- 53 PCBs were produced last December (MOQ).
 - A few will be shipped to SA to test/complete the preproduction in PCB Trax



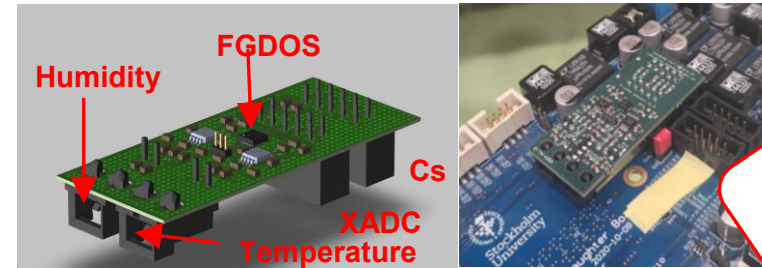
TileCoM v1.3



- Revision 2.3 of the CPM
 - Single AMC board with full-size form factor
 - 6 x Samtec Firefly
 - XCKU115-2FLVA1517E



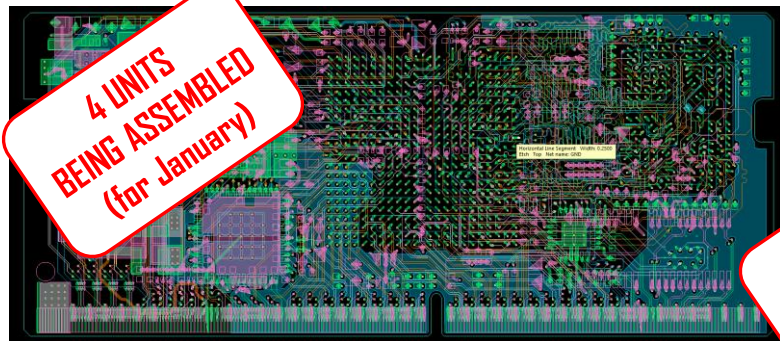
- Sensing environment conditions inside the TileCal modules
 - Analog signal conditioning for temperature (PT100) and humidity (polymer) using INA333 + Total Ionizing Dose (TID) sensor



TileSensor board v1.0

4 UNITS TESTED AND WORKING -to be installed in PI in January-

- Rev 1.3 of the TileCoM
 - SODIMM-240pin: 6.7 cm x 3 cm
 - 10 layers, 1 mm thickness, with 251 components



TileCoM v1.3

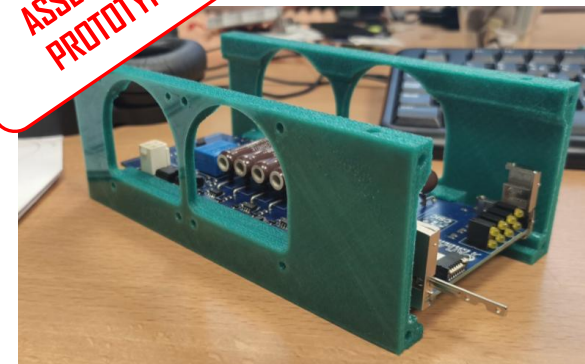
- Optical GBT-GPIO expander
 - Remote control of the HV and LED drivers from CPM



TileGBTx board v2.0

ASSEMBLING PROTOTYPE!

- Plastic support for on-table test benches + Ethernet backplane
 - Support with built-in guidelines
 - Four 60 mm x 60 mm fans
 - Backplane with 4 SFP and power distribution



UNDER DESIGN (Q1 2026)

