



Summary of activities

(mainly Compact Processing Module...)



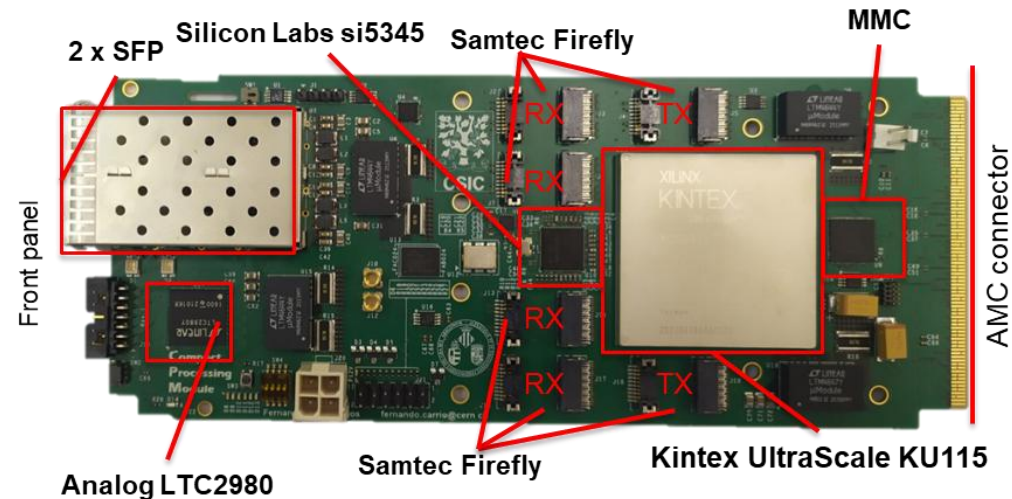
Fernando Carrió Argos
Instituto de Física Corpuscular (CSIC-UV)

March 10^h 2025

Valencia Tile meeting

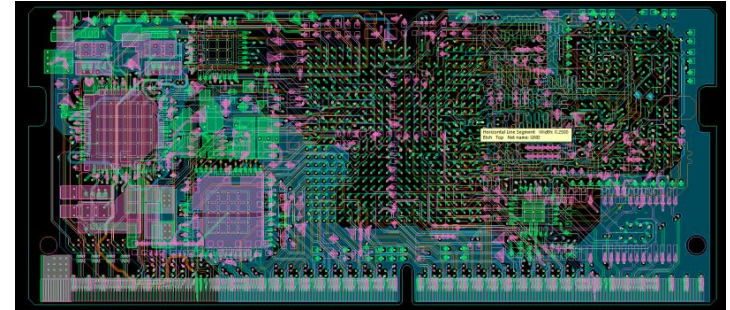


- **Single AMC board with full-size factor**
 - 32 RX channels via 4 Samtec Firefly
 - 16 TX channels via 2 Samtec Firefly
 - Up to 14 channels via AMC connector
 - **Kintex UltraScale: XCKU115-2FLVA1517E**
- Procurement status @ Valencia
 - All active components and mechanics for 128 CPMs are on hand (except for a few for v2.3)
 - Received 60% FPGAs for production + 40% procured by South Africa
 - **80% of Firefly modules received**

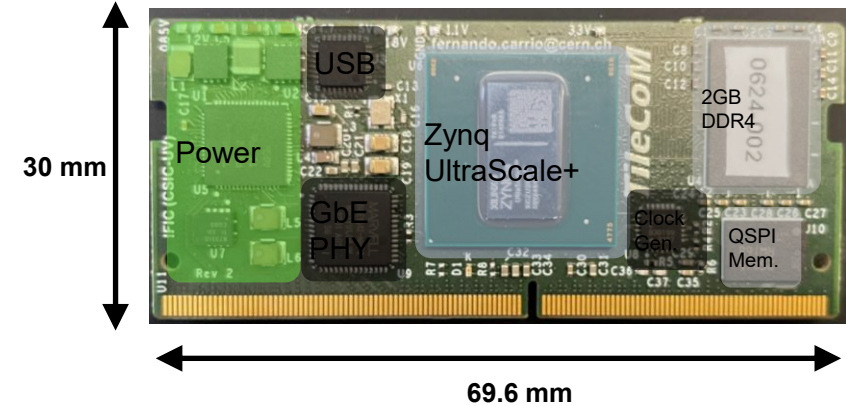


- Received 4 preproduction (v2.3) CPM boards → currently under test
 - Few components not correctly assembled: LEDs and one button
 - Additional batch of 9 CPMs **launched** → complete preproduction + Prometeo
 - Produced 20 PCBs with Panasonic Megtron 6 Halogen Free

- Custom SoM based on AMD Zynq UltraScale+ ZU2CG device
 - OPC servers for Detector Control System sensors reading
 - Remote front-end FPGA programming
 - CPM and TDAQi JTAG programming and debugging using Virtual Xilinx Cable
 - Acting similar to a SBC, configuration of CPM and front-end electronics
- 4 units of the Preproduction version (v1.3) being/or assembled
 - **Expected for this week**
- 53 PCBs were produced last December (MOQ).
 - A few will be shipped to SA to test/complete the preproduction in PCB Trax



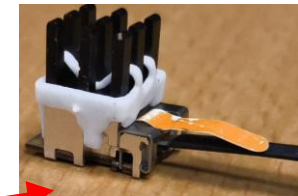
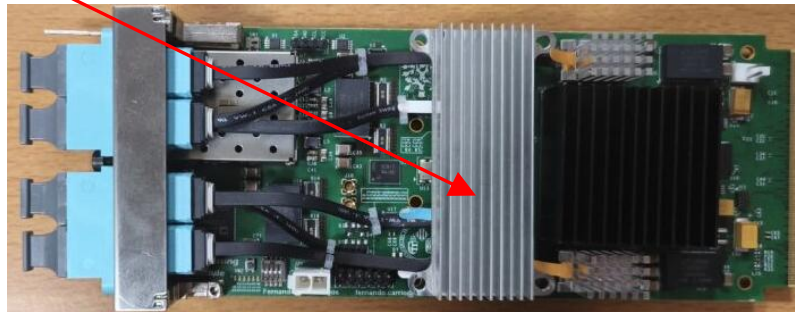
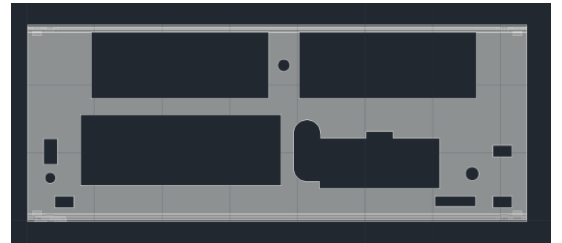
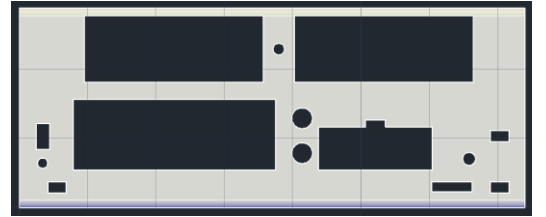
TileCoM v1.3



Compact Processing Module - Heatsink Mechanics

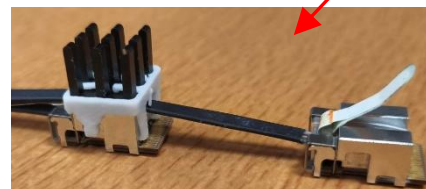


- Front panel design with minor modifications (David in contact with Mechanic workshop)
- Strict requirements to keep Firefly operating temperatures below 50°C
- ~~Full heatsink covering Fireflys and/or KU FPGA (v2.1)~~
- COTS heatsinks for Firefly TXs(640/640) and FPGA (70/160)
 - **One heatsink covering the 4 Firefly RXs.**
 - Still some risk of applying stress on the PCB + maintenance remains complex



– Custom plastic clip for independent heatsinks

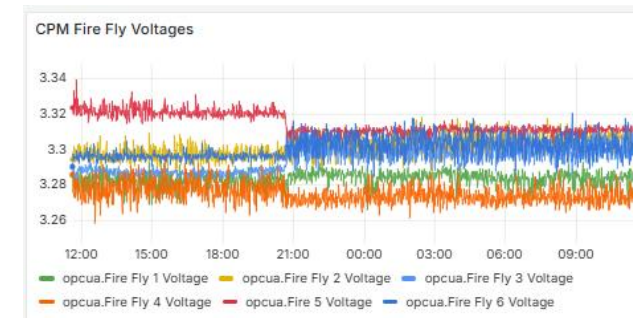
- No mechanical stress, easy maintenance
- Thermal performance acceptable
- Made in PA16 (Nylon)
- Being tested in 175



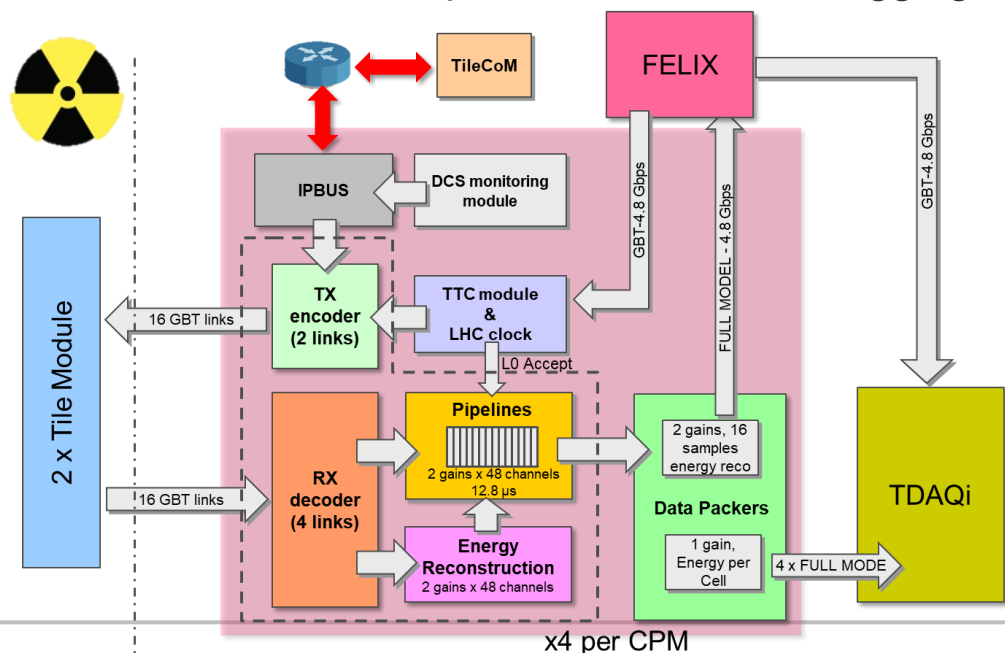
FW: Compact Processing Module



- Most functionalities in place and validated during test beams, VST and Demonstrator
 - 2 link @ 4.8 Gbps to FELIX: TTC and Readout + 1 GbE for IPbus communication
 - LTI - FULL MODE (9.6 Gbps) implemented -> **tested with BNL-155!**
 - 28 x links to DaughterBoards (4.8/9.6Gbps): **GBT with FEC and new data format**
 - 4 x links @ 9.6 Gbps to TDAQi: FULL mode
 - Remote programming via IPbus for both CPM and DaughterBoards
 - Block to detect corruption in the data samples to be added (stuck bits, spikes, etc)
 - Firmware updates for the DCS readings → Brenton as part of his Master thesis
 - Deployment in P1 by Brenton: Ipbus → IS → pBeast
 - Several firmware updates to extend debugging capabilities



DCS readings via IPbus



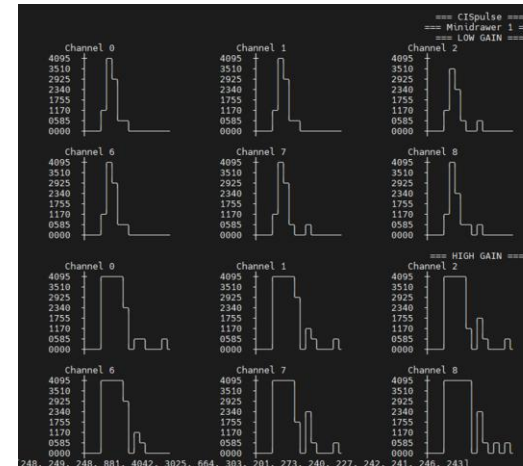
119 .. 116	115	114	113	112 .. 106	105	104	103 .. 92	91 .. 80	79 .. 68	67 .. 56	55 .. 44	43 .. 32	31 .. 0
H	M	I	RB	RSV	RR	G	P6	P5	P4	P3	P2	P1	FEC

Where:

- H: GBT header.
- M: DCS & monitoring data.
- I: Integrator data.
- RB: Read back commands.
- RSV: Reserved bits.
- RR: Reset Request from the Daughterboard.
- G: FEB gain. 0 is low gain and 1 high gain.
- Px: PMT samples.
- FEC: Forward Error Correction.

BW assigned	Assigned bits	Description/ max requirement
80 Mbps	4	GBT header → Used as returned BCR
80 Mbps	1	DCS monitoring data. It includes a maximum of 100 sensors * 10 Hz * 32-bit words for monitoring of temperature sensors, voltages and currents.
80 Mbps	1	Integrator data. It includes a maximum of 6 PMTs * 200 Hz * 32-bit words
80 Mbps	1	Read back of MB and DB registers
80 Mbps	1	Reset Request from the DB
80 Mbps	1	High and Low gain identifier
5.760 Gbps	72	PMT readout data
2.56 Gbps	32	Forward Error Correction

- Software ecosystem continuously evolving and growing up: Demonstrator, Prometeo, Vertical Slice Tests
- Online libraries for the CPM: TROOPER libraries
<https://gitlab.cern.ch/fcarrio/trooper-libraries/-/tree/master>
 - C++ libraries for TDAQ, also compiled as .so python libraries. Cmake, Make
- PrometeoPy application using them:
<https://gitlab.cern.ch/fcarrio/prometeopy>



PrometeoASCII with Trooper libraries



Grafana@ testbeam using pBeast + IS

- Preliminary software for DCS monitoring for the Demonstrator (Filipe, Brenton, Mpho)
 - Publishing into ATLAS IS -> pBEAST -> Grafana
 - OPC UA developments in parallel for Phase -II
- Control Prometeo Web panel
 - Control and monitoring of links
 - Fw loading and initialization

PROMETEO Control Panel

API connection OK

Configuration
 Auto-refresh: 2 s | Address: prometeo | Updated: 10/03/2026, 08:15:33

DaughterBoard

Side A: Fw version "0x9fca2025" | Jump FW | reset FW | Config

Side B: Fw version "0x9fca2025" | Jump FW | reset FW | Config

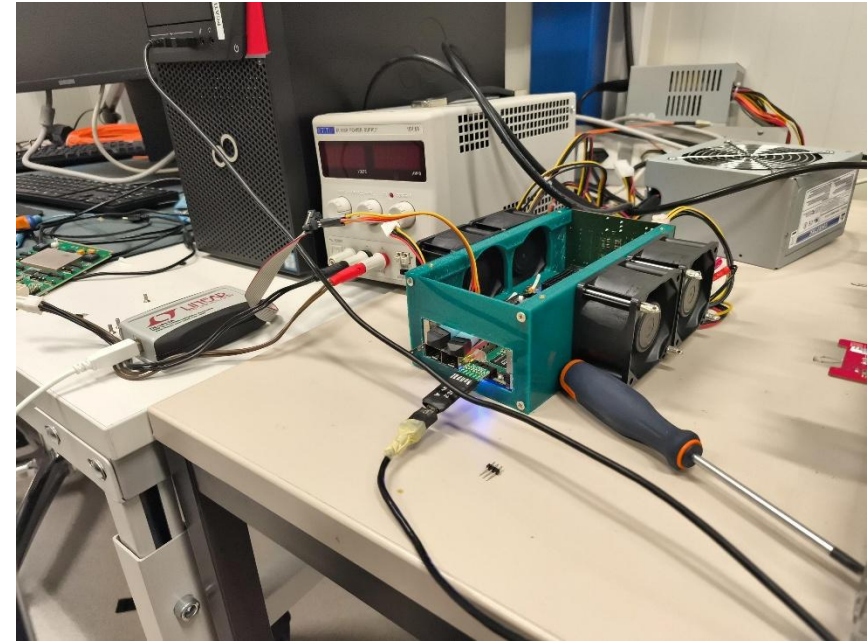
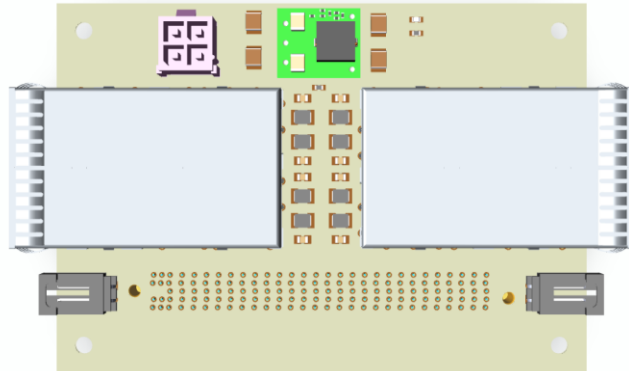
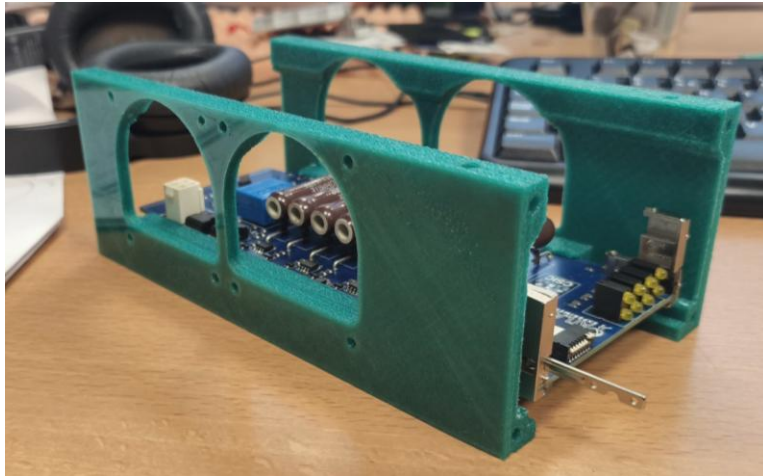
Compact Processing Module

resetRX | resetCounters

MD	Link	MGT TX RDY	MGT RX RDY	GBT HEADER	GBT RX RDY	Errors	BER	Effective	Frames	RTT
1	A0	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	A1	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	B0	1	1	1	1	0	6.86e-15	0	3641491715490	49
1	B1	1	1	1	1	0	6.86e-15	0	3641491715490	49

Control Prometeo Web panel

- 3D support for on-table test benches + Ethernet backplane -> Fully working
 - Support with built-in guidelines
 - Four 60 mm x 60 mm fans screwed into the support
 - Backplane with 4 SFP and providing power to CPM and fans



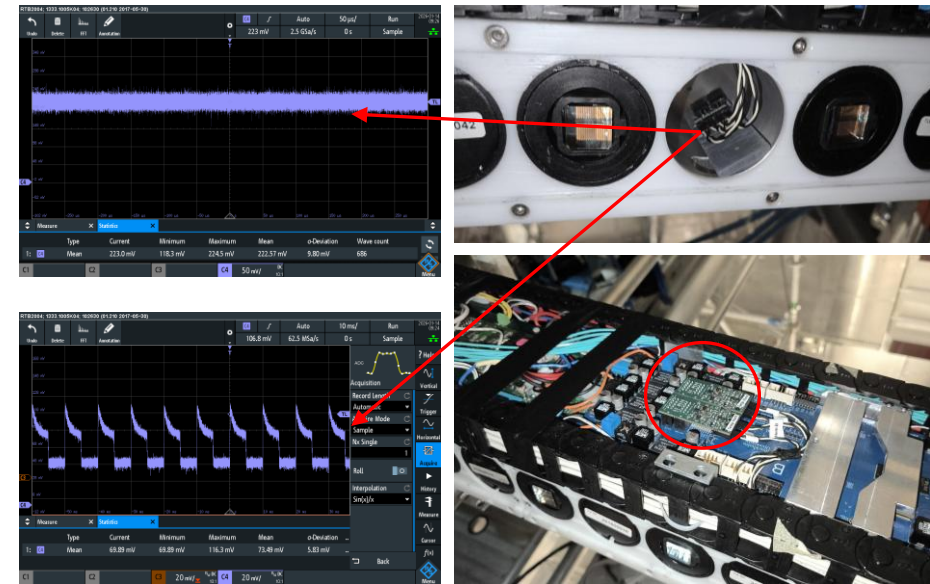
- PDR and FDR designs fully validated
 - All designs largely frozen before FDR, with no major issues identified
- Initial integration tests between CPM, Carrier, TDAQi
 - Home institutes, test beam area, Demonstrator
 - *GbE connection with TileCoM not fully validated in the carrier*
- Thermal tests completed in 2023 in SR1
 - Full system validated under worst-case thermal conditions
- Firmware and software quite advanced

- PreProduction of boards
 - TileCoM, GbE switch → Ongoing Valencia/SouthAfrica
 - ATCA carrier boards → VLC, 4 boards almost validated
 - Compact Processing Modules → VLC, 4 units under test
 - 9 more to be assembled in February/March
- Preproduction validation at home institutes during Q4'25-Q2'26
 - Definition and description of acceptance and validation tests
 - Functionality and stress tests to be done
- Additional integration tests at CERN: CPM + Carrier + TileCoM + TDAQi

2021

Q2 2026

- Environmental sensors installed in the Demonstrator as a candidate system for Phase-II
 - System controlled from Daughterboard GPIO pins and readout using XADC
 - Analog signal conditioning for temperature (PT100) and humidity (polymer) using INA333
 - Sealicon FGDOS for TID + Dickson bridge to charge it (20V)
 - Two sensors: 0-10 Gy and 0-50 Gy with 8-bit resolution
 - 2 sensor boards equipped in MD4, where probes has been installed in PMT hole 44
- Control of I2C and SPI lines from remote CPM via IPbus
 - Propagation signals via GBT protocol over fiber at 4.8 Gbps
 - 2 × SPI interfaces and 2 × I2C interfaces
 - LED trigger with LEMO
 - Fully working now



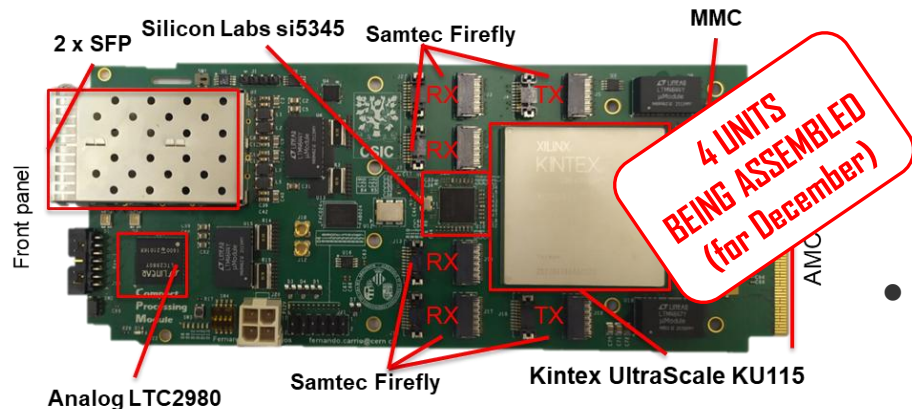
TileSensor board v1.0



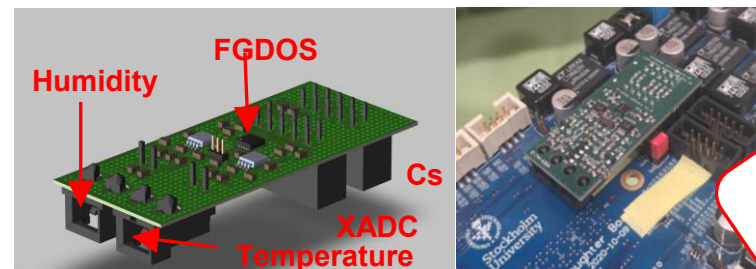
Tile GBTx board

BACKUP

- Revision 2.3 of the CPM
 - Single AMC board with full-size form factor
 - 6 x Samtec Firefly
 - XCKU115-2FLVA1517E



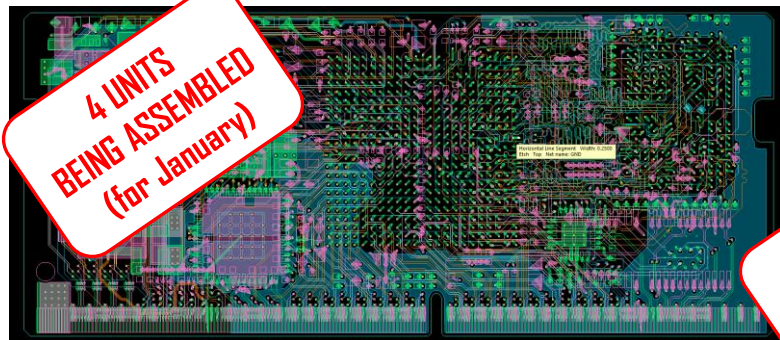
- Sensing environment conditions inside the TileCal modules
 - Analog signal conditioning for temperature (PT100) and humidity (polymer) using INA333 + Total Ionizing Dose (TID) sensor



TileSensor board v1.0

4 UNITS TESTED AND WORKING -to be installed in PI in January-

- Rev 1.3 of the TileCoM
 - SODIMM-240pin: 6.7 cm x 3 cm
 - 10 layers, 1 mm thickness, with 251 components



TileCoM v1.3

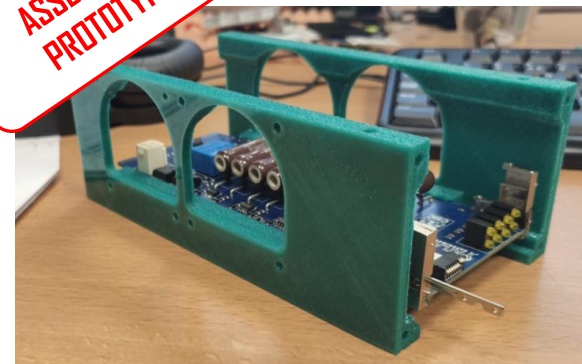
- Optical GBT-GPIO expander
 - Remote control of the HV and LED drivers from CPM



TileGBTx board v2.0

ASSEMBLING PROTOTYPE!

- Plastic support for on-table test benches + Ethernet backplane
 - Support with built-in guidelines
 - Four 60 mm x 60 mm fans
 - Backplane with 4 SFP and power distribution



UNDER DESIGN (Q1 2026)

