Strategy for SHiP Electronics, DAQ & Online

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Introduction

- **SHiP common electronics** has been evolving for almost a decade. It followed the evolution of technologies and of leading people involved.
  - We have a team of coordinators closely working together about Electronics, DAQ and Online.

- **Our goal has always been to find the best efficiency/cost optimization**

- **We now have a complete global architecture proposal for the TDR.**
  - **Details (like protocols) still need to be finely studied…**

- We have written an **EDMS document (link)** describing this architecture and the requirements for its implementation
  - It concerns the subdetectors specific elements as well as all the common items
  - Subdetectors are asked to give us their feedback, comments …
  - It will be regularly evolving based on these exchanges

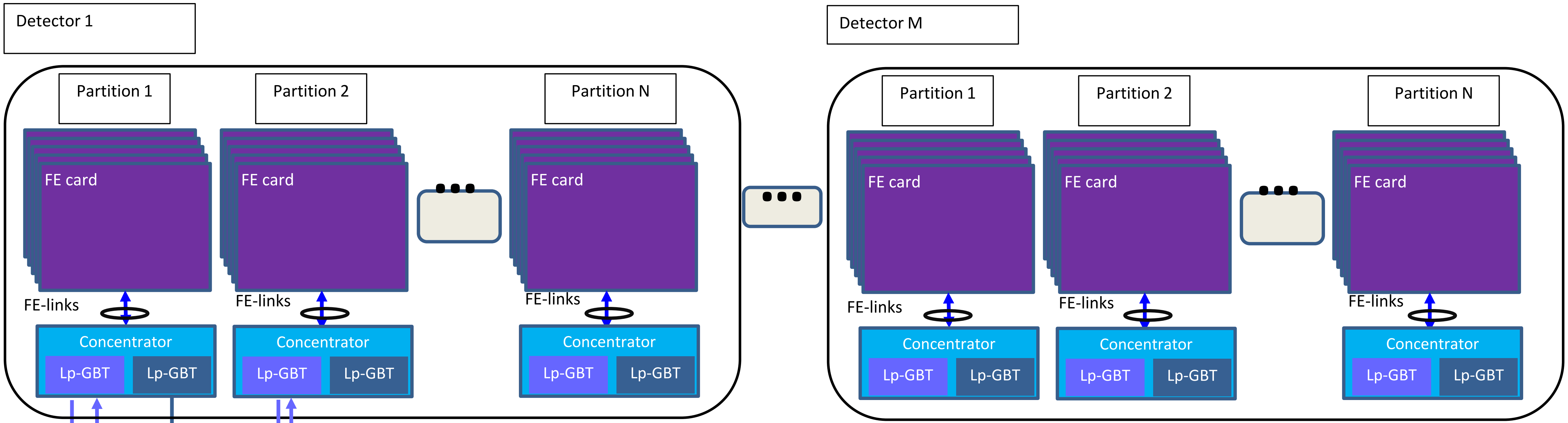
Main principles for SHiP

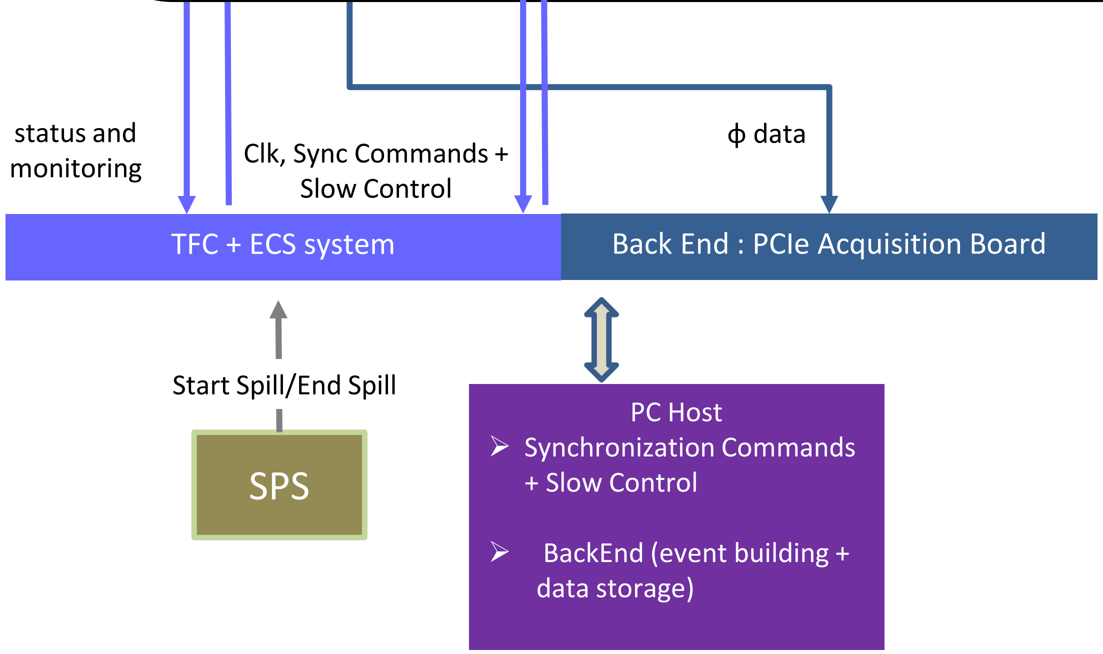
- Our goal from the beginning was to have a good flexibility associated with low cost and limited manpower for hardware development

  - **Architecture now based on LpGBT system developed at CERN for LHC experiments**
    - **Optimized for Triggerless** continuous readout during SHiP data Cycles.
    - **Time-tagged**: since the system is triggerless, **every piece of data has to be time-tagged in order to build the physics events**.

  - **At the level of subdetectors, simple links are proposed, which can be implemented inside low cost FPGAs or CPLDs.**
    - The option of directly using LpGBTs there still remains possible
    - The scheme for the interface between the concentrator boards and the FEE has been recently simplified
    - Other readout options could be envisaged but **only for data links**

Global System architecture





TFC/ECS FE-link : 4 LVDS copper pairs

- Clk : 40 MHz
- TFC (downstream link): 80, 160 or 320 Mb/s ?
- ECS (downstream control link): 80, 160 or 320 Mb/s ?
- Status/Monitoring (upstream): :80, 160 or 320 Mb/s

ϕ data FE-links : 4 LVDS copper pairs / link

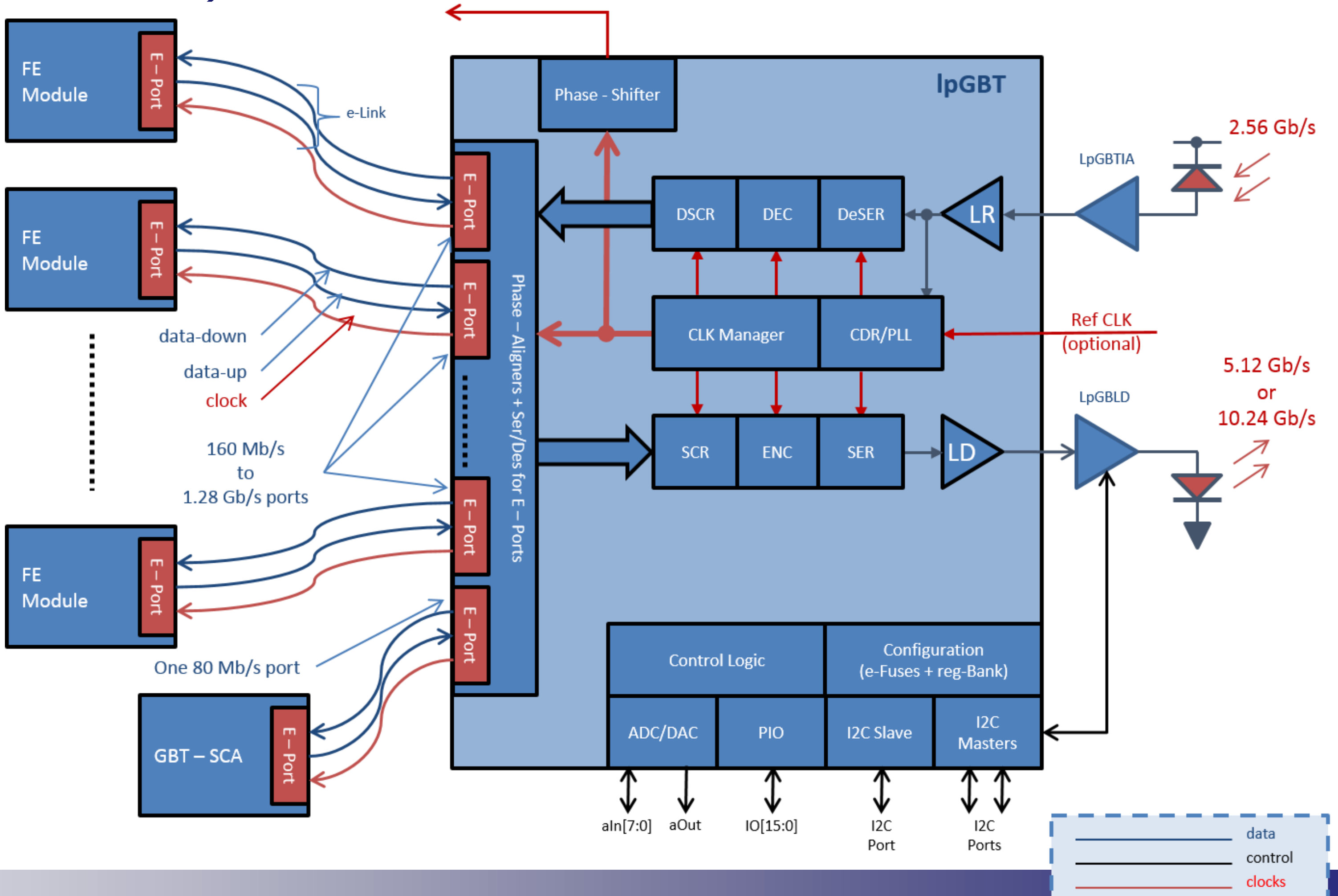
- ϕ data (upstream links) : high speed between 160 Mbps and 1280 Mbps

LP-GBT Main characteristics

- The lpGBT is a low-power-Giga-Bit-Transceiver https://gbtproject.web.cern.ch/gbtproject/#lpgbt-ecosystem
- It converts optical fibres into:
  - Several e-ports with a number of e-links (upstream & downstream)
  - Clock outputs with good timing performance

  (also : I2C master, slow ADC/DAC, GPIO …)

  - 7 downstream eports
  - 4 upstream eports
  - 28 clock outputs
- Every eport can have between 1 and 4 e-links, depends on configuration (see next slide)



LP-GBT Main characteristics

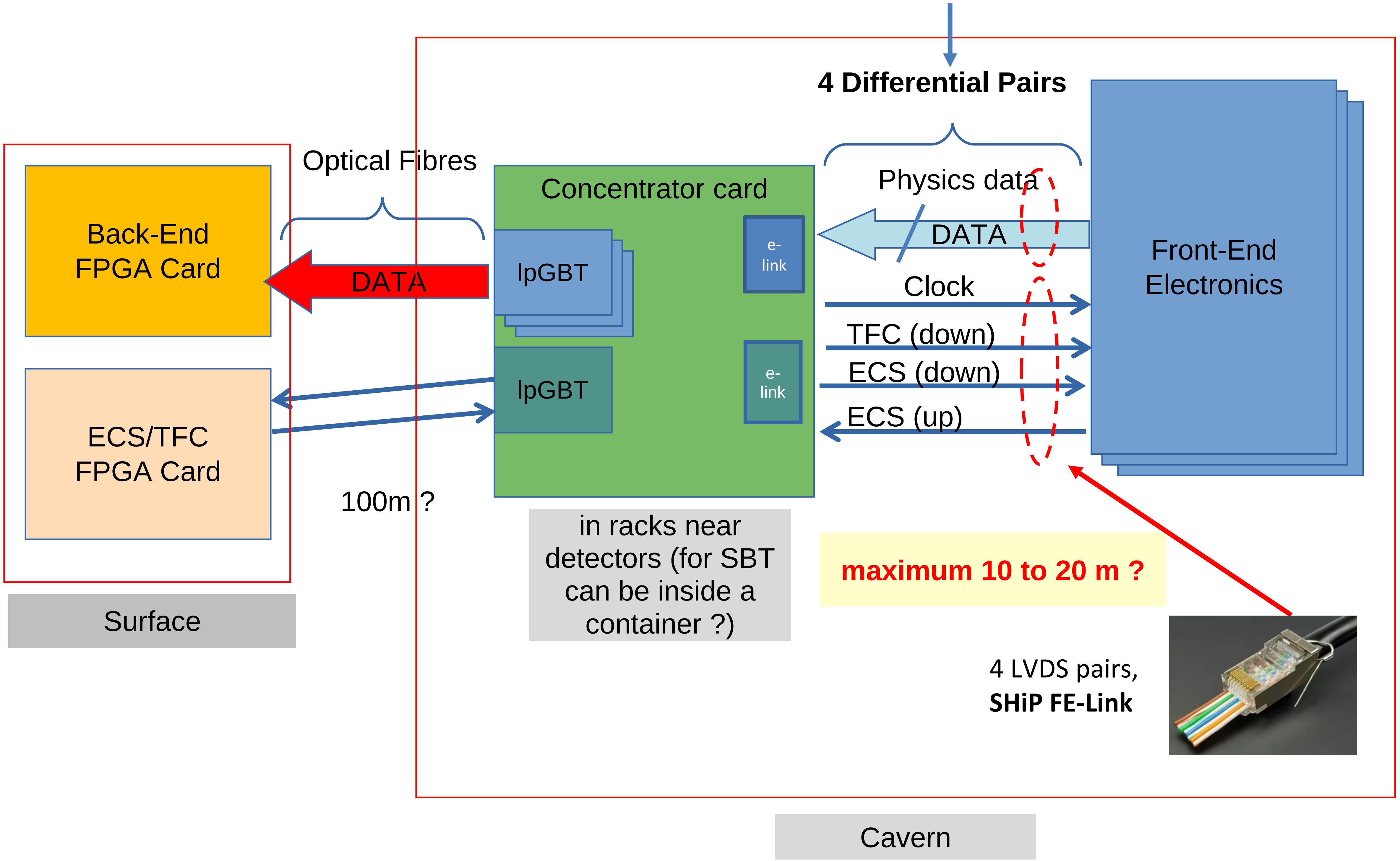
- The lpGBT can operate in many ways:
  - TX/RX/Full-Duplex (2 fibres per lpGBT, are not mandatory!)
  - **Speed : 10,24Gbps** or **5,12Gbps** upstream (ϕ data). Downstream fixed to **2.56Gbps** (TFC + ECS).
  - FEC12 and FEC5: Forward Error Correction systems
    - FEC12 => More robust, but less usable bandwidth available
  - e-ports can operate at various frequencies
    - Downstream (for TFC and ECS): 80Mbps, 160Mbps, 320Mbps
    - Upstream (monitoring or physics data): 160Mbps, 320Mbps, 640Mbps, 1280Mbps

Output eLinks (down-link)			
Bandwidth [Mb/s]	80	160	320
Maximum number	16	8	4

Input eLinks (up-link)												
Up-link bandwidth [Gb/s]	5.12						10.24					
FEC coding	FEC5			FEC12			FEC5			FEC12		
Bandwidth [Mb/s]	160	320	640	160	320	640	320	640	1280	320	640	1280
Maximum number	28	14	7	24	12	6	28	14	7	24	12	6

Proposed scheme

One link for control and N links for data



Status (1)

- This scheme permits optimizing the control and readout without the need of an FPGA on the concentrator boards, but with one on the FE.
  - The elinks can be used directly in transmission and reception via the differential pairs
  - The **number of pairs for data readout is independent** of the number of FE links for clock and control => it thus offers the possibility to the subdetectors to optimize their number of links

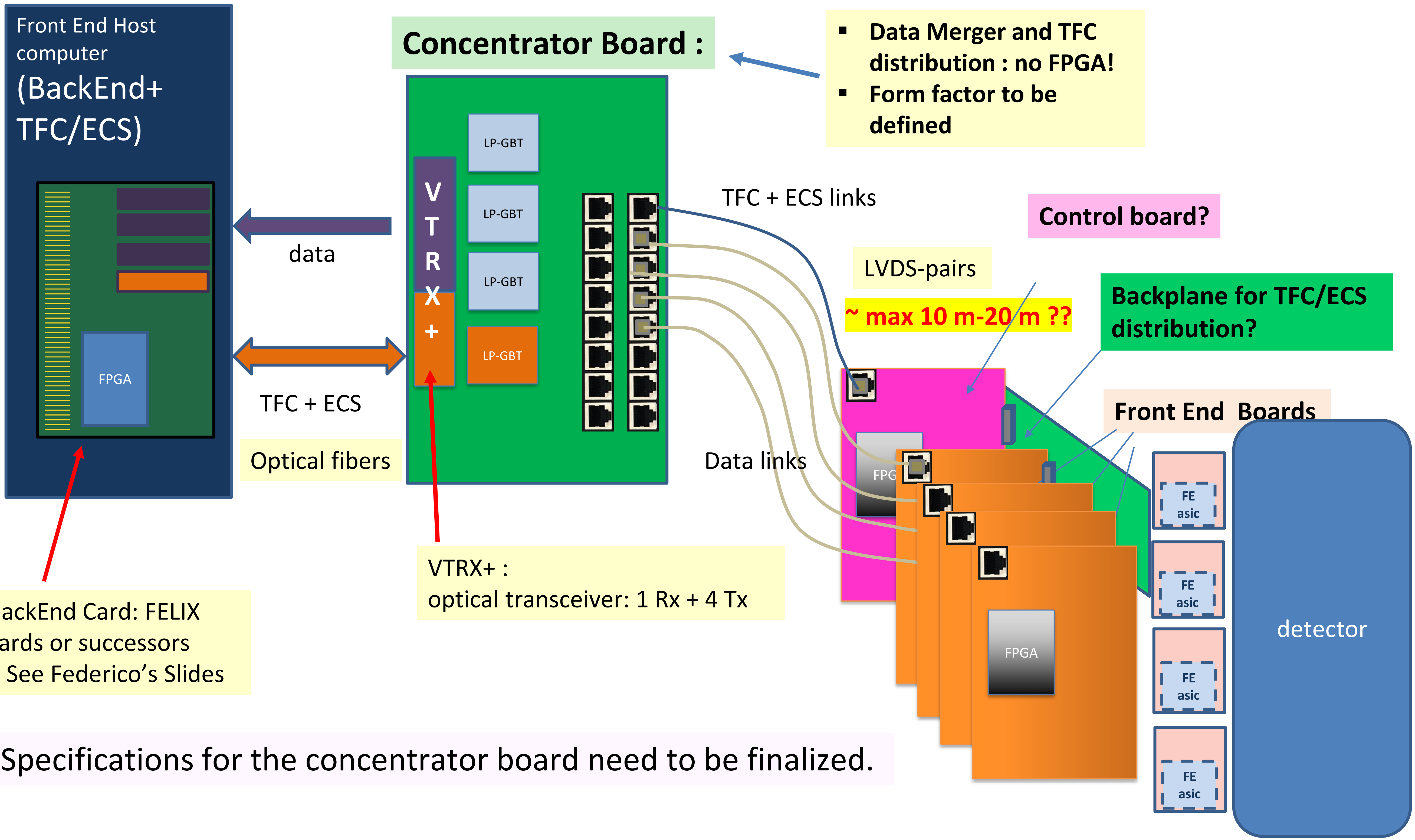
- It permits making use of the existing VLDB+ board, connected via FMC connectors to a FPGA demo kit, to emulate the readout of detector data (currently under tests at CERN)
  - We have to measure the correlation of bit rat vs cable length
- The development of a FPGA-based intermediate board between FE and concentrator is also envisaged for subdetectors who want to avoid having the FPGA directly on FE (like SBT for managing the FastIC+).

Status (2)

- The next step will be the definition of the data formats inside the different links
  - Not forgetting the need for field busses like I2C, SPI, JTAG => the interfaces with the ECS pairs will be implemented in FE FPGA firmware
  - And the need for **FPGA reconfiguration** => ECS pairs directly connected to dedicated CPLD

- **A new constraint**: while we tend to reuse many elements from former experiments, including FE electronics, we need to ensure the compatibility with our architecture (not always evident …)
  - Intermediate FPGAs might also be required there to implement interfaces between existing hardware/firmware and our common items
  - This is supposed to be under responsibility of concerned subdetectors, except if a common set of requirements can emerge.

Example of standard implementation



Specifications for the concentrator board need to be finalized.

Detectors Summary table

[Shared link]

Subdetector	Sd High-Granual Calorimeter (SHGC)	Sd Tracking Calorimeter Pads (STCP)	Sd Tracking Calorimeter sciFi (STCF)	Dd Background Tagger Straw (DBTS)	Dd Background Tagger Timing (DBTT)	Dd Surround Background Tagger (DSBT)	Dd Spectrometer Straw Tracker (DSST)	Dd Spectrometer Timing Detector (DSTD)	Dd ECAL (DECA)	Dd Ecal Precision Layers (DEPL)	Dd HCAL (DHCA)
SubDetector TB Conveners		K. Skovpen, N. Anfimov		T. Bowcock	K. Skovpen, N. Anfimov	H. Lacker, H. Fischer	D. Bick	G. Vasquez, C. Betancourt	W. Bonivento, R. Wanke	W. Bonivento	W. Bonivento, R. Wanke
SubDetector Electronics Contact											
Involved Institutes		Gent	EPFL	Liverpool	Gent/EPFL	Berlin	Hamburg	Zurich	Mainz		Mainz
Type of particle detector											
Source of electronics signals											
# channels											
Type of Measurement (Time, Charge, ToT, Hit (0/1), Waveform ...)											
Time window (ns)											
Resolution (ns)											
Type of Very FE Electronics (Amplifier, Discriminator ...)											
Very FE circuits (ASIC name, Discrete components ...)											
Noise Counting Rate /Ch ?											
Local conditions for channel triggering											
Double Hit resolution (deadtime ns)											
Maximum Latency between particle and signal transmission (ns)											
FE electronics localisation											
Calibration procedure?											
Type of configuration data on-detector (Registers, RAM ...)											
Amount of configuration data (Bytes)											
Data Link Type (example : FE-Link, LP-GBT or other?)											
Data link speed (FE-Link or Other) (Mbits/s)											
Total Number of FE-Data links											
Common Data Concentrator (yes/no)											
Specific Data Concentrator (yes/no)											
Total Number of Common Data Concentrators											
Current Readout Solution existing, re-used											
Hits/particle (avg, max)											
Particles/spill											
Payload per Hit (Bytes/hit) : *(using the common data structure)*											
Total Hits/ Spill											
Total Data/ Spill [Mbyte]											
Tracks/event											
Events/spill											
Event overlap fraction (spillover)											

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…rs Summary table to fill

- SubDetector TB Conveners
- SubDetector Electronics Contact
- Involved institutes
- Type of particle detector
- Source of electronics signals
- # channels
- Type of Measurement (Time, Charge, ToT, Hit (0/1), Waveform …)
- Time window (ns)
- Resolution (ns)
- Type of Very FE Electronics (Amplifier, Discriminator …)
- Very FE circuits (ASIC name, Discrete components …)
- Noise Counting Rate /Ch ?
- Local conditions for channel triggering
- Double Hit resolution (deadtime ns)
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- FE electronics localisation
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- Current Readout Solution existing, re-used
- Hits/particle (avg, max)
- Particles/spill
- Payload per Hit (Bytes/hit) : (*using the common data structure)*
- Total Hits/ Spill
- Total Data/ Spill [Mbyte]

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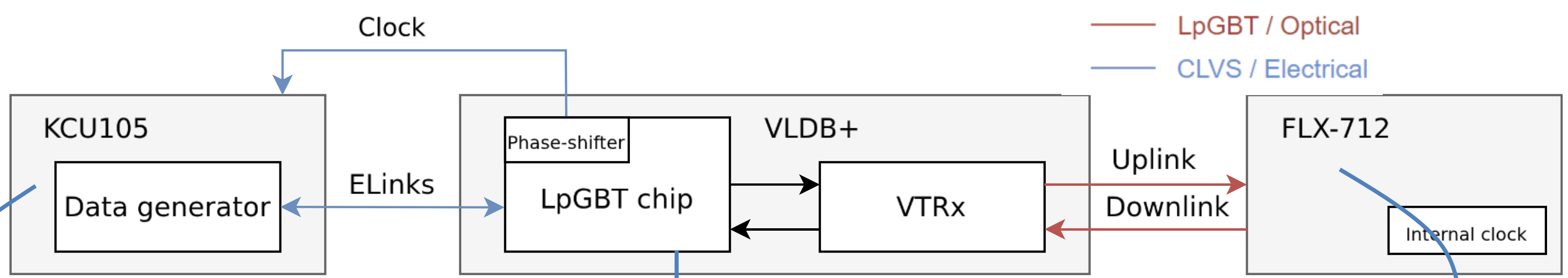
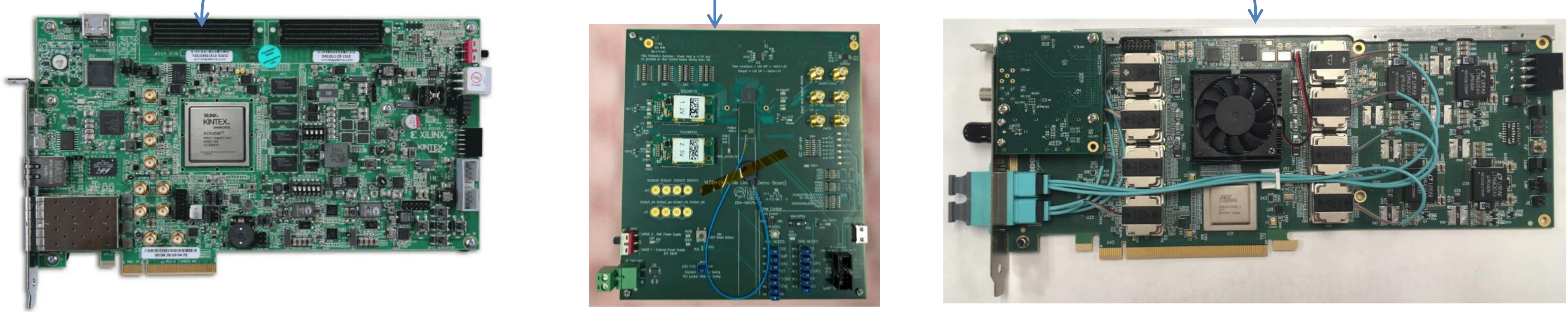
…fimov		T. Bowcock	K. Skovpen, N. Anfimov	H. Lacker, H. Fischer	D. Bick	G. Vasquez, C. Betancourt	W. Bonivento, R. Wanke	W. Bonivento	W. Bonivento, R. Wanke
	EPFL	Liverpool	Gent/EPFL	Berlin	Hamburg	Zurich	Mainz		Mainz

TFC & DAQ test benches

- Testbenches being currently developed: Testbench KCU105 & VLDB+
  - KCU105 generates emulated Elink data and sends it via CLVS to the VLDB+.
  - Clock can be taken from the phase-shifted clock of the VLDB+ or its Elink clocks.
  - Currently performing physical verification.



From José Javier GONZÁLEZ ABASCAL



- In the future : **NetFELIX**
- Joint project from several experiments: ATLAS, ALICE, LHCb, SHiP…
- Objective: Common BackEnd solution (hardware + firmware). Current phase: Design specifications.
- So far SHiP BE tests in FLX-712 and will use FLX-155 when available.
- NetFELIX will be the next generation after FLX-155.

Summary

- **We are in the process of getting subdetector final feedback about the architecture proposal in order to be able to design the missing SHiP-specific common items.**

- **The design of the concentrator board has recently been taken care of by a new German group**

- **At the subdetector levels, different options of complexity are envisaged.**
  - A new option could be that the required FPGA interface be transferred to a common intermediate board

- There is space for participation, especially in the field of:
  - FE electronics
  - Help for groups aiming at using ASICs like FastIC+
  - At the interface between FE and common electronics.