Meeting BPM IFIC

Project meeting - 27th of January 2026

Juan Carlos Fernández Ortega, Laura Karina Pedraza, Daniel Esperante, Nuria Fuster Martínez, Marçà Boronat, César Blanch, Benito Gimeno, Daniel González

juancarlos.fernandez@ific.uv.es

TABLE OF CONTENTS

1. Introduction

May design

2. Local Oscillator Generator
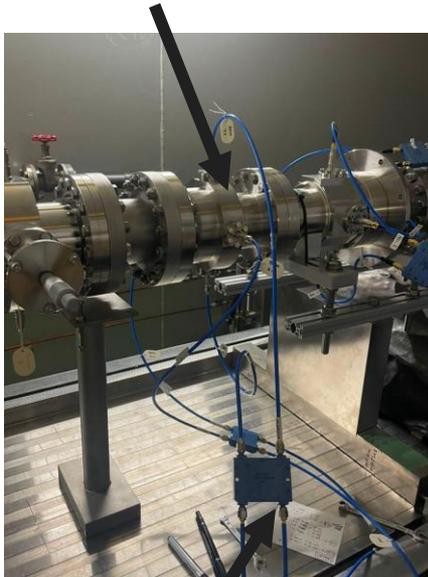
1. Downconversion system

3
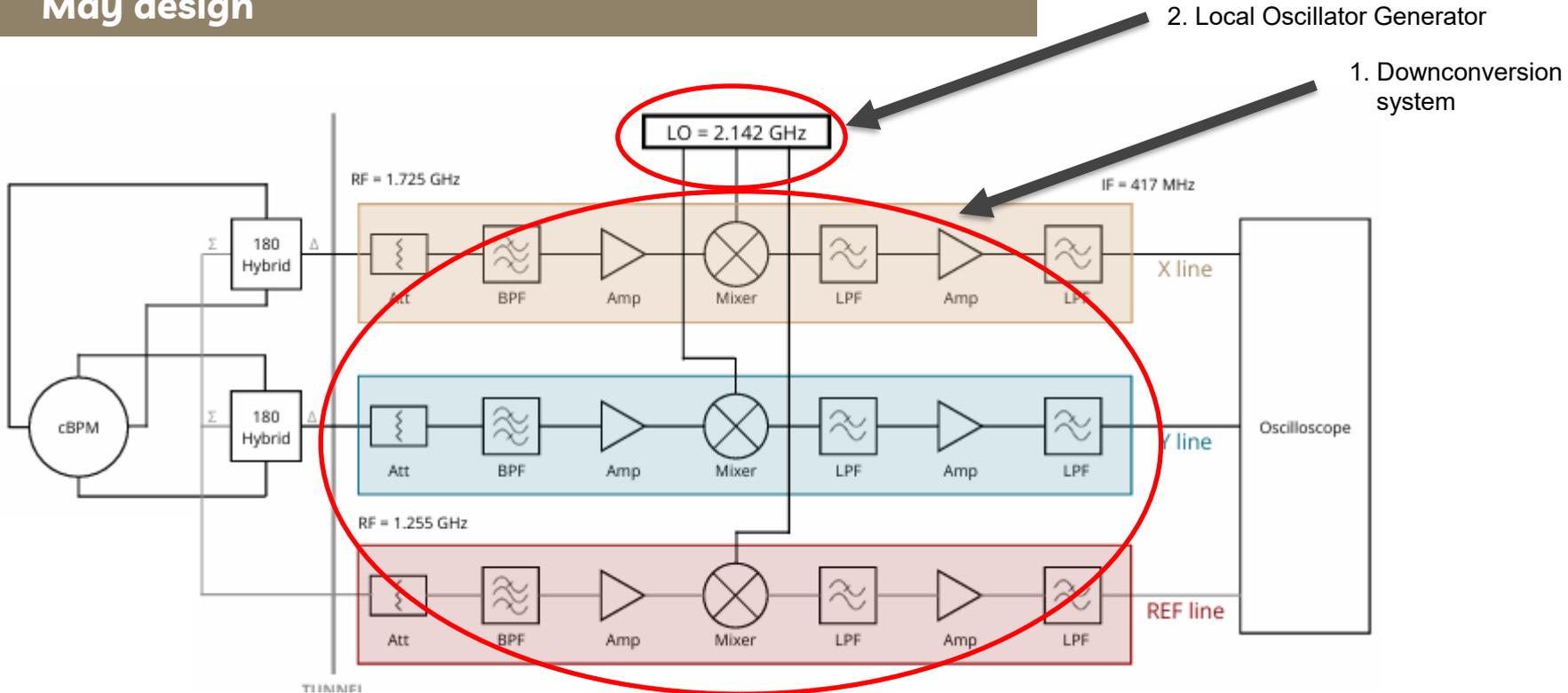
2. Double downconversion
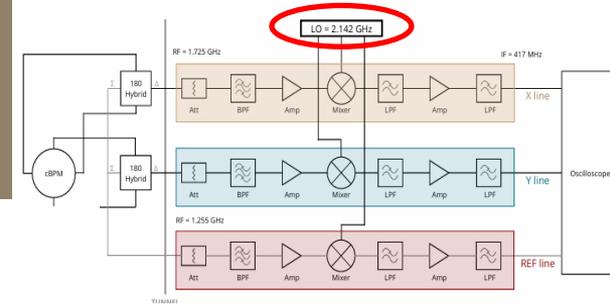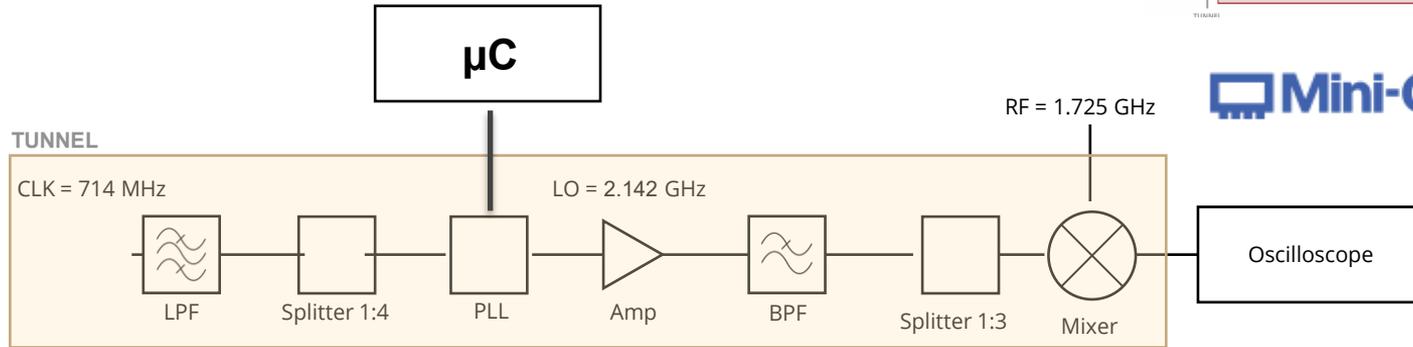
- **Local Oscillator input is 714 MHz from ATF RF slave signal generator and generates the necessary frequency multiples for synchronization between our system and ATF bunch repetition rate.**

- **Microcontroller programs the PLL via the SPI protocol to ensure accurate frequency control.**

2. Double downconversion

cBPM

Hybrid coupler

I N S I D E   T U N N E L

Downconversion system

LO signal generator

Oscilloscope
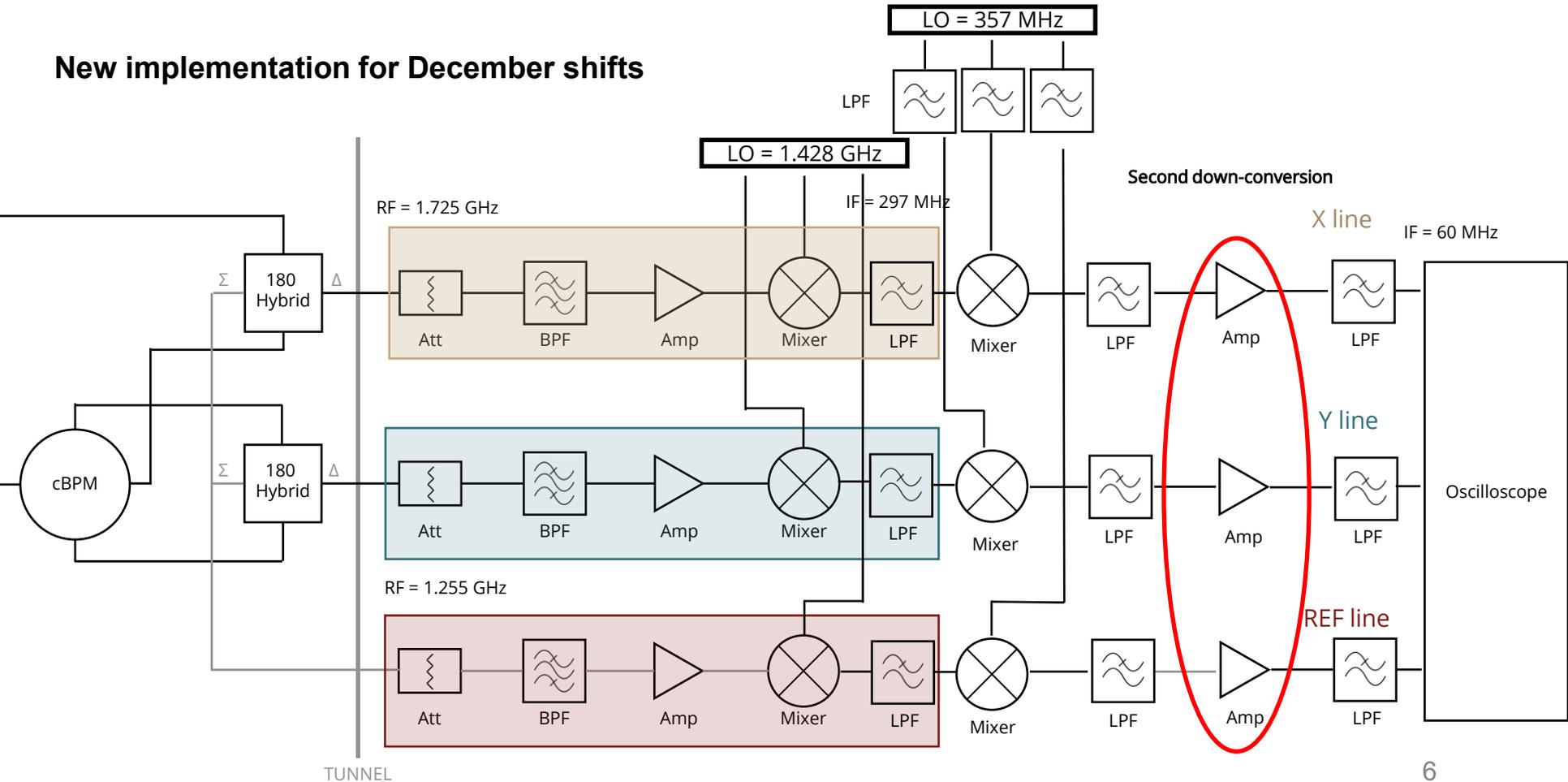
NEXT TO TUNNEL

C O N T R O L   R O O M

DDC algorithm for signal processing

Resolution measurement

Calibration procedure of the cBPM

5

New implementation for December shifts

O. Friar, Building, Optimising and Measuring the Performance of Downconverting electronics using X-Microwave Modules, Major Project Report, 2022

2. Double downconversion

June design (Local Oscillator generator)

Mini-Circuits

- **1st downconversion**

- **2nd downconversion**

μC

μC

TUNNEL
CLK = 714 MHz

LO = 2.142 GHz

RF = 1.725 GHz

PLL

Amp

BPF

Splitter 1:3

Mixer

TUNNEL
CLK = 714 MHz

LO = 357 MHz

RF = 297 MHz

PLL

LPF

Splitter 1:3

Mixer

Oscilloscope
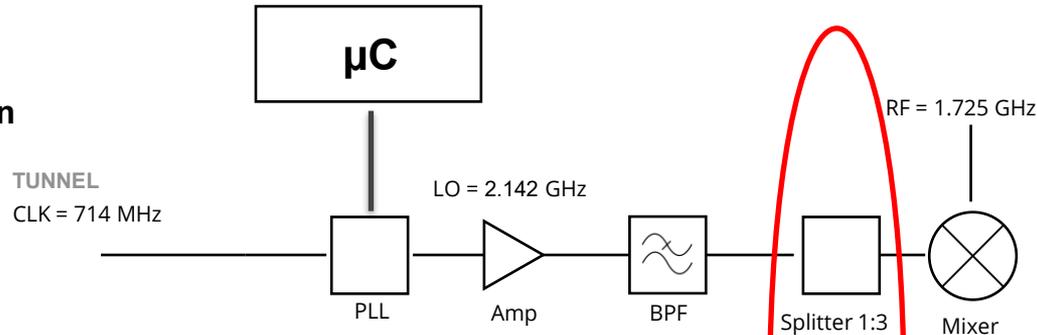
- **Different mixers**
- **2nd mixer needs a lower input power.**

7
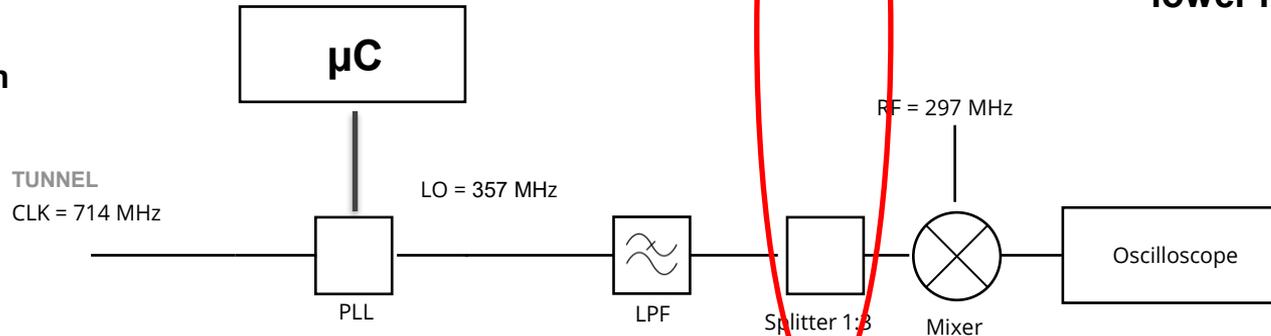
Coaxial
Frequency Mixer

Level 7 (LO Power +7 dBm)   5 to 1000 MHz

Splitter 1:2

Mixer   LPF   LPF   Mixer

LPF   LPF
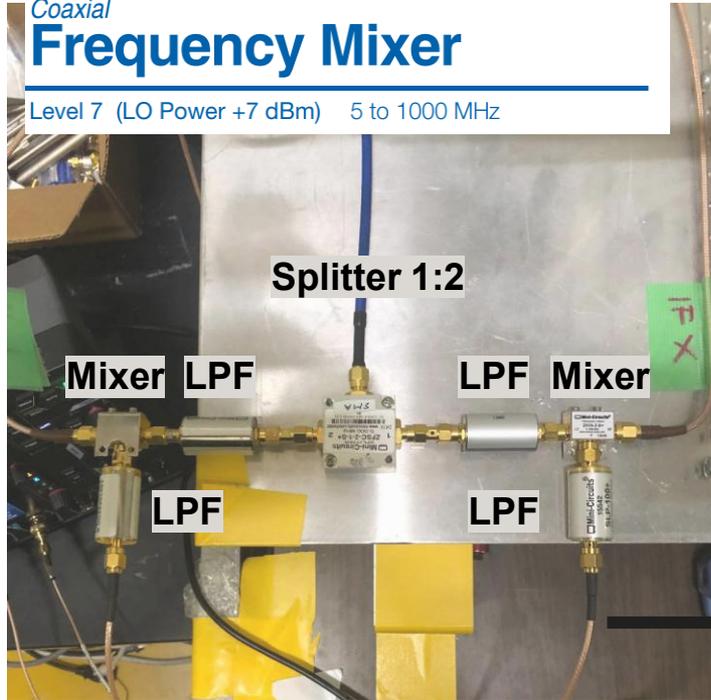
- **Amplifier of ATF.**
- **Possible saturation…**
- **Need of similar amplifier.**

Low Noise Amplifier

ZFL-500HLN+
ZFL-500HLN

50Ω   10 to 500 MHz

Features
- low noise, 3.8 dB typ.
- high IP3, +30 dBm typ.

Applications
- VHF/UHF
- small signal amplifier
- communications system

CASE STYLE: Y460

Connectors	Model	Price	Qty.
SMA	ZFL-500HLN(+)	$99.95	(1-9)
BRACKET (OPTION "B")		$2.50	(1+)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications.

Low Noise Amplifier Electrical Specifications

MODEL NO.	FREQUENCY (MHz)		NOISE FIGURE (dB)	GAIN (dB) Flatness Max.		MAXIMUM POWER (dBm)		INTERCEPT POINT (dBm)	VSWR (:1) Typ.		DC POWER	
	f_L	f_U	Typ.	Min.	Total Range	Output (1 dB Compr.)	Input (no damage)	IP3 Typ.	In	Out	Volt (V) Nom.	Current (mA) Max.
ZFL-500HLN(+)	10	500	3.8	19	±0.4	+16	+15	+30	2.0	2.0		110

8

3. FPGA + ADC

A) FPGA and ADC Project Status

FPGA (first tests)

Artix 7 – AC701 for testing, probably will change to a FPGA manufactured by IOXOS company.

FPGA+ADC manage data position information in real-time signal processing.

ADC: 16 bit, 250 Msps, 8 channels.

BUT... if 60 MHz double-downconversion finally works fine:

Considering this ADC: 16 bit, 250 Msps, 8 channels.
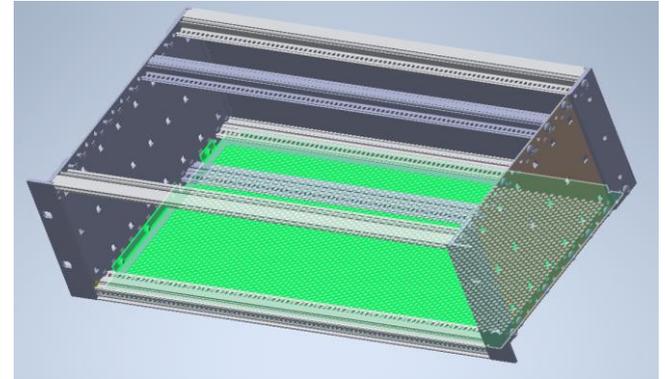
4. Hardware improvements

- Make more compact system and reliable.
- Change of frequency output due to problem of synchronization with ATF (resolved in May Shifts). However, we have changed some components in this set of shifts.
- Preparing all these changes done during July-November in Valencia.
- These changes have been performed in the last two weeks of November at ATF.

Set analog down-conversion system inside new crate,
similar crate that Local-Oscillator signal.

Front panel

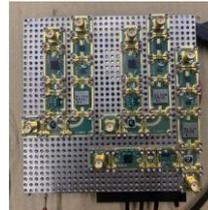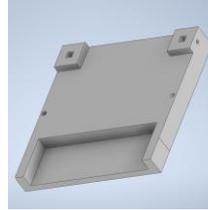**Back panel**

4. Hardware improvements

- Make more compact system and reliable.
- Change of frequency output due to problem of synchronization with ATF (resolved in May Shifts). However, we have changed some components in this set of shifts.
- Preparing all these changes done during July-November in Valencia
- These changes have been performed in the last two weeks of November at ATF.

Set new holders for PLL inside Local Oscillator crate and set new aluminum plates for analog components.
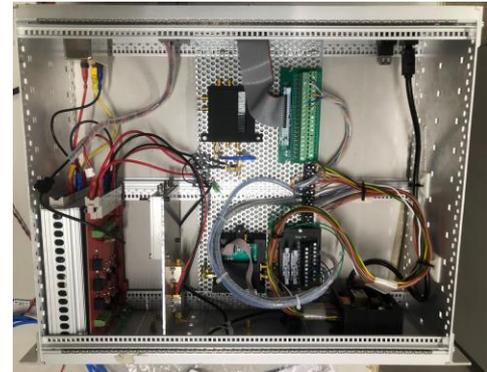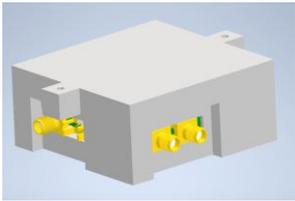
5. Future work

	2025	2026		2027	
	Oct - Dec	Jan - Jun	Jul - Dec	Jan - Jun	Jul - Dec
Finalize CEA BPM performance characterization	🟩	🟩	🟩		
Test with beam the new cavity BPM		🟩	🟩	🟩	🟩
Develop and test the partially o fully digital DAQ system	🟩	🟩	🟩	🟩	🟩
Investigate how to evaluate the BPM-spQM alignment accuracy	🟩	🟩	🟩	🟩	🟩
Mechanical design of dummy model BPM-flanges-beam pipe			🟩		
Construction of dummy model BPM-flanges-beam pipe			🟩	🟩	
Test dummy model at test cryostat at KEK				🟩	🟩

5. Future work

- ✓ Beam time along 2025, 2026 and 2027 (once or twice per year)

- ✓ Installation of new prototype in 2026 adding it to the LINAC at ATF.

- ✓ Test new cavity BPM performance at ATF.

- ✓ Develop the DAQ system based on µTCA and try to implement at ATF.

2026

January						
Su	Mo	Tu	We	Th	Fr	Sa
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

February						
Su	Mo	Tu	We	Th	Fr	Sa
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28

March						
Su	Mo	Tu	We	Th	Fr	Sa
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

Meeting BPM IFIC

Project meeting - 27th of January 2026

Juan Carlos Fernández Ortega, Laura Karina Pedraza, Daniel Esperante, Nuria Fuster Martínez, Marçà Boronat, César Blanch, Benito Gimeno, Daniel González

juancarlos.fernandez@ific.uv.es