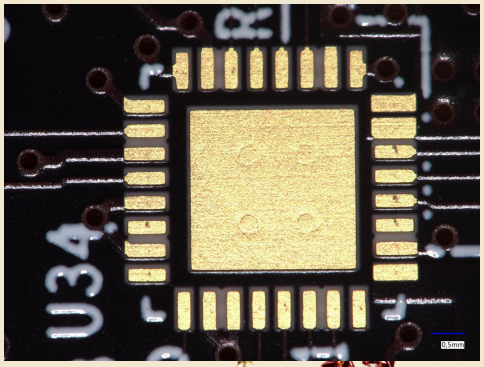
2025 activities

Alberto Valero

Carrier board progress

- 4 units of ACBBv2.3 produced
- Assembly in Prodesign. Only minor problems
- Changes identified for final version. No showstopper for FDR
- Main one: DAMN problem: some solder mask removed during fabrication due to distances < 0,2 mm



Instituto de Física Corpuscular (University of Valencia - CSIC)

CSIC | Universitat de València | IFIC

PCB Fabrication specifications

Designation

Name:	TileACBB	**Date:**	3/3/25
Version:	2.3	**Designer:**	Alberto Valero
Contact:	alberto.valero@cern.ch		

Mechanical specifications

External dimensions (mm):	280 x 322.25 mm	**Thickness (mm):**	2.42
Layers:	14	**Panel:**	No

Copper Thickness

External Layers (µm):	42	**Internal Layers (Signal) (µm):**	35
		Internal Layers (Planes) (µm):	35

Board Finish requirements

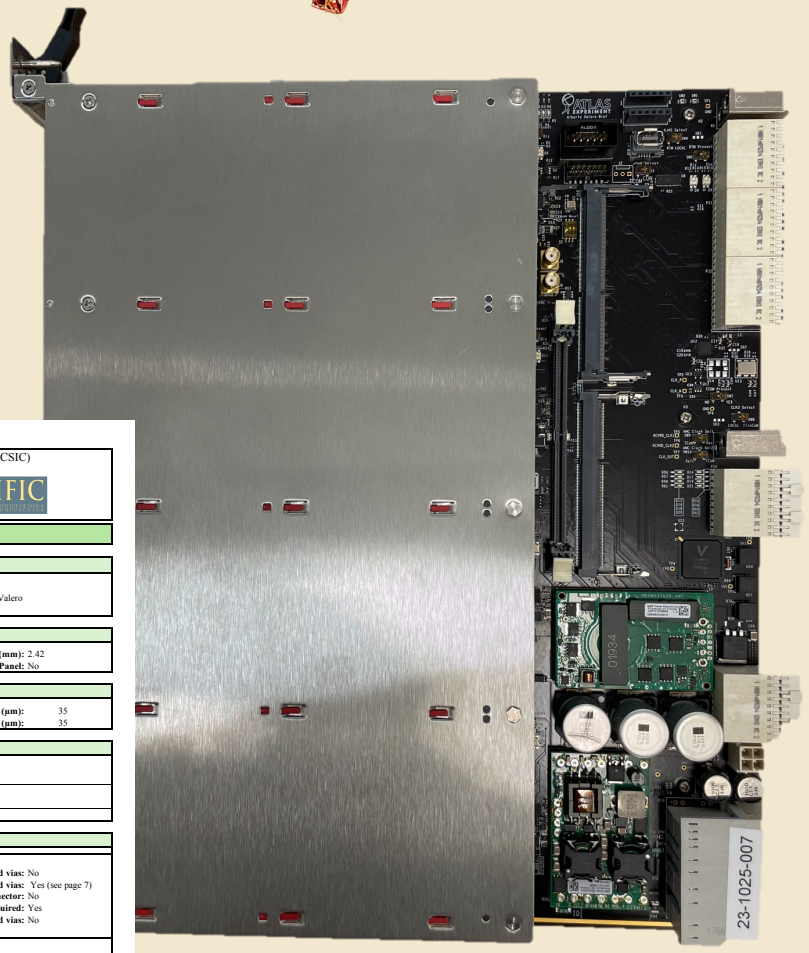
Silkscreen TOP:	Yes	**Silkscreen BOTTOM:**	Yes
Silkscreen color:	White		
Soldermask TOP:	Yes	**Soldermask BOTTOM:**	Yes
Soldermask color:	Black		

Surface Finish: ENIG - Electroless Nickel/Immersion Gold according to ***IPC-4552***

Additional Information

Dielectric Material:	Panasonic Megtron-6 Halogen Free		
Minimun Track Width (µm):	100	**Blind vias:**	No
Minimum Hole Diameter (µm):	150	**Filled and Caped vias:**	Yes (see page 7)
Minimum track/pad clearance (µm):	100	**Card Edge Connector:**	No
Press-fit trhough holes:	Yes (see page 3)	**Test Coupons Required:**	Yes
Electrical Test:	Yes	**Buried vias:**	No

Controlled Impedance:	Layers 3 and 12
Impedance unipolar:	50 Ω
Impedance edge couple offset striplines:	100 Ω

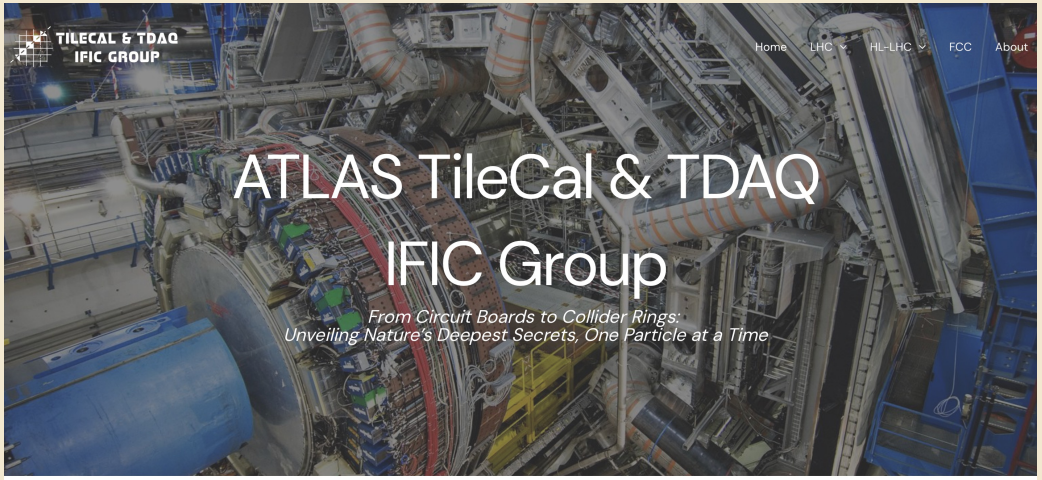


Components

- FPGAs for CPMs : all in hands!
- SAMTEC Firefly: only missing 50 TX and 80 RX
- SFPs: in hands
- Mechanical kits: all in hands
- Dry Cabinet installed in computer room (low temp/hum)

Webpages

tilecal.ific.uv.es



Our research activities

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Thank You!