Summary of activities

(mainly Compact Processing Module…)

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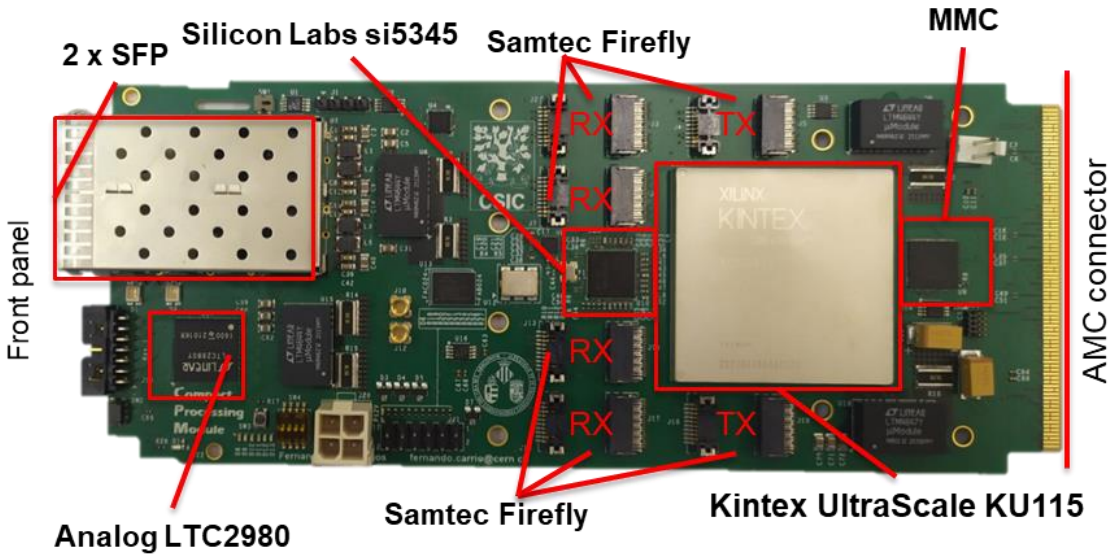
TileVLC meeting

HW: Compact Processing Module - Overview

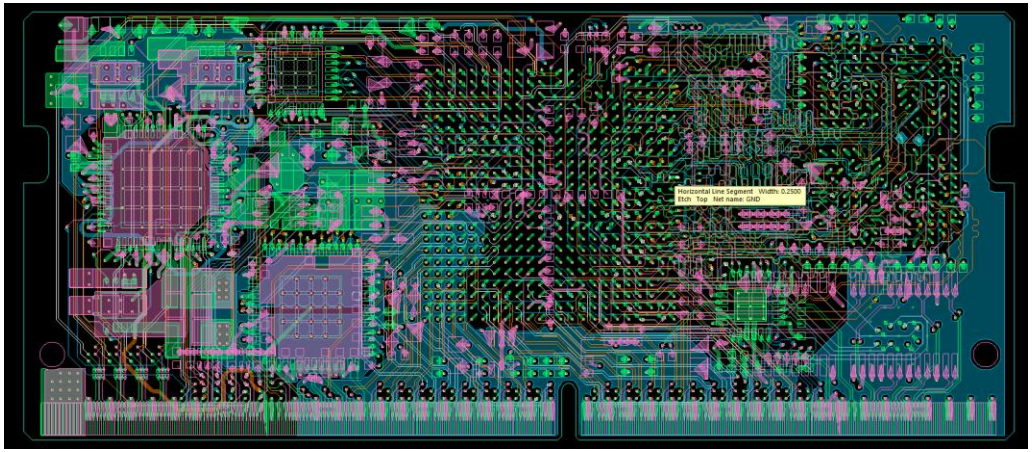
- **Single AMC board** with full-size form factor
  - **6** x Samtec Firefly
  - **Up to 14 channels** via AMC connector
  - **XCKU115-2FLVA1517E**
- Status of CPM v2.3:
  - Minor changes wrt to last the version
  - 20 PCBs produced and 4 CPMs being assembled in Rompal SA
  - Additional 12 to be produced in Jan with speed grade -1
  - Mechanics being produced at IFIC
    - Front panel and heat sink

- Procurement status @ Valencia
  - All active components for 128 CPMs received
  - Received 60% FPGAs for production
  - 260 TX Firefly modules arrived
  - Last batch of 100 RX Firefly modules received after firmware update
    - 110 previous ones not updated, no impact in optics
- Procurement status @ Wits
  - All FPGAs for production
  - Procurement for the prod of the TileCoM ongoing
  - Producing GbE switches (?)



HW: TileCoM v1.3 updates

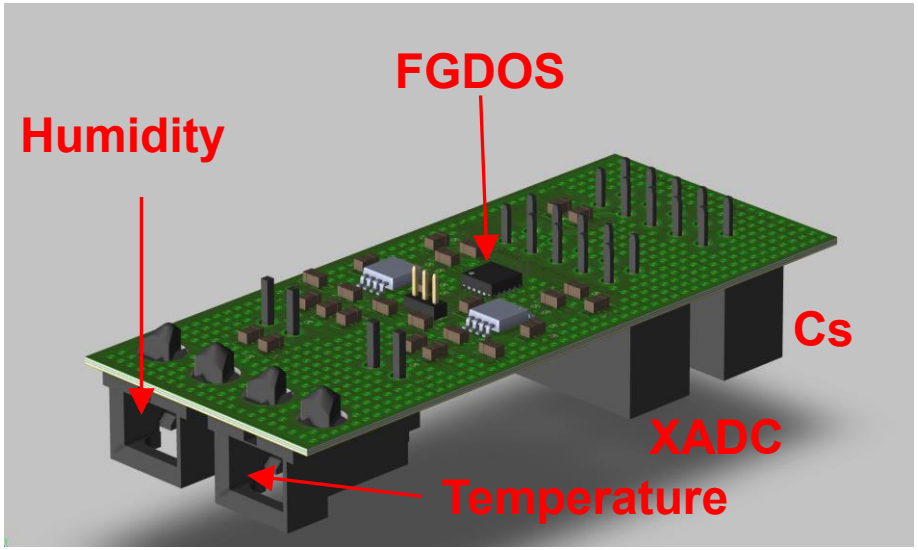
- DCS and remote programming of the upgraded readout electronics + ILANA control
- 55 x TileCoM v1.3 PCBs to be received this week (MOQ)
  - 10 layers, 1 mm thickness
  - 6.7 cm x 3 cm with 251 components.
  - Minor changes mainly in the layout
    - Improvements in the analog ground layout
    - Improved paste mask land patterns for QFN components
    - Added some extra capacitors at Vin
    - Location of some capacitors
    - DC caps for high-speed ports
- Order for assembling 4 prototypes in Rompal done
- Components for 4 prototypes received at CERN
  - To be shipped this week to Rompal



TileCoM v1.3

HW: Front-end Environment Sensors

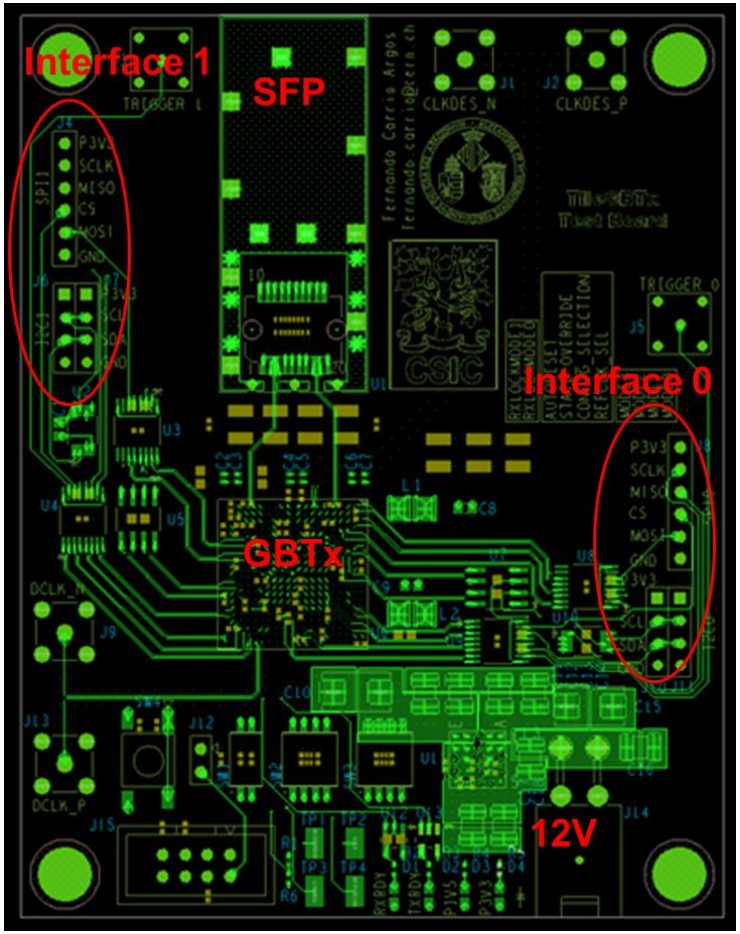
- Sensing environment conditions inside the TileCal modules using the XADC from the DaugtherBoard - 1 per SD
- Overview:
  - 4 layers, 22 x 52 mm
  - Analog signal conditioning for temperature (PT100) and humidity (polymer) using INA333
  - Sealicon FGDOS for TID + Dickson bridge to charge it (20V)
    - 0-10 Gy / 0-50 Gy and 8-bit resolution
- 4 boards to be delivered by today at CERN - Paid by Technical Coordination
- If fully working will be installed in the Demonstrator in January



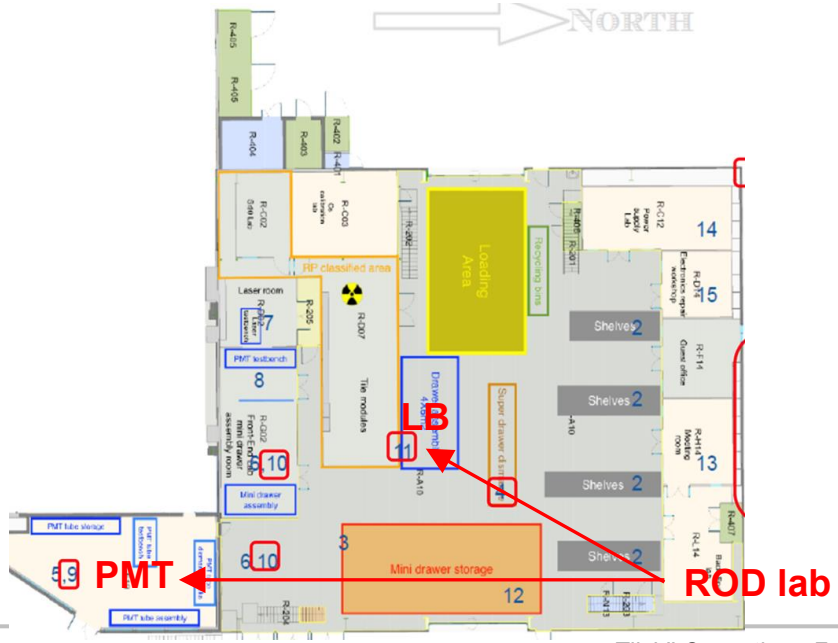
TileSensor board v1.0

HW: GPIO over fiber

- Remote control of the HV and LED drivers from CPM over GBT protocol for the PMT block and long barrel test benches
- General overview: 4 layers, 80 x 102 mm
  - 1 GBTx chip 4.8 Gbps
  - Differential to single ended buffers and I2C buffers
  - 2 × SPI interfaces and 2 × I2C interfaces
  - LED trigger with LEMO
- 2 boards being assembled at IFIC
  - Paid with the CERN Prometeo budget

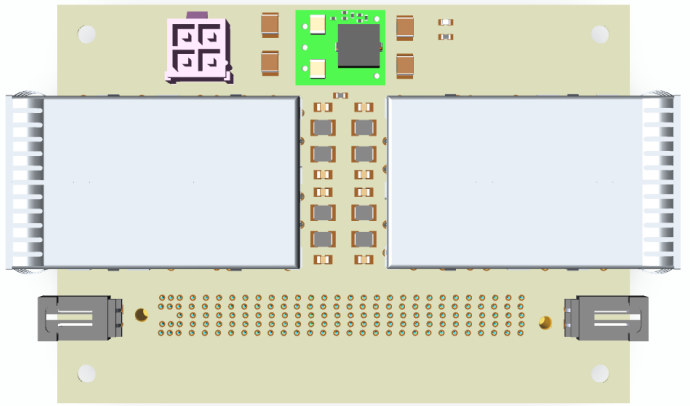


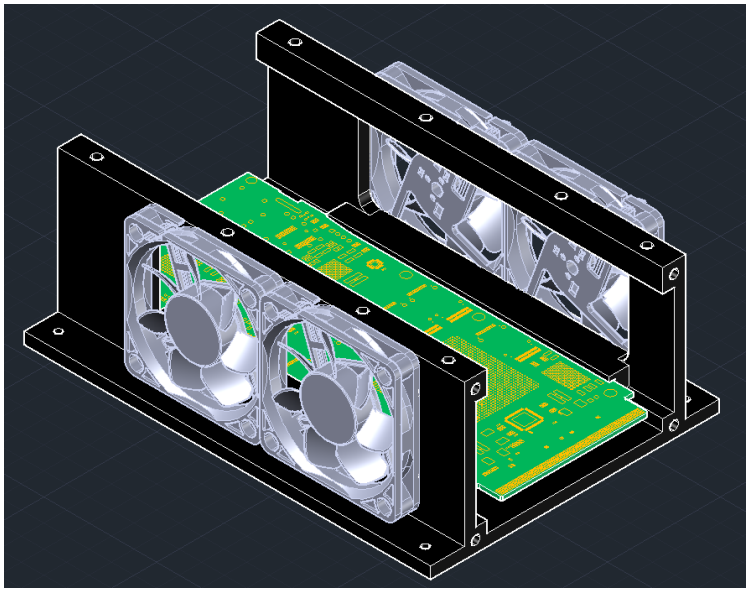
TileGBTx board v2.0

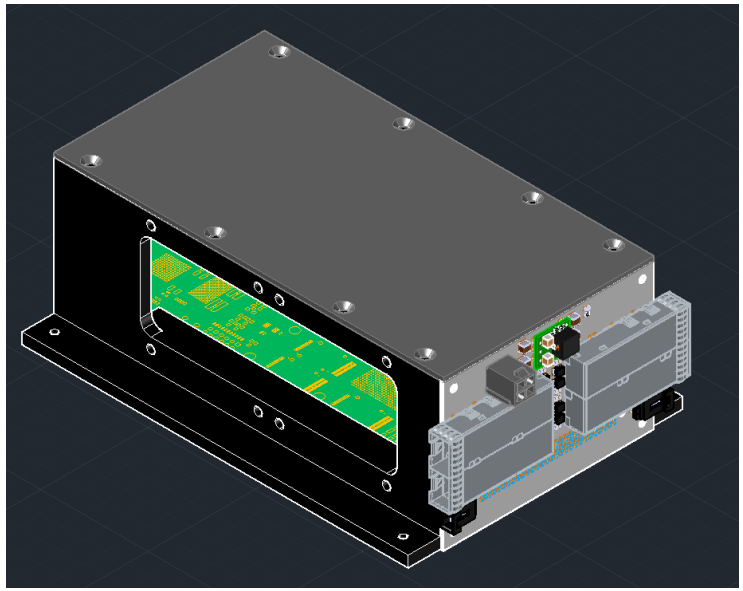


HW: Backplane and support for portable test benches

- Plastic support for on-table test benches + Ethernet backplane
- Support with in-buit guidelines:
  - 145 x 70 x 100 mm
  - 4 x 60 mm heatsinks with 12V connectors
  - To be produced at CERN (ideasquare)
- Backplane
  - 4 SFP modules connected to the KU GTH
  - 1x 12V input power connector (4 pin)
  - 2 x 12V output connector for fans (2 pin)

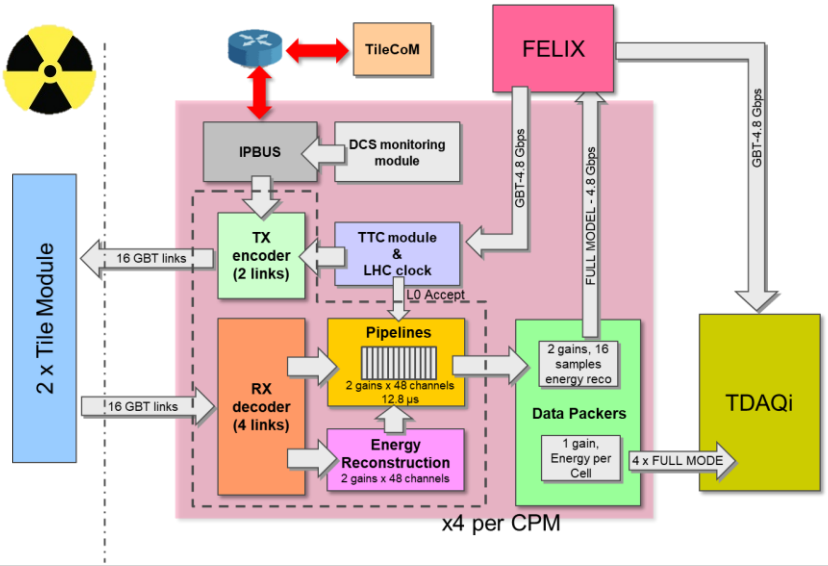


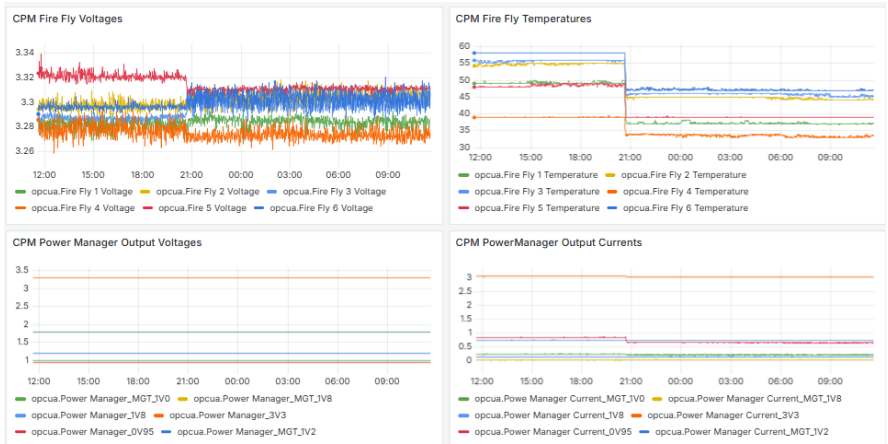




FW: Compact Processing Module

- Almost all functionalities in place and validated
  - 2 link @ 4.8 Gbps to FELIX: TTC and Readout + 1 GbE for IPbus communication
    - LTI - FULL MODE (9.6 Gbps) being developed
      - To be tested next week @ CERN
  - 32 x links to DaughterBoards (4.8/9.6Gbps)
  - 4 x links @ 9.6 Gbps to TDAQi
  - New block to detect corruption in the data samples (stuck bits, spikes, etc)
    - Being implemented by Thiago as part of his QT
  - Firmware updates for the DS readings -> Brenton as part of his Master thesis
    - Deployment in P1 in December: Ipbus -> IS -> pBeast
  - Several firmware updates in mind

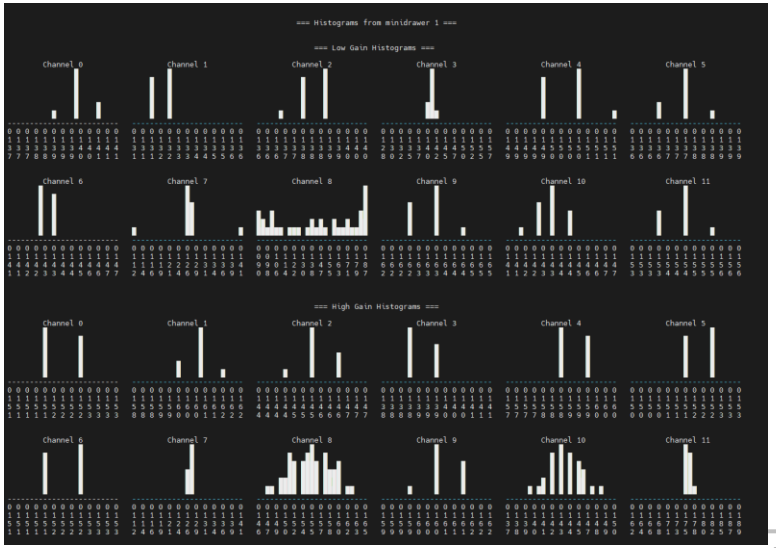




SW: Compact Processing Module

- Python libraries using official uHAL with high-level functions are completed
- TROOPER libraries: https://gitlab.cern.ch/fcarrio/tropper-libraries/-/tree/master
  - C++ libraries + using pybind11 → allows consistent usage of libs when using Python
  - Very simple structure:
    - Core: very low-level functions (write, reads, helper functions)
    - Drivers: low-level functions to control specific registers: TTC, FELIX config, pipelines
    - Applications: high-level applications, e.g. link monitoring
- Prometeo-like debugging tools, ASCII mode for Demo

  CIS linear, CIS pulse, ADC linear, Pedestals, etc
  - Generation of a json file with the raw data and analysis results
    - Working with Pavle and Aaron




```
(venv) [fcarrio@lxplus939]/eos/home-f/fcarrio/TestBeam/prometeo% python Main.py --debug --mode ADClinear
Using connection file from argument: addresses/connections.xml
Reusing existing ipbus instance for device: cpm175
Reusing existing ipbus instance for device: cpm175
CH00:   225   502   785  1068  1352  1631  1914  2197  2480  2761  3043  3324  3605  3887  4095  4095
CH01:   249   523   801  1080  1359  1634  1914  2194  2473  2750  3027  3304  3583  3860  4095  4095
CH02:   243   519   800  1082  1364  1640  1923  2205  2487  2767  3048  3326  3607  3887  4095  4095
CH03:   254   528   808  1088  1368  1644  1924  2204  2484  2763  3040  3318  3597  3876  4095  4095
CH04:   243   519   799  1080  1359  1638  1919  2199  2481  2760  3037  3317  3598  3878  4095  4095
CH05:   249   525   805  1085  1365  1641  1921  2202  2482  2761  3038  3316  3596  3875  4095  4095
CH06:   255   532   813  1095  1377  1656  1938  2220  2502  2782  3061  3341  3623  3903  4095  4095
CH07:   244   520   799  1082  1363  1641  1922  2203  2485  2765  3044  3323  3603  3883  4095  4095
CH08:   231   510   793  1078  1363  1643  1928  2212  2497  2779  3061  3343  3627  3910  4095  4095
CH09:   256   533   814  1095  1376  1652  1934  2215  2497  2775  3055  3333  3614  3893  4095  4095
CH10:   251   528   807  1088  1368  1644  1925  2206  2486  2764  3042  3321  3601  3881  4095  4095
CH11:   230   509   791  1074  1357  1635  1918  2201  2484  2765  3046  3325  3609  3891  4095  4095
ipbus instance for device destroyed.
(venv) [fcarrio@lxplus939]/eos/home-f/fcarrio/TestBeam/prometeo%
```

Prometeo version with pyTROOPER libraries

Other duties

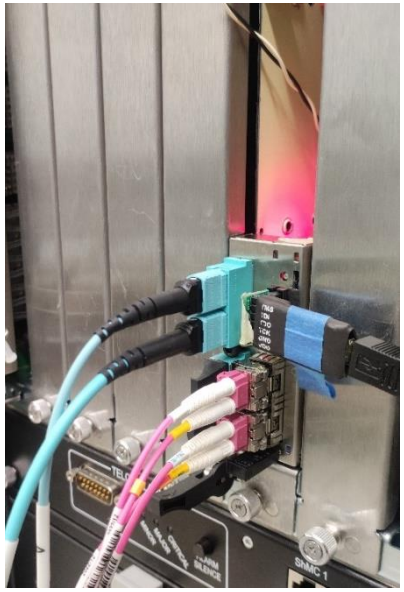
- Other duties:
  - Operation of the demonstrator modules and a few collaboration on the SW development
  - Several meetings with TC and P2 management for coordination activities during LS3 such as rack layout, fiber planning and ATCN

BACK-UP Slides

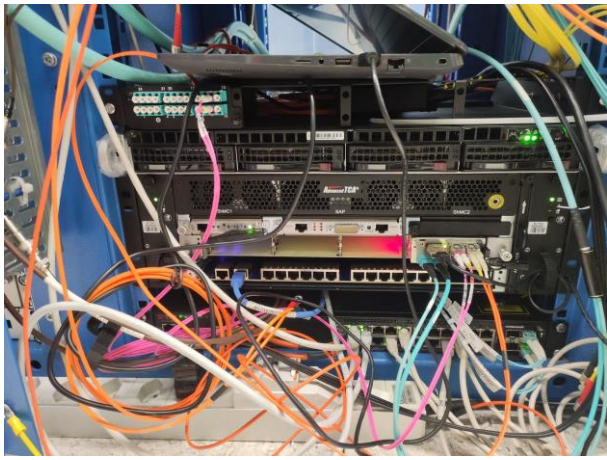
Compact Processing Module - Firmware

- 1 CPM installed during the last testbeam
  - Operating two modules: Extended and Long Barrel
  - Using "test-beam" data format GBT with widebus and CRC
- 1 CPM installed in P1 for the Demonstrator
  - Operating one module
  - Using the data format for phase-II: GBT with FEC
    - As defined in the specifications

- Firmware well advanced
  - Added lots of new features
    - Remote programming of DB and CPM
      - Golden + Operation image
    - Final data format implemented (only for Demonstrator)
    - Spy memories for advanced debugging (8000 consecutive samples per channel)
    - Optimized pipeline memories
      - One pipeline per minidrawer and not per channel
    - Phase monitoring link system for the uplinks
    - Eye diagrams through ipbus

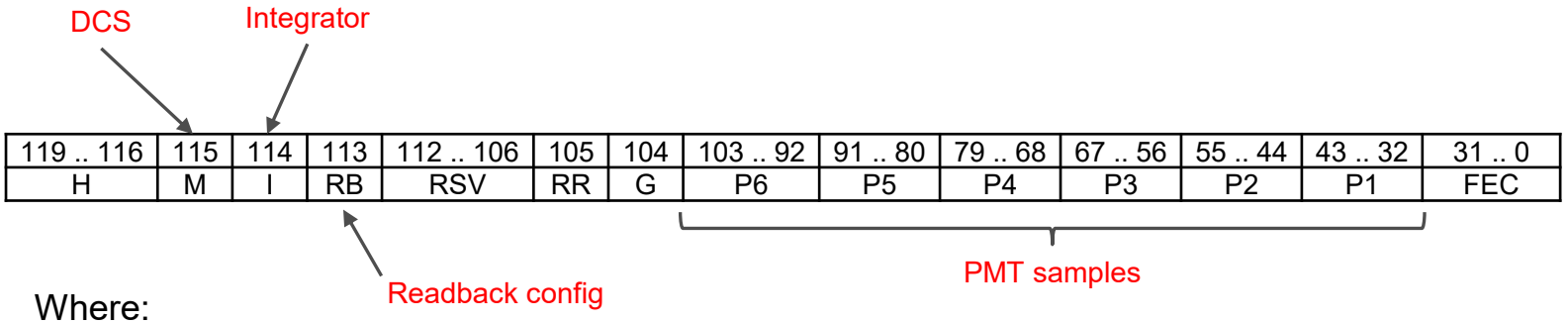


CPM at the TB area



CPM at USA15

Data formats - Uplink



Where:

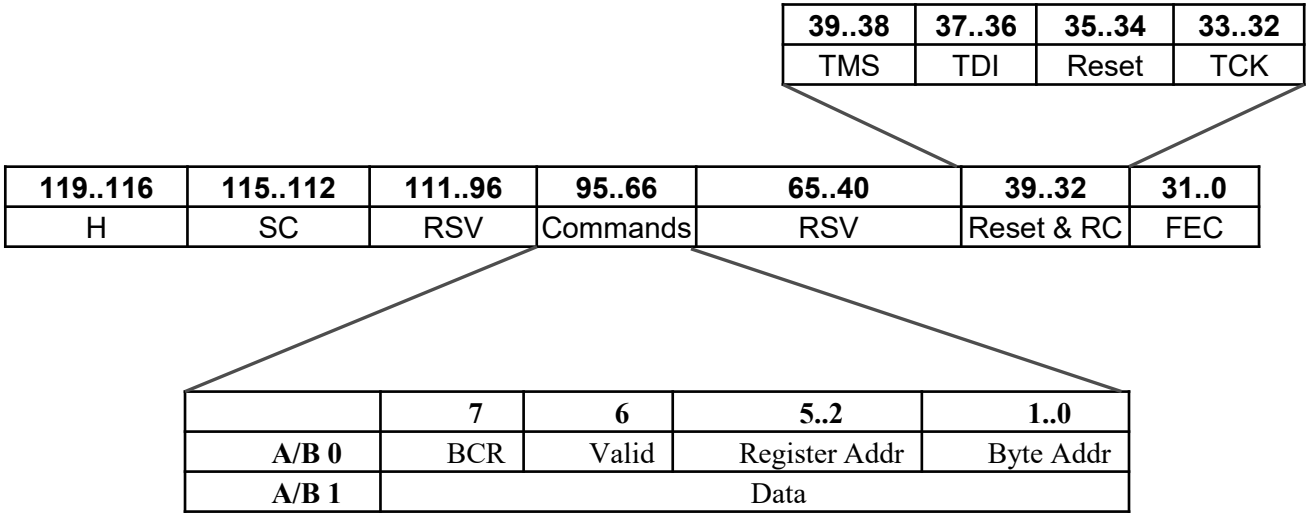
- H: GBT header.
- M: DCS & monitoring data.
- I: Integrator data.
- RB. Read back commands.
- RSV: Reserved bits.
- RR: Reset Request from the Daughterboard.
- G: FEB gain. 0 is low gain and 1 high gain.
- Px: PMT samples.
- FEC: Forward Error Correction.

BW assigned	Assigned bits	Description/ max requirement
80 Mbps	4	GBT header → Used as returned BCR
80 Mbps	1	DCS monitoring data. It includes a maximum of 100 sensors * 10 Hz * 32-bit words for monitoring of temperature sensors, voltages and currents.
80 Mbps	1	Integrator data. It includes a maximum of 6 PMTs * 200 Hz * 32-bit words
80 Mbps	1	Read back of MB and DB registers
80 Mbps	1	Reset Request from the DB
80 Mbps	1	High and Low gain identifier
5.760 Gbps	72	PMT readout data
2.56 Gbps	32	Forward Error Correction

Detector readout path Downlink & data format

- 1 link per minidrawer side connected to a GBTx chip
  - LHC clock recovery for the ADC sampling clock and synchronous communication
  - Trigger, Timing and Control data
  - Other front-end configuration commands (resets, ADC configuration, etc)

- As uplinks, downlinks data is protected with Forward Error Correction code



Expert Weeks - latency measurements

- Injecting a CIS pulse and measuring the arrival time in the different parts of the subsytem.
  - DBv6.4, CPM, carrier and TDAQi + 80 meter fibers and internal fibers
- Joint effort of Stockholm, Valencia and Heidelberg https://edms.cern.ch/document/2417233/3
- Preliminary we are still inside the latency budget (1.425 us / 1.7 us) but very tight
  - 25 ns not included from ToF+optics
  - Still need ~4BC for CPM reco, ~4/5 BC for TDAQi calculations and trasmission, some additional logic in the DB: ~ 1 BC
  - 1.125 us + 25 ns + 10 BC = **1.400 us** *Fiber lengths to Trigger not included (up to 4 BC)*

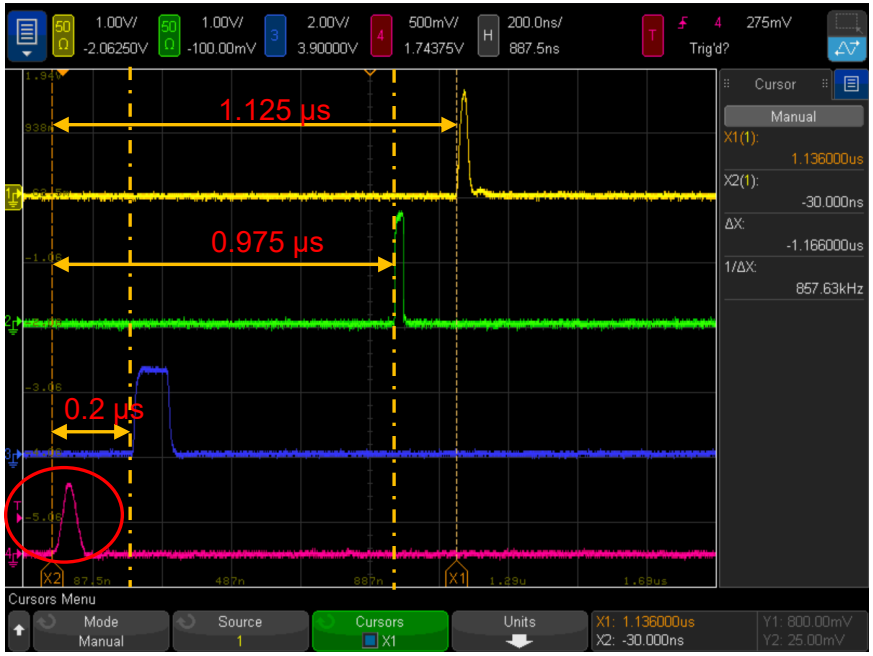
CBE MPV

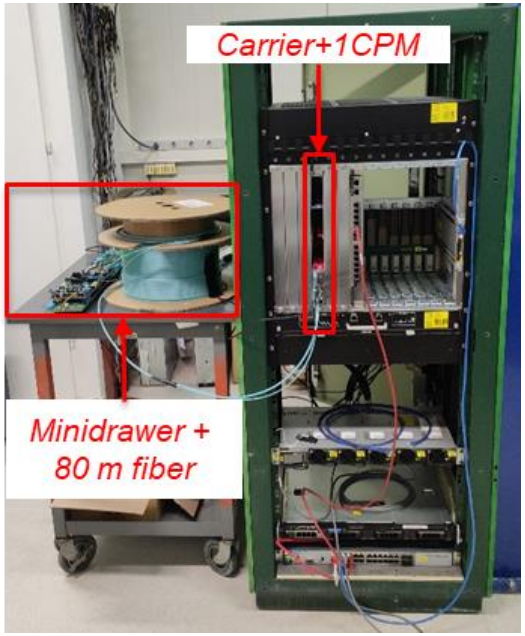
TDAQi
After decoding

CPM
After receiving the full pulse (7 samples)

DaughterBoard
Arrival of the pulse

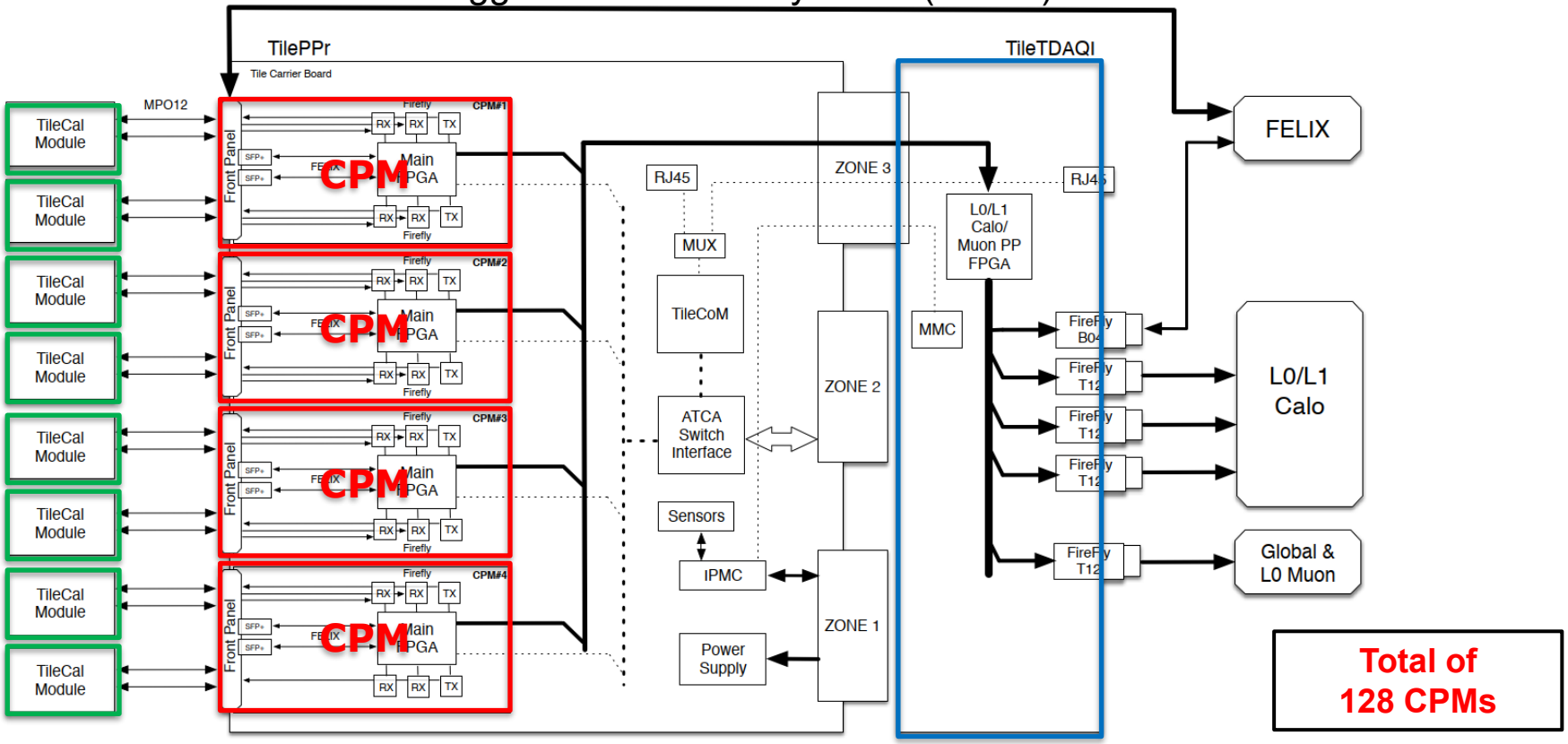
CIS pulse





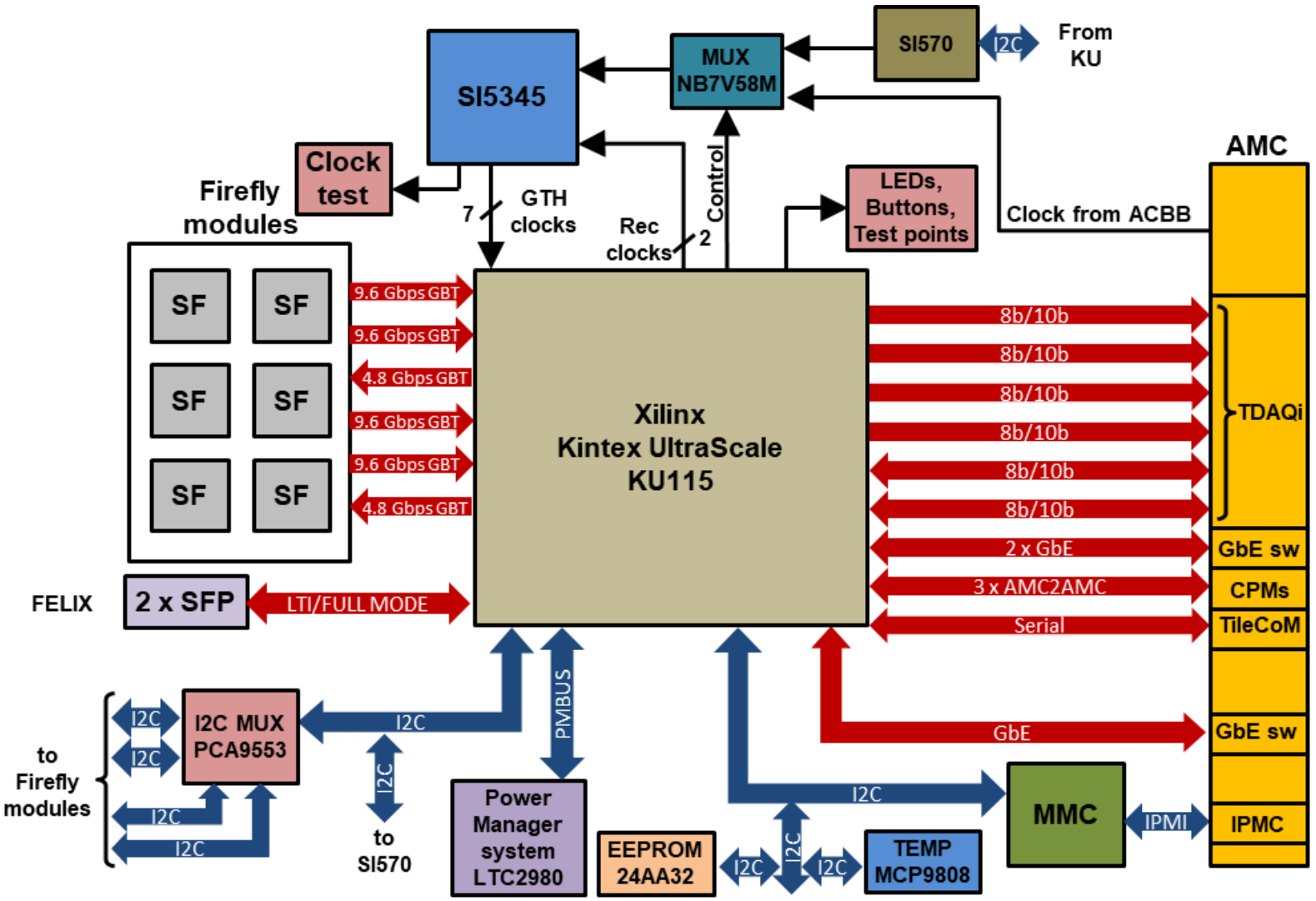
HL-LHC off-detector electronics

- **The Tile PreProcessor is the core element of the off-detector electronics**
  - Data processing and handling from on-detector electronics
  - Provides clocks and configuration for the TileCal modules
  - Interface with the ATLAS trigger and readout systems (FELIX)



- **32 TilePPr** boards in 4 ATCA shelves**:** ATCA carrier + **4 Compact Processing Modules**
- **32 TileTDAQ-I:** Interfaces with L0Calo, Global and L0Muon

Block Diagram & Interconnections



Thermal test setup

- Several ATCA shelfs availlable for testing
  - Communication tests with Global - to be done
  - Complete infrastructure for thermal tests
- Thermal tests performed during the second week of December at b2175 with excellent results
  - Tested a full PreProcessor ATCA blade
    - 4 × CPM, Carrier, TDAQi
- Setup conditions
  - All FPGAs loaded with IBERT reproducing the number of links and speeds for Phase-II
  - Temperature, V/I data was published online in InfluxDB and presented in Grafana
  - Remaining front slots equipped with ASICS load boards
  - Back slots equipped with fillersASIS load boards set to 400W, and fans to maximum (level 15) → Emulating PPrs at max power consumption
- Tests done for each possible slot configuration
  - Using ATCA fillers for empty slots

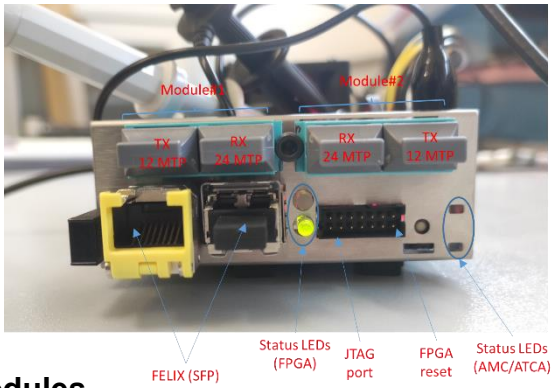
ATCA thermal test bench at b2175

	Physical slot													
	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Option 1	PPr 1	Empty	PPr 2	PPr 3	Empty	PPr 4	Interface							
Option 2	PPr 1	Empty	PPr 2	Empty	PPr 3	PPr 4	Interface							
Option 3	PPr 1	PPr 2	Empty	PPr 3	Empty	PPr 4	Interface							

Possible PPr positions in ATCA shelf

Compact Processing Module - Overview

- **Single AMC board** with full-size form factor
  - **32 RX channels** through 4 Samtec Firefly
  - **16 TX channels** through 2 Samtec Firefly
  - **Up to 14 channels** through AMC connector
  - **Kintex UltraScale: XCKU115-2FLVA1517E**

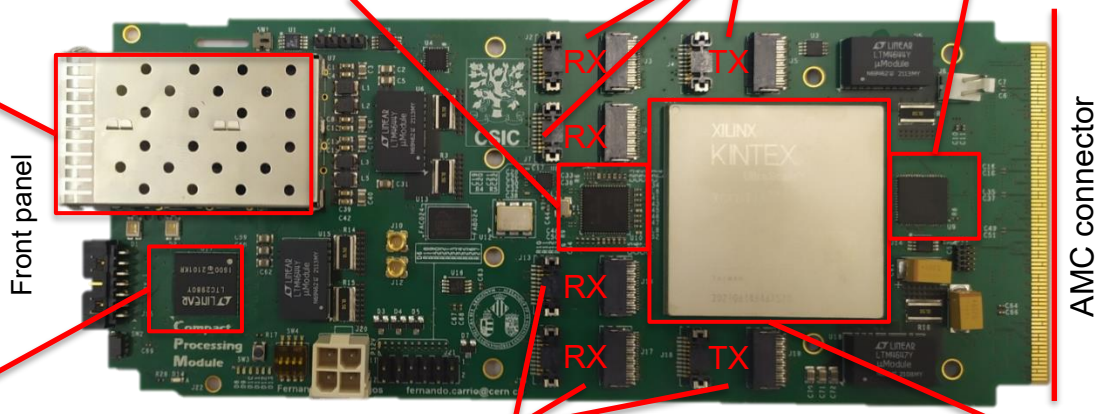


2 x SFP
FELIX interface
Clock +TTC data
L0-triggered data

Silicon Labs si5345
Clock generator
Jitter cleaning

6 x Samtec Firefly optical modules
4 RX+2TX optical links up to 14 Gbps
MPO connectors ending

MMC
Power managment



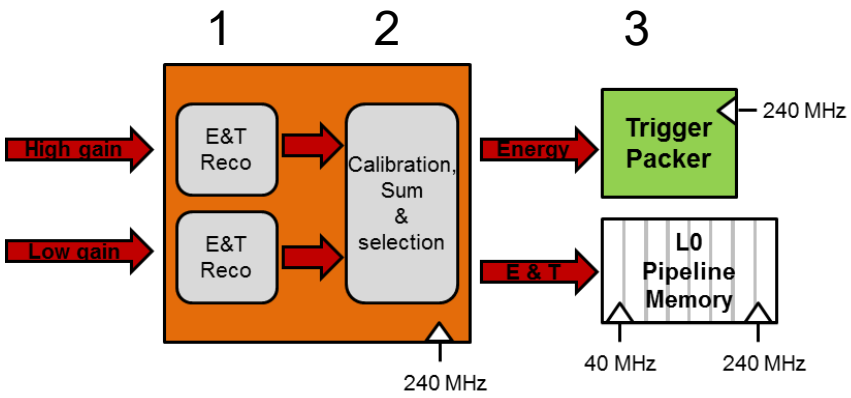
Analog LTC2980
Power monitoring
PMBus interface

Samtec Firefly

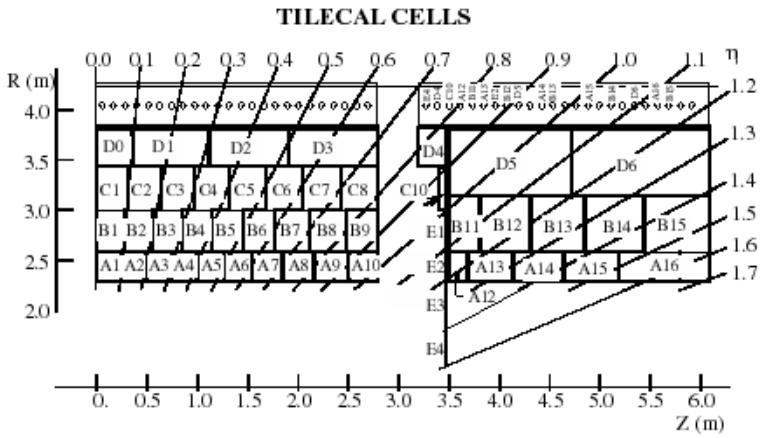
Kintex UltraScale KU115
Acquisition
Data buffering
Processing

Trigger real-time path

- CPMs provide reconstructed energy (and time) per cell to the TDAQi for every Bunch crossing
  - Cells have a granularity of ΔηxΔφ=0.1x0.1 for A/B/C cells and 0.2x0.1 for D cells
  - 45 channels in Long Barrels, 32 channels in Extended Barrels
    - 4 channels from EBs are E-cells which are not sent to the trigger system
- Energy&Time Reconstruction block
  - 1. Reconstruction of energy and time per PMT and gain: Up to 4 processing reco blocks per PMT
  - 2. Energies are selected (e.g. high gain if not saturated), summed into cells and then calibrated
  - 3. Results are transmitted to the L0-pipeline memories and to the Trigger Packer



E&T Reconstruction block



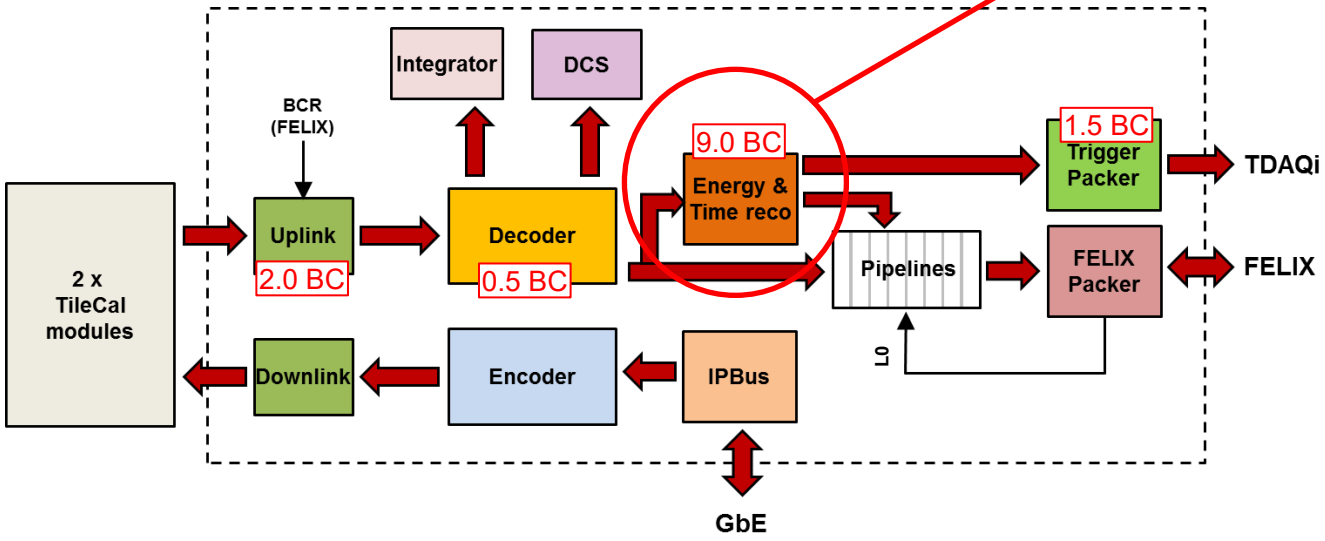
Latency of the trigger path

- Maximum latency estimated for the real-time trigger path is 325 ns
  - Still some latency contingency can be taken from the on-detector electronics
  - Considering the MPV values from the ATLAS TileCal TDR and Phase-II latency document

Firmware block	Latency	
Uplink	50 ns	2.0 BC
Data Decoder	12.5 ns	0.5 BC
Energy Reconstruction + sample delay	225.0 ns	9.0 BC
Trigger Packer	12.5 ns	0.5 BC
Trigger interface	25 ns	1.0 BC
Total	**325 ns**	**13 BC**

Summary of the trigger latency (CPM)

Preliminary and optimistic value
Expert Week planned in Dec'24 to understand this number



Block diagram of the Kintex UltraScale firmware

Exploring feasibility towards the Final Design Review

- Several 7-input models implemented within the full firmware (2 x 77 channels), and connected to the TDAQi interface. Challenges observed:
  - **Scalability:** 154 NN might be needed if 2 gains are used. Even if each model consumes a small franction of resources, they can "eat" all resources. As rough reference:
    - E.g. 7-7-7-1 and 9-9-1 would use above 32% of LUT, and 9-9-9-1 would use 50%
    - **Understood that LUT and FF are more a limiting factor than the DSP blocks (~72DSP/channel)**
  - **Timing**: even at 280 MHz many architectures failed timing! → Others took about 8 hours to compile
    - Signal congestion in many areas → pipeling at the cost of extra latency
  - **Clock Domain Crossing** and **synchronization**: passing data from 40/80/280MHz
    - Clock congestion makes it even more difficult → clock arch. optimization ongoing

	MLP 7–1	MLP 7–7–1	MLP 7–7–7–1	MLP 9–1	MLP 9–9–1	MLP 9–9–9–1
Inputs (samples)	7	7	7	9	9	9
Neurons per layer	7	7	7	9	9	9
Hidden layers	0	1	2	0	1	2
LUT	521	942	1363	817	1507	2197
FF	168	171	174	170	174	175
DSP	8	15	22	10	19	28
Parameters	64	120	176	100	190	280
Freq. max	280 MHz	280 MHz	280 MHz	360 MHz	360 MHz	360 MHz
Latency	3+3 BC	3+4 BC	3+5 BC	4+3 BC	4+4 BC	4+5 BC

Latencies not optimized, reduced by increasing the frequency (if timing allows)

Main FPGA - Overview

- Xilinx Kintex UltraScale KU115
  - XCKU115-**2**FLVA1517E
    - 1.5 M logic cells, 48 GTH transceivers, 5520 DSP blocks, 75.9 Mb
    - 1517 pins → A1517 package (35 mm x 35 mm)
  - Choosen speed grade -2, (current prototypes with -1)
    - GTH max data rate of 16.375 Gbps
    - DSP operating up to 661 (594) MHz (when all internal registers are used → extra latency)
    - Clock buffers & MMCM and PLL up to 725 (630) MHz

Resource	Available
LUT	663,360
LUTRAM	293,760
FF	1,326,720
BRAM	2,160
DSP	5,520
IO	624
GT	48
BUFG	1,248
MMCM	24
PLL	48

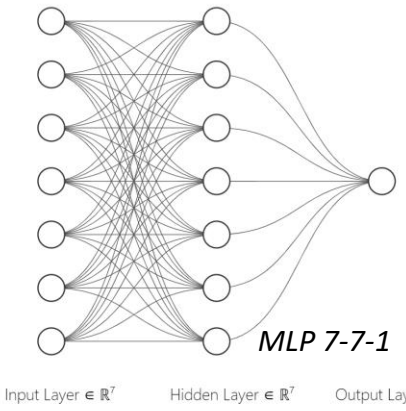
Resources of the Kintex UltraScale 115 with A1517 package

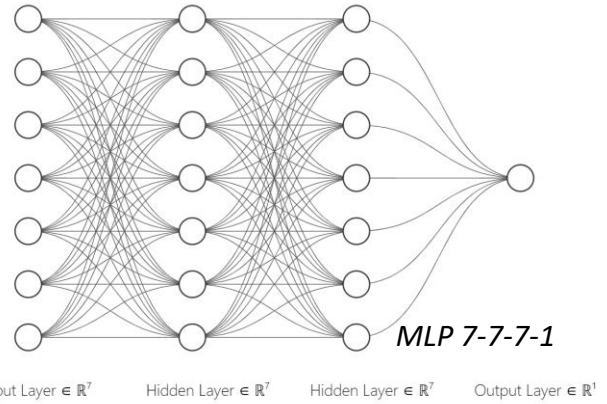
	KU025[1]	KU035	KU040	KU060	KU085	KU095	KU115
System Logic Cells	318,150	444,343	530,250	725,550	1,088,325	1,176,000	1,451,100
CLB Flip-Flops	290,880	406,256	484,800	663,360	995,040	1,075,200	1,326,720
CLB LUTs	145,440	203,128	242,400	331,680	497,520	537,600	663,360
Maximum Distributed RAM (Mb)	4.1	5.9	7.0	9.1	13.4	4.7	18.3
Block RAM Blocks	360	540	600	1,080	1,620	1,680	2,160
Block RAM (Mb)	12.7	19.0	21.1	38.0	56.9	59.1	75.9
CMTs (1 MMCM, 2 PLLs)	6	10	10	12	22	16	24
I/O DLLs	24	40	40	48	56	64	64
Maximum HP I/Os[2]	208	416	416	520	572	650	676
Maximum HR I/Os[3]	104	104	104	104	104	52	156
DSP Slices	1,152	1,700	1,920	2,760	4,100	768	5,520
System Monitor	1	1	1	1	2	1	2
PCIe Gen3 x8	1	2	3	3	4	4	6
150G Interlaken	0	0	0	0	0	2	0
100G Ethernet	0	0	0	0	0	2	0
GTH 16.3Gb/s Transceivers[4]	12	16	20	32	56	32	64
GTY 16.3Gb/s Transceivers[5]	0	0	0	0	0	32	0
Transceiver Fractional PLLs	0	0	0	0	0	16	0

Kintex UltraScale FPGA Family overview

Exploring feasibility towards the Final Design Review

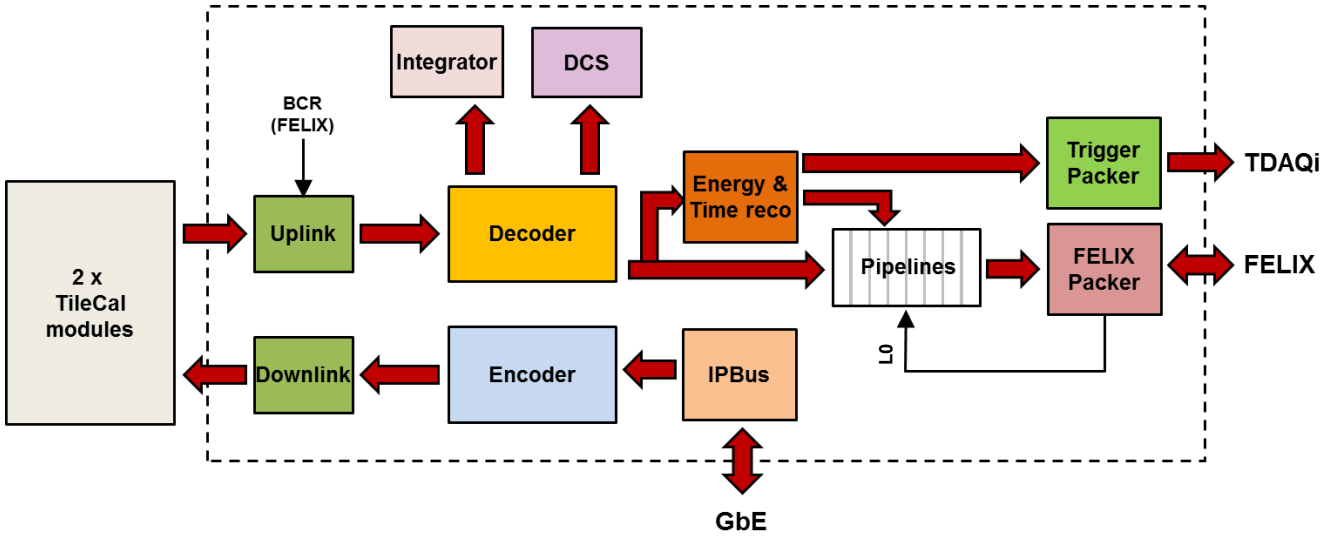
- Preliminary studies to evaluate the feasibility in terms of resource usage and latency towards the Final Design Review (22/23 Oct)
- Reproducing a realistic scenario case for HL-LHC
  - ~~**Toy example**: a basic Multi Layer Perceptron + ReLU activation + control FSM~~
    - Simplest NN model candidate
    - 18-bit input, up to 48-bit output, 18-bit weights, 32-bit bias → Configurable precision
    - Processing data interval of 1 BC → new input sample for every BC
  - Hard-IP DSP blocks building different architectures: ***1 DSP per neuron (perceptron)***
    - 7-1 (8 neurons), 7-7-1 (15 neurons), … , up to 9-9-9-1 (28 neurons)
  - Latencies between 6 and 9 BCs including the 3(4) BCs for the central peak sample
  - Added a few IPbus registers per MLP for loading the weights and bias + control
  - Code verified and validated with stand-alone VHDL test benches + patterns





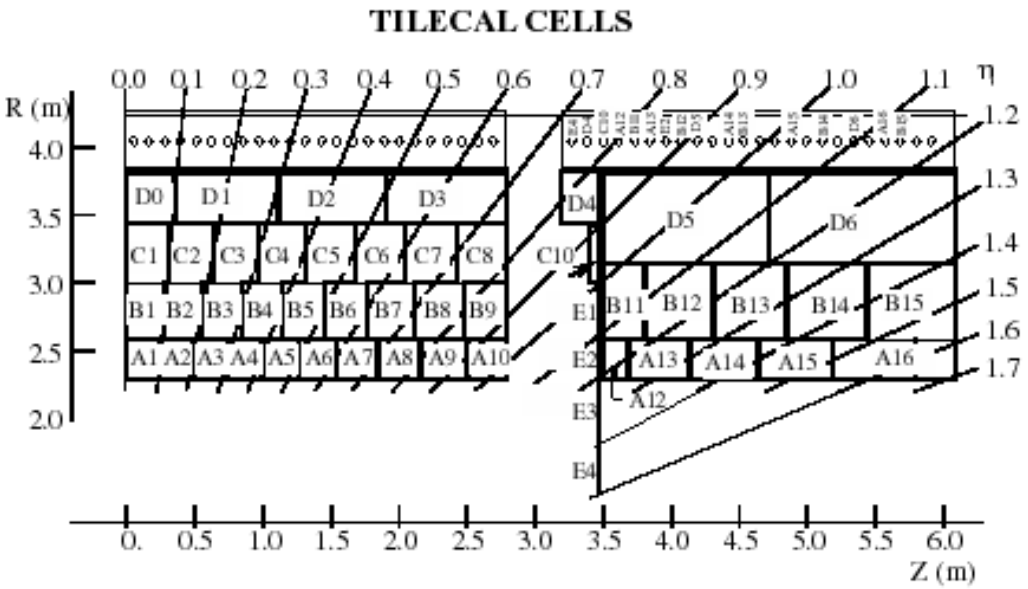
Firmware requirements

- Main firmware requirements
  - Readout and operation of **two TileCal modules**
    - 28 GBT uplinks@9.6 Gbps, 14 GBT downlinks@4.8 Gbps
  - FELIX interface: compatible with L0 trigger architectures
    - Two LTI frame / Full-Mode links at 9.6 Gbps
    - Store detector data in pipeline memories up to 10 μs
    - Event transmission a maximum trigger rate of 1 MHz
  - Energy & time reconstruction
    - Online time and energy reconstruction of 77 channels x 2 gains → **154 reco algorithm blocks**
    - 4 TX links@9.6 Gbps using 8b/10b encoding (expandable to 7 links)
  - GbE interfaces for configuration and monitoring



Block diagram of the Kintex UltraScale firmware

TileCal Trigger Towers



BARREL			
Eta	**PMTs by cell**	**PMT Positions**	**Adder Position**
0.0-0.1	A1R A1L BC1R BC1L D0R	5 2 3 4 **1**	4
0.1-0.2	A2R A2L BC2R BC2L D1L	9 6 7 8 **14**	7
0.2-0.3	A3R A3L BC3R BC3L D1R	11 10 13 12 **15**	10
0.3-0.4	A4R A4L BC4R BC4L D2L	19 16 17 18 **26**	15
0.4-0.5	A5R A5L BC5R BC5L D2R	21 20 23 22 **27**	21
0.5-0.6	A6R A6L BC6R BC6L D3L	25 24 29 30 **40**	28
0.6-0.7	A7R A7L BC7R BC7L D3R	31 28 35 36 **43**	31
0.7-0.8	A8R A8L BC8R BC8L	37 34 41 42	34
0.8-1.0	A9R A9L B9R B9L A10R A10L	39 38 45 46 47 48	42

EXTENDED BARREL			
Eta	**PMTs by cell**	**PMT Positions**	**Adder Position**
0.8-1.0	C10R C10L D4R D4L D5R	5 6 3 4 **17**	7
1.0-1.1	B11R B11L D5L	9 10 **18**	10
1.1-1.2	A12R A12L B12R B12L D6R	7 8 15 16 **37**	21
1.2-1.3	A13R A13L B13R B13L D6L	11 12 23 24 **38**	15
1.3-1.4	A14R A14L B14R B14L	21 22 33 34	28
1.4-1.6	A15R A15L B15R B15L A16R A16L	29 30 43 44 41 42	34
Gap/Crack	E1 E2 E3 E4	13 14 **1** 2	

Resource occupancy estimation from PDR

- **Main FPGA** resource usage estimation based on PPr Demonstrator fw

	PPr Demonstrator Virtex 7 485T			CPM KU115		
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Used**	**Available**	**Utilization**
Number of Slice Registers	152,696	607,200	25%	305,392	1,326,720	23.02%
Number of Slice LUTs	154,811	303,600	50%	309,622	663,360	46.67%
Number of RAMB36E1	107	1,030	10%	-	2,160	-
Number of RAMB18E1	741	2,060	35%	1004	4,320	23.25%
Number of MMCMs	4	14	28%	6	24	25.00%
Number of PLLs	2	14	14%	4	24	16.67%
Number of Transceivers	19 + 4	56	41%	48	48	100%
DSP slices	1152	2,800	41%	2,304	5,520	41.73%

FPGA logic:
State machines, de/multiplexer, encoder/decoders, etc

RAM memory:
Pipeline buffers and monitoring
PPr Demo fw is 12.8 us

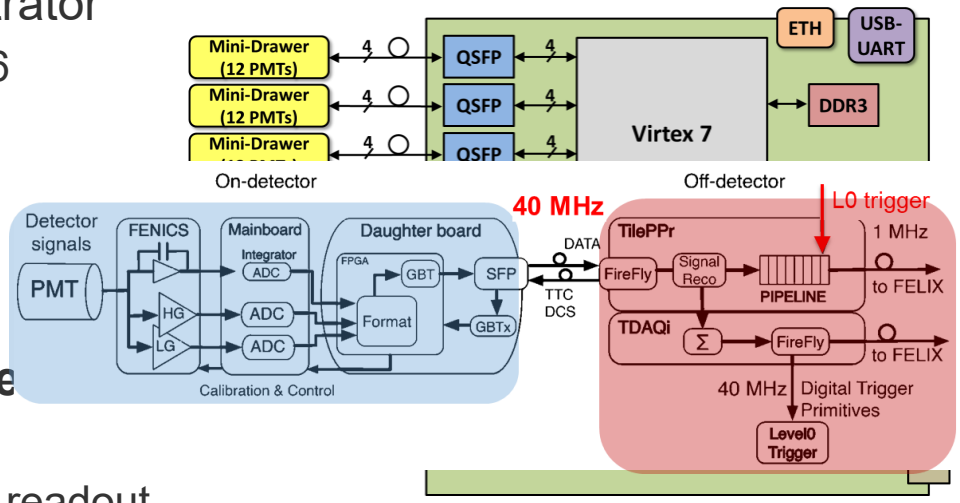
Clocking circuitry

Transceivers:
DaughterBoard, TDAQ-I, FELIX, Ethernet, spares

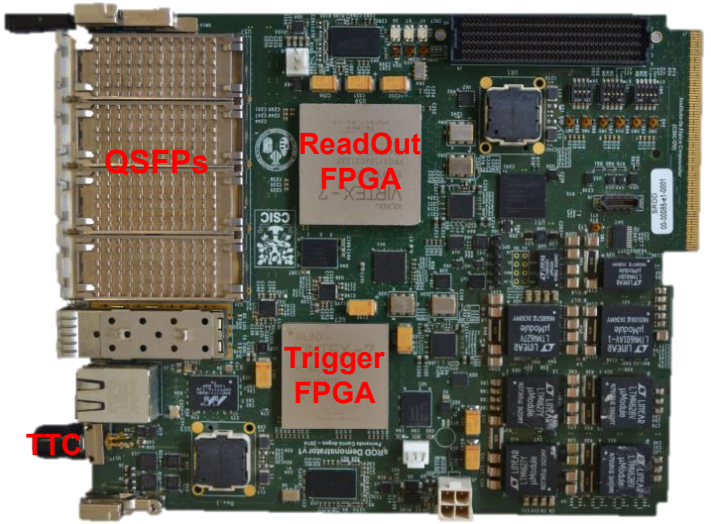
- Low resource occupation for **Control FPGA** (Artix 7)
  - ~11% of Slice Registers
  - ~3.5 % of Slice LUT
  - 50% of 36 kb BRAMs

Previous R&D - PPr Demonstrator

- **Fully functional prototype** for Demonstrator
  - 8 boards produced between 2015 and 2016
  - Double mid-size AMC board
  - Xilinx Virtex 7 (48 GTX), Kintex 7 (28 GTX)
  - 4 QSFP optical modules
  - TI CDCE62005 jitter cleaner + ADN2814
- **1/2 of the Compact Processing Module**
  - Operates 1 TileCal module → 160 Gbps
  - Interfaces with legacy and Phase II ATLAS readout systems (ROD, FELIX)
- **Extensively tested and validated**
  - Several test beam campaigns between 2016 and 2018
- **Optimal Filtering algorithm** for **online** energy reconstruction implemented in FPGA
  - R&D using **Neural Networks** with promising results in high pile-up conditions
- CPM firmware design will be **largely based on this system**



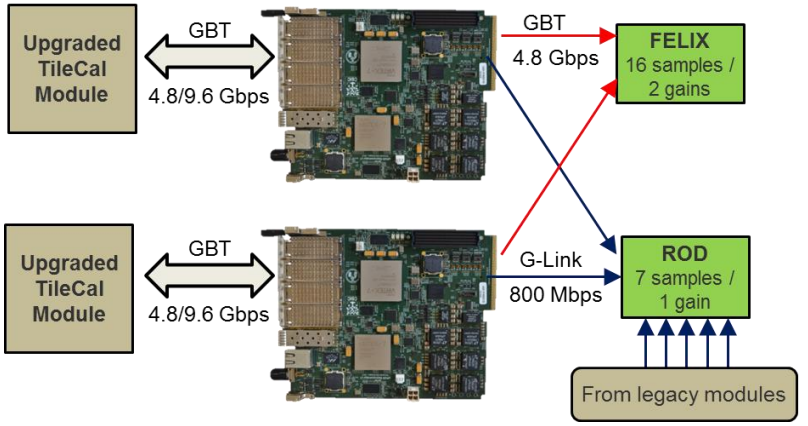
Block diagram of the PPr Demo



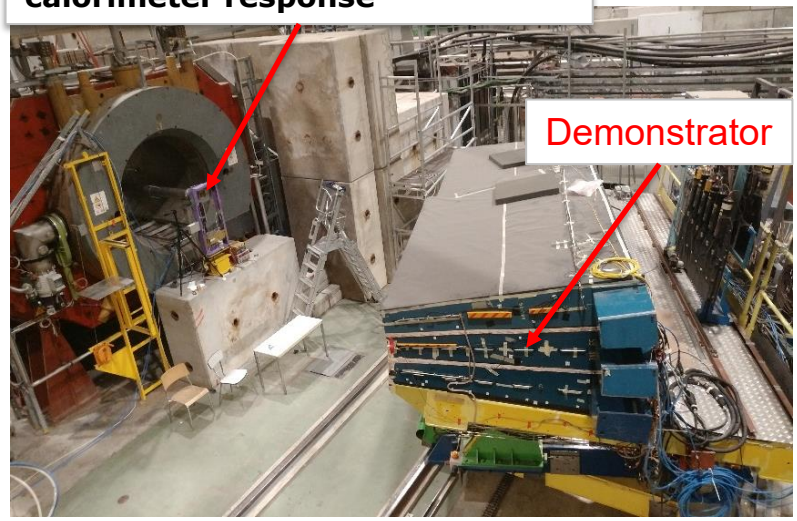
PPr Demonstrator

Previous R&D - Test Beam setup

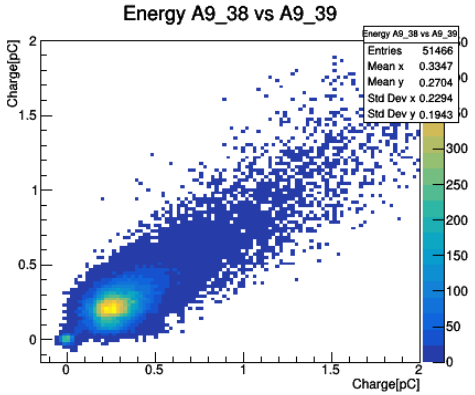
- Located at the **S**uper **P**roton **S**ynchrotron (SPS) North Area on the H8 beam line
  - **7 test beam campaigns** between 2015 and 2018
- Detector modules equipped with upgraded and legacy electronics for performance comparison
- **Fully integrated** with the ATLAS TDAQ software and DCS system
  - Front-end electronics configuration
  - Physics, calibration and laser runs
  - HV and LV control/monitoring
  - Data taking through FELIX / legacy system

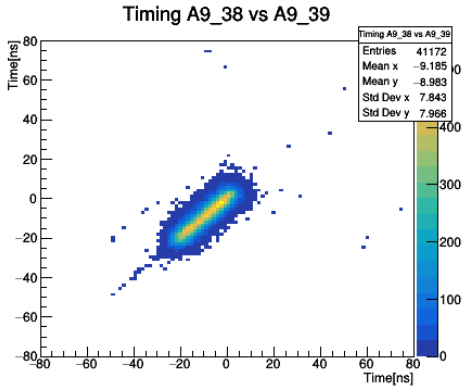


Beams of Hadrons, Electrons and Muons were used to study the calorimeter response



Test beam setup at H8 line

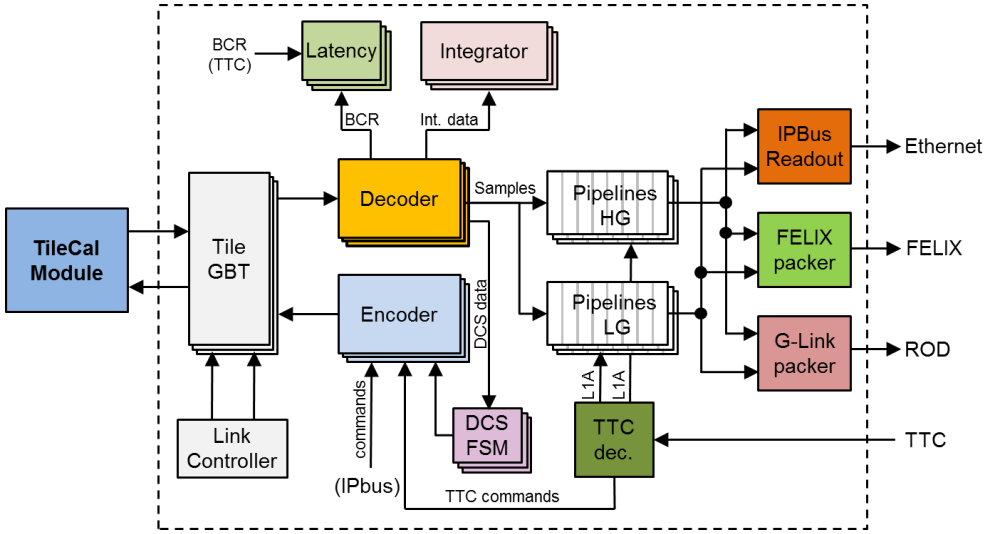




- **Demonstrator module inserted into ATLAS experiment last July**

Previous R&D - Firmware

- 16 GBT links with on-detector electronics
  - 9.6 Gbps for uplinks, 4.8 Gbps for downlinks
- Different blocks for data handling, DCS configuration and monitoring
- 96 pipelines memories with 12.8 μs depth (48 PMT channels x 2 gains)



- TTC decodification
  - Level-1 Accept signal and commands
  - LHC clock recovery
- Three different readout paths:
  - FELIX (GBT)
  - ROD (G-Link)
  - Ethernet port (IPBus)
- Controlled through Ethernet – IPBus

	Virtex 7 485T		
Slice Logic Utilization	**Used**	**Available**	**Utilization**
Slice Registers	152,696	**607,200**	25%
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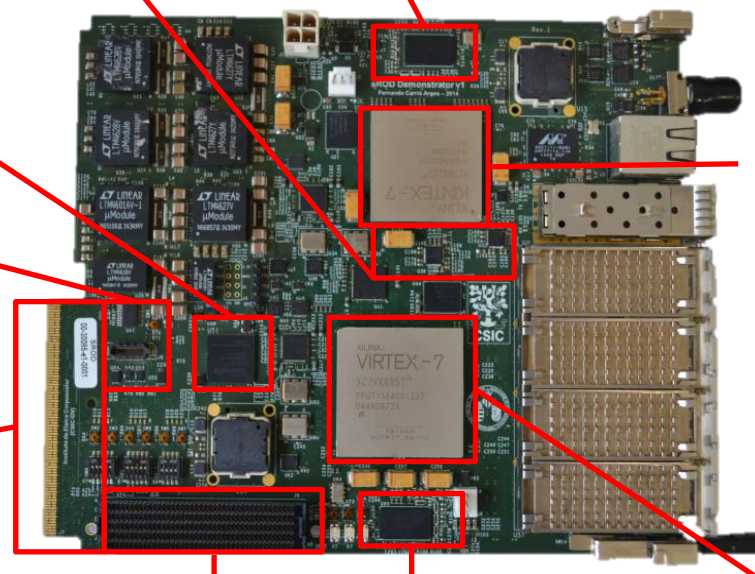
RAMB36E1	107	**1,030**	10%
RAMB18E1	741	**2,060**	35%
MMCMs	4	**14**	28%
PLLs	2	**14**	14%
Transceivers	19 **+ 4**	**56**	41%
DSP slices	**1152**	**2,800**	41%

TilePPr Demonstrator - overview

- First prototypes delivered at the end of 2014
- Extensively used in test beams and labs
- Power consumption below 60 W

- PCB stack-up: 16 layers
  - Dielectric Nelco N4000-13SI
- 4 QSFP modules: 160 Gbps
- Avago MiniPOD: 120 Gbps
- Backplane: 40 Gbps

320 Gbps



2 x CDR IC
- ADN2814
- Clock/data from TTC

DDR3
512MB

Xilinx Spartan 6
- Slow control capabilities

Module Management Controller (MMC)
- Power connection management

TTC input

Xilinx Kintex 7 FPGA
- XC7K420T
- 28 transceiver@10 Gbps

4 QSFP modules (16 links)
Up to 160 Gbps

AMC connector
- 12 V power connection
- High-speed communication path

FMC connector
- Expansion funcionalities

DDR3
512MB

Xilinx Virtex 7 FPGA
- XC7VX485T
- 48 transceiver@10 Gbps