TileCal-IFIC Group: Readout electronics R&D for FCC

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Jornadas de la Red Española de Futuros Colisionadores

CIEMAT – September 23, 2025

CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

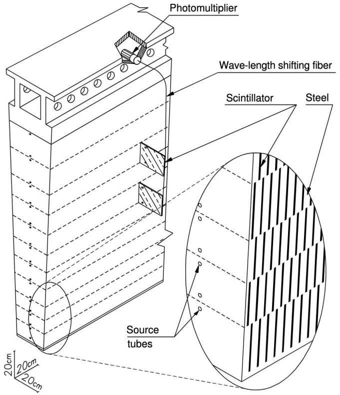
VNIVERSITAT DE VALÈNCIA

INSTITUT DE FÍSICA CORPUSCULAR

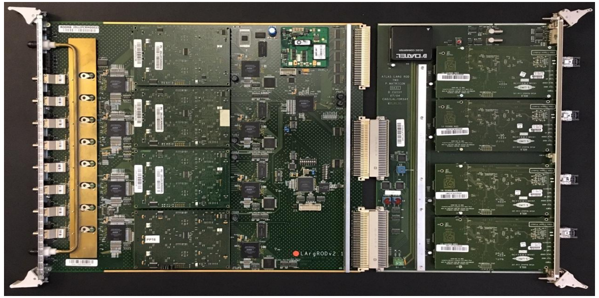
EXCELENCIA SEVERO OCHOA

Research Group History

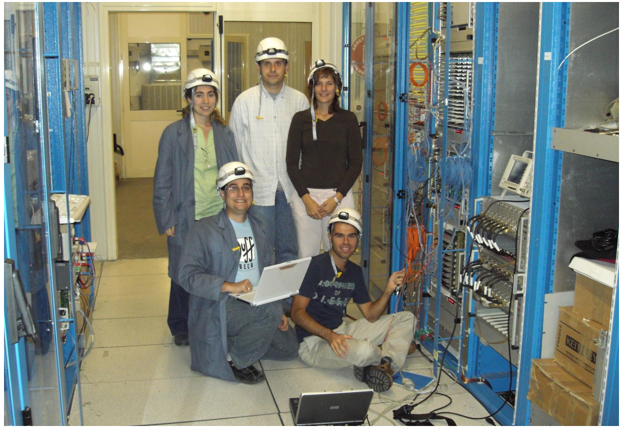
- ATLAS Tile Calorimeter (TileCal): central hadronic calorimeter of the experiment, made of steel and scintillating tiles
- The TileCal-IFIC group has participated in many different areas:
  - Assembly of 320 submodules
  - Qualification of 1750 PMTs (17%)

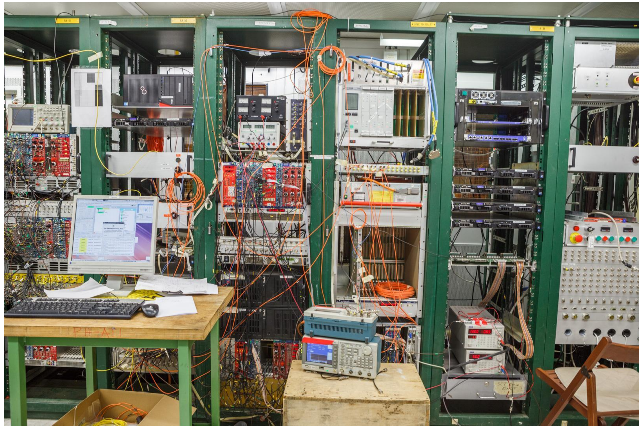


Research Group History (cont'd)



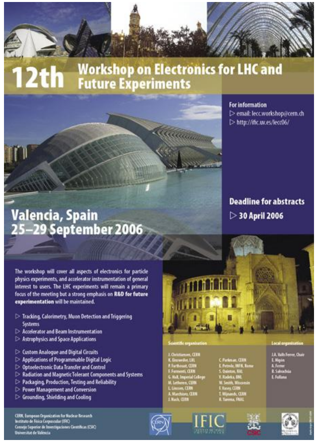
- **Read-Out Drivers (RODs)**: production, installation, commissioning, and maintenance
  - FPGA firmware and DSP code: development and maintenance
- Operations: Data preparation, signal reconstruction, DAQ
- **Tile PreProcessor (PPr)** for HL-LHC: design, production and installation (76% core contribution to PPr production ~1.2 M€)





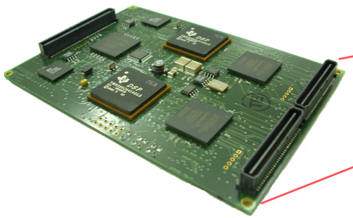
Research Group History (cont'd)

- **Coordination roles:**
  - in TileCal: Upgrade Coordinator, Upgrade Deputy Project Leader, Electronics Upgrade Coordinator, etc.
  - in ATLAS: Trigger Coordinator, Trigger Menu and Signature Performance Coordinator, E/gamma convener, Next Generation Trigger Project Task 2.7 leader, etc.
- **Projects:**
  - Plan Nacional: >10 projects for TileCal construction, operation and upgrades
  - Generalitat Valenciana and EU resilience funds
- Organized schools and conferences in Valencia: LECC2006, ISOTDAQ school in 2020, ATLAS TDAQ Week in 2024

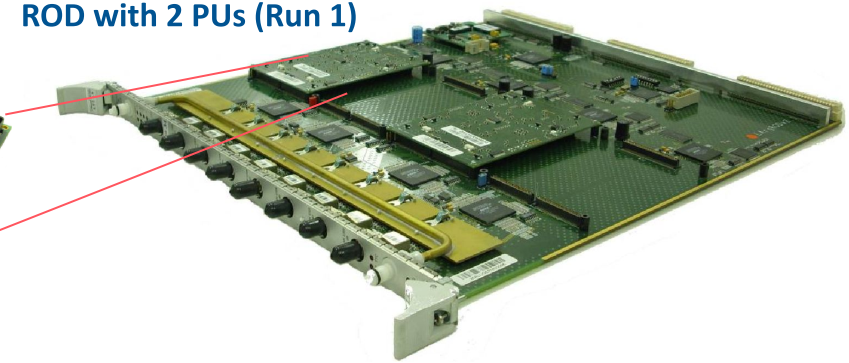


TileCal Read Out Drivers (RODs)

- **ROD**: core element of the current back-end electronics
  - Interface between the front-end electronics and the HLT
  - 9U VME custom module, 32 RODs to readout the entire detector
  - Functions: Deserialization, data/trigger synchronization, error checking, signal reconstruction, detector raw data compression, output data formatting, monitoring, data flow control (veto)
  - Each ROD has:
    - 10 FPGAs: data routing and formatting (VHDL)
    - Up to 4 Processing Units: data processing in DSP (C & assembler)



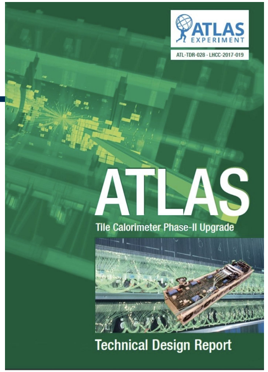
Processing Unit (PU)

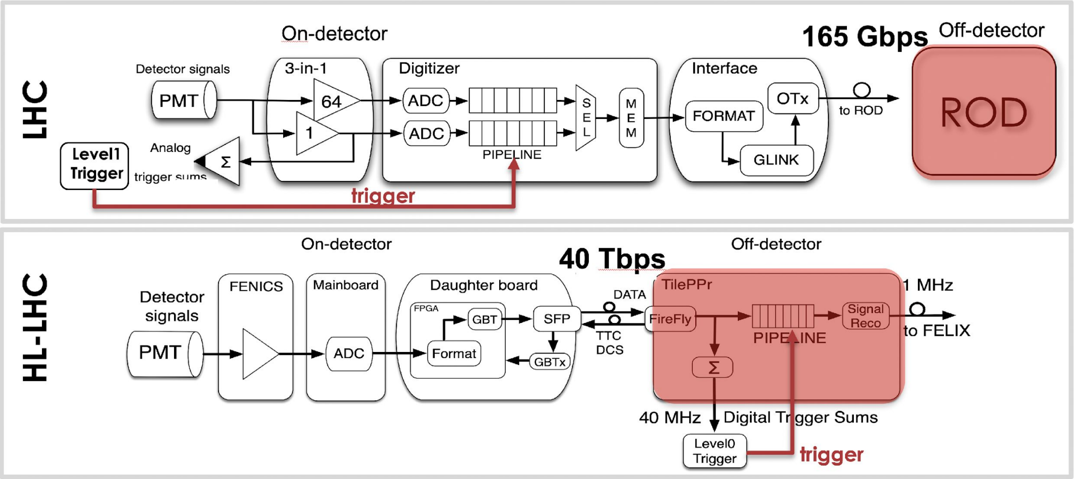


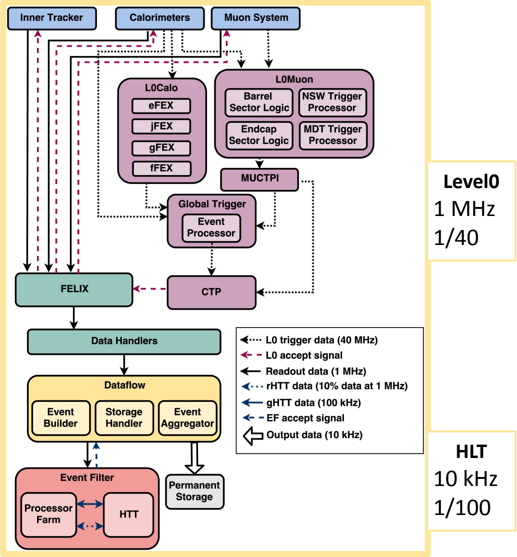
ROD with 2 PUs (Run 1)

DAQ evolution for HL-LHC

- Minimize internal detector electronics to avoid radiation exposure
  - 40 Tbps bandwidth required with fixed and deterministic latency
  - Send information to the trigger system for each cell with maximum resolution and low, deterministic latency → **PreProcessor (PPr)** crucial element in the Trigger/DAQ chain
  - Real-time energy reconstruction with high resolution for ~10,000 channels
  - **Crucial contributions to the system design and development since the IDR**





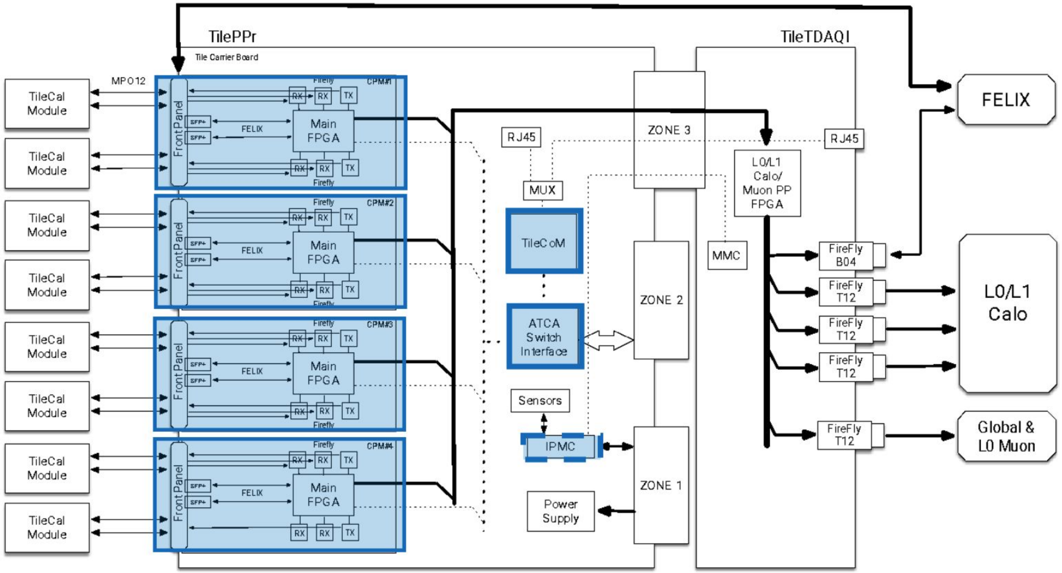


TileCal HL-LHC off-detector electronics

- **Tile PreProcessor (PPr):** core element of the off-detector electronics for HL-LHC
  - Data processing, clock distribution, on-detector configuration, energy reconstruction, low latency interface with L0 trigger and readout
  - Modular concept: design optimization, manufacturing processes, enhance components maintenance and replaceability and facilitate future improvements in terms of functionality

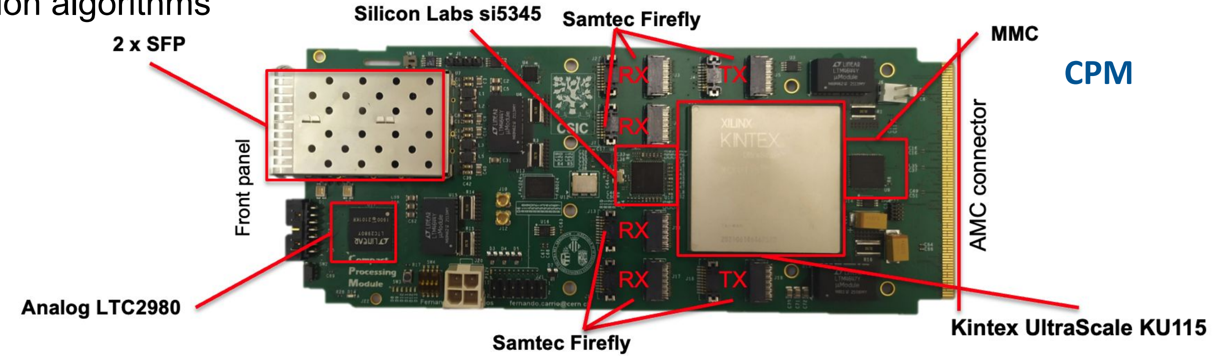
The TileCal-IFIC Group is responsible for the design and production of:

32 ATCA Carrier Boards
32 GbE Switch modules
32 TileCoM SoC modules
32 IPMCs
128 CPMs



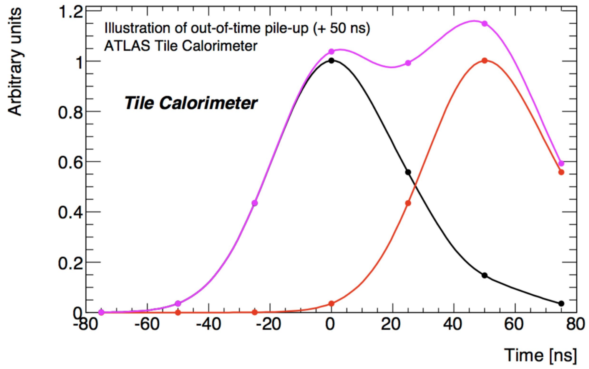
Development of the PPr system

- PPr prototypes currently being validated, with demonstrator system in current ATLAS data taking → Next step: Production and validation of 32 modules
  - 128 Compact Processing Modules (CPMs) by the end of next year.
  - Installation, maintenance, and upgrades throughout the HL-LHC operational lifetime (2030–2041)
  - HDL development: signal reconstruction algorithms

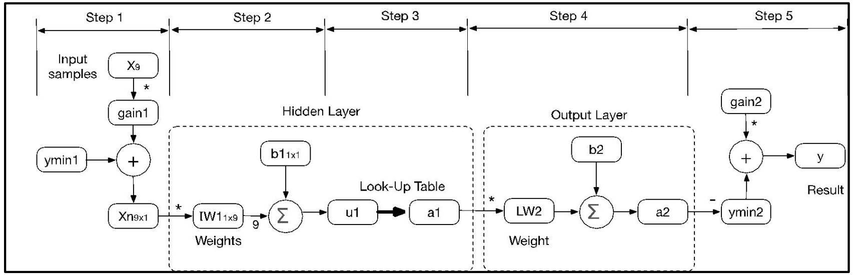


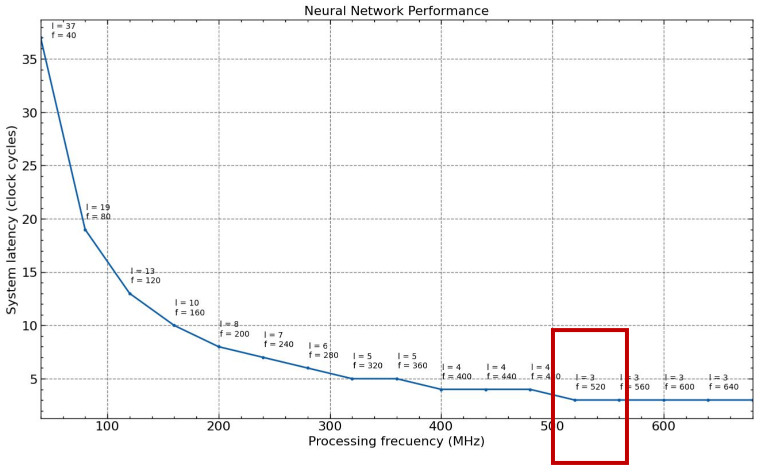
Real Time Signal reconstruction with AI

- Convert digital samples into signal *energy* and *time*
  - ~10,000 channels @ 40 MHz (25 ns) → 77 channels per CPM
  - High pile-up (μ~200) → Distortion of the signal shapes
- Signal reconstruction based on neural networks
  - Offline training using simulated or real data
  - Use of DSP blocks in FPGA, optimized for fixed-point arithmetic
  - 77 channels in parallel – 3 bunch crossings (75 ns)
  - Studying different network options: convolutional, recurrent, multilayer perceptron, weight binning, etc.

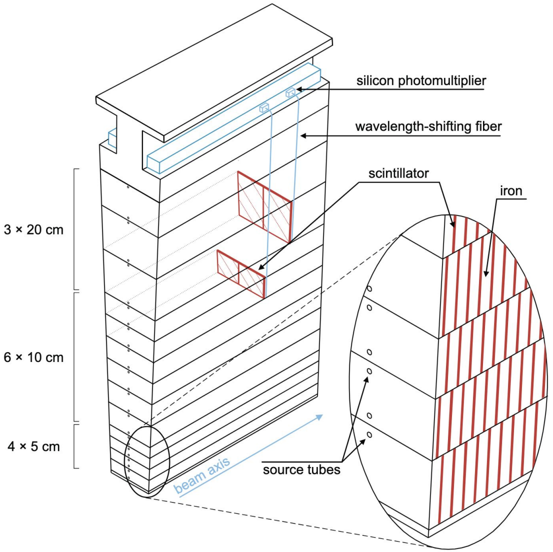


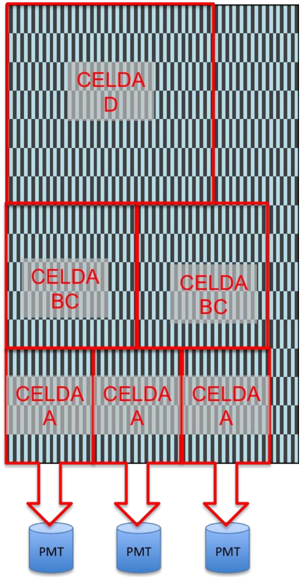
Latency 75 ns

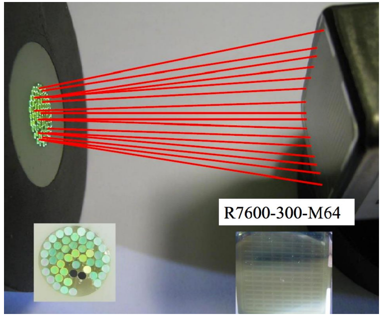




Contributions to DRD Calo (DRD6)







- Proposal to build a scintillator calorimeter with TileCal-like geometry for FCC
  - Greater longitudinal and transverse segmentation → Improved spatial resolution
- **Allegro:** Calorimeter similar to ATLAS (EM + Had) with enhanced segmentation
  - “Digital” calorimeter capable of reconstructing particle showers

IFIC-CIEMAT Prometeo Project

- Title: **Advanced Data Processing Technologies for Exploring New Physics in Future Particle Colliders**
  - Funded with 600k € during 2025-2029 by Generalitat Valenciana under the Prometeo program for excellence research groups.
- Researchers (physicist / engineer):
  - **IFIC:** Arantxa Ruiz (PI), Alberto Valero, Ximo Poveda, Fernando Carrió, Juan Valls
  - **CIEMAT:** Cristina Fernández, Ignacio Redondo
  - Looking for PhD student (physicist/engineer)
- **Context & Motivation:**
  - Support **Future Circular Collider (FCC)** development.
  - Contribute to **ECFA Detector R&D Roadmap** in **DRD6** (Calorimetry) and **DRD7** (Electronics)
- **Main Goals of the project**:

Physics case studies for FCC-ee & FCC-hh	**Develop advanced calorimeter components:** Multi-channel SiPMs / MPPCs, Radiation-hard readout/control electronics.	**Innovate DAQ systems** for massive data rates	**Real-time signal processing** with **NNs on FPGAs**	**Cross-disciplinary technology transfer** (electronics, computing, photodetectors)

GENERALITAT VALENCIANA

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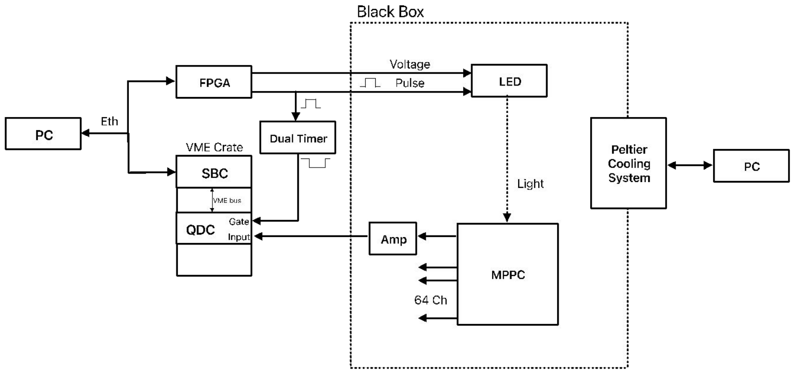
IFIC-CIEMAT Prometeo Project

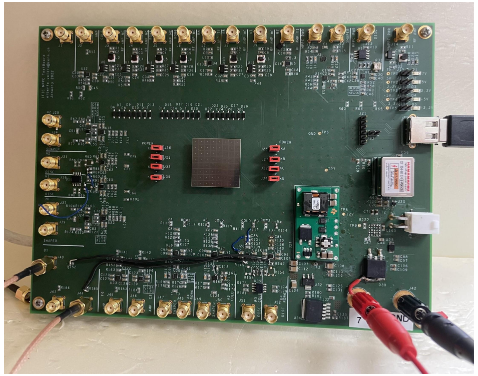
- Work plan organized in six work packages (WPs)
- Key activities / deliverables:
  - Build test benches for SiPMs.
  - Design front-end & back-end electronics.
  - Implement high-speed optical links.
  - Develop FPGA-based AI algorithms.
  - Simulate detector performance & optimize designs.
  - Fabricate prototypes and validate in beam tests.

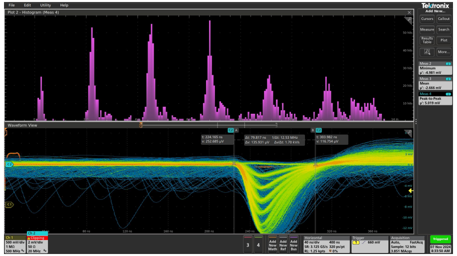
	2025		2026				2027				2028				2029		
Task	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
Work Package 1 (WP1): Evaluation and Certification of Silicon Photomultipliers (SiPMs)																	
1. Identify commercially available and prototype SiPMs for evaluation.	■	■	■														
2. Develop a PMT test bench for detailed performance analysis, including light yield, timing, and noise characteristics.			■	■	■	■	■	■	■								
3. Test radiation tolerance and longevity under high-radiation environments.									■	■	■	■					
4. Publish findings on SiPM performance for potential FCC applications.											■	■	■	■			
Work Package 2 (WP2): Development of Readout and Control Electronics																	
1. Design front-end electronics for signal amplification, shaping and digitization.	■	■	■	■	■	■	■										
2. Integrate control systems to manage device operation and calibration.			■	■	■	■	■	■	■	■							
3. Prototype readout modules and validate their performance in a controlled laboratory environment.								■	■	■	■	■	■				
4. Ensure compatibility with FCC detector system requirements.												■	■	■			
Work Package 3 (WP3): Data Acquisition (DAQ) Systems Development																	
1. Design front-end DAQ components to digitize signals from SiPMs.	■	■	■	■	■	■	■	■	■	■							
2. Develop high-speed optical links for data transfer.			■	■	■	■	■	■	■	■							
3. Implement a modular back-end system for data processing and storage.							■	■	■	■	■	■	■	■			
4. Test DAQ systems under simulated FCC data conditions.												■	■	■	■	■	
Work Package 4 (WP4): Signal Processing and Reconstruction Algorithms																	
1. Develop neural network-based algorithms for real-time signal processing on FPGA platforms.			■	■	■	■	■	■	■	■	■	■	■	■			
2. Optimize algorithms for noise filtering and particle flow reconstruction.							■	■	■	■	■	■	■	■	■		
3. Benchmark the algorithm performance against traditional reconstruction methods.								■	■	■	■	■	■	■			
4. Test and integrate algorithms with the DAQ system.												■	■	■	■	■	■
Work Package 5 (WP5): Feasibility Studies and Simulations																	
1. Develop simulation models for high-granularity calorimeter configurations in FCC-ee and FCC-hh environments.	■	■	■	■	■	■	■										
2. Study energy resolution, efficiency, and particle flow reconstruction under different scenarios.						■	■	■	■	■	■						
3. Analyze detector performance in terms of radiation hardness and long-term stability.										■	■	■	■	■	■		
4. Provide optimization recommendations for detector designs based on simulation results.													■	■	■	■	■
Work Package 6 (WP6): Prototyping and Test Beam Campaigns																	
1. Fabricate 3,Äì5 prototype calorimeter modules based on DRD6 recommendations.								■	■	■	■	■	■	■			
2. Integrate SiPMs, electronics, and DAQ systems into prototypes.								■	■	■	■	■					
3. Conduct test beam campaigns at CERN SPS or similar facilities to validate performance.										■	■	■	■	■	■	■	■
4. Analyze results to refine detector design and implementation strategies.															■	■	■

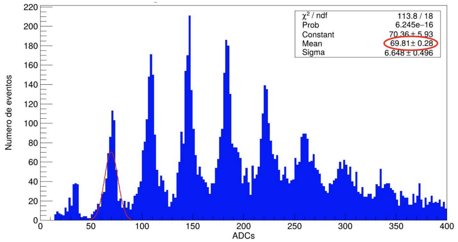
Preliminary work: MPPC Certification

- Testbench revival:
  - New black box, Peltier system for temperature control
  - Custom board designed to readout 64-channel MPPC (multi-pixel photon counter)
  - Tested Hamamatsu S13361-3050AE-08 (64ch) S13361-6050AE-04 (16ch)
  - Setup able to detect single photoelectrons on the oscilloscope



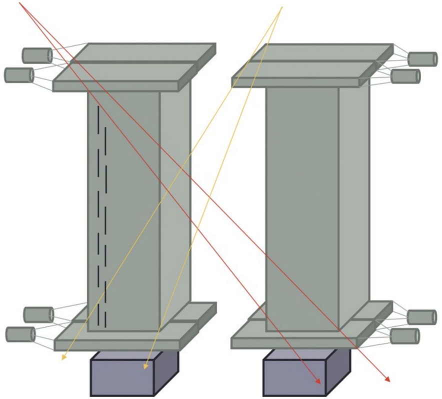


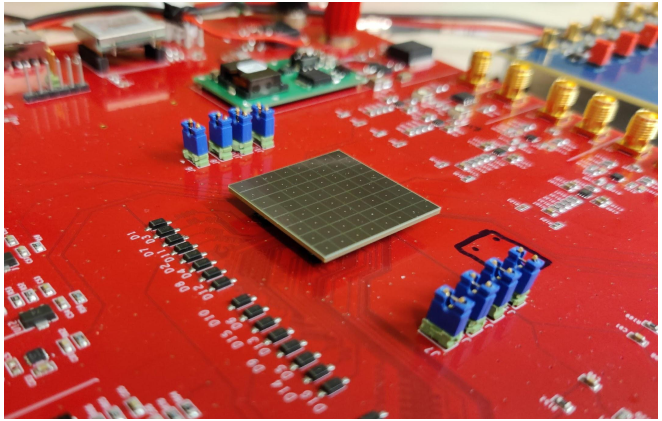


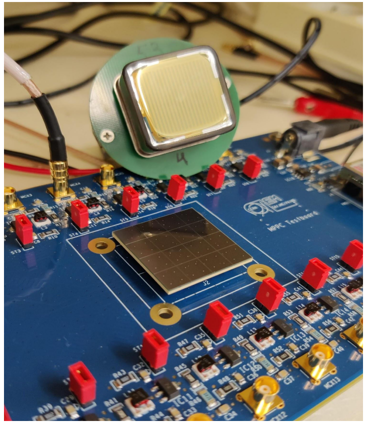


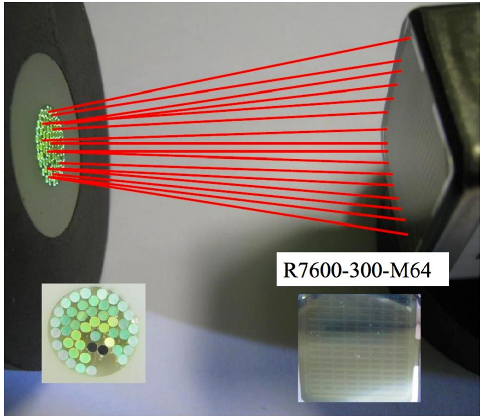
Detector R&D6 : Calorimetry

- Instrumentation of two high-granularity modules:
  - Maximum segmentation
  - Cosmic rays – sources
- Use of new readout technologies:
  - Silicon Photomultipliers and Multi-Pixel Photon Counters
  - Up to 64 channels in the same area → high granularity
  - Challenge: processing information from all channels









Summary

- Long expertise of the TileCal-Valencia team in ATLAS hadronic calorimetry:
  - Detector Construction
  - PMT certification
  - Read-out electronics:
    - RODs during Runs 1-3
    - TilePPr for HL-LHC
- Looking ahead:
  - Already involved in DRD6 and DRD7
  - Project in collaboration with CIEMAT to develop new readout technologies for FCC, with the goal of building a calorimeter prototype

Acknowledgements

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  - Project CIPROM/2024/69 funded by Generalitat Valenciana
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