LHCb Upgrade II

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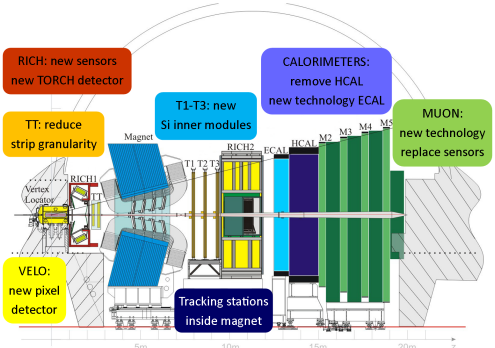
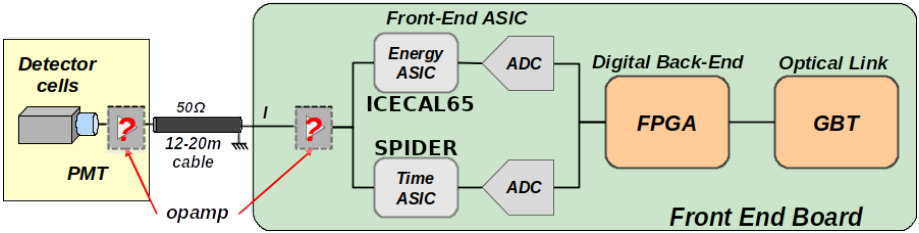
LHCb Upgrade II

- Wide program of improvements for the LHCb detector to face the HL-LHC era (time measurements against combinatorial explotion due to luminosity/pile-up)
- IFIC involved in front-end electronics development for two subsystems:
  - PicoCal: PMT readout for heterogeneous technology calorimeter,
  - SciFi: SiPM readout for scintillating fibre section of the Mighty Tracker.



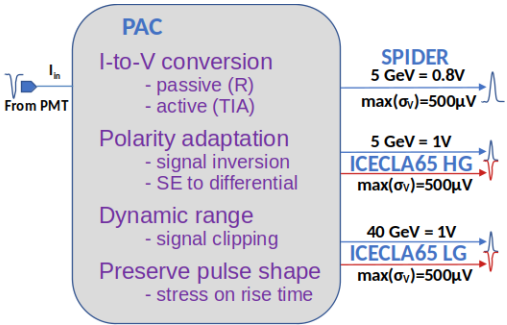
PicoCal Electronics

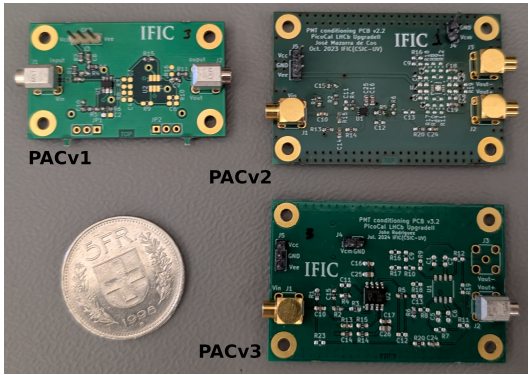
- PicoCal aims at energy (12bit,$E_T \approx 40$GeV) and time ($\sigma_t \approx 10$ps) measurements using different technologies (SpaCal/Shashlik, W/Pb, GAGG/Polystyrene).
- ASICs using PMT signal under development in TSMC 65nm ($V_{supply}=1.2$V).
- Front-end electronics in racks on the platform on top of the detector.
- Variable length analog link (coaxial 50Ω) between modules and font-end.
- PMT conditioning circuit for ASIC input range on base or front-end board.



PAC: PMT Acquisition & Conditioning Circuit

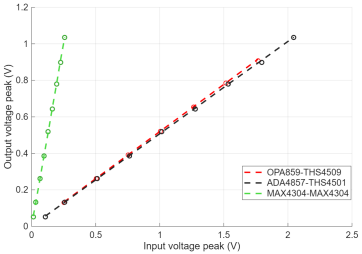
- COTS based two stage amplifier with intermediate divider/filter.
- Several prototypes with different footprints for testing multiple OpAmps.
- Commercial OpAmps force tradeoff among speed, stability and dynamic range. (process 2ns t_{rise}/250MHz BW signal over 40mA/2V range with 50Ω conversion)





PAC: PMT Acquisition & Conditioning Circuit

- Intensive lab test to produce a configuration for each board compatible with SPIDER (v1) and ICECAL65 LG (v2 and v3) energy and voltage range :
  - PACIFICv1: MAX4304(1.8V/V;2.5V/V) on both stages with 0.55V/V divider,
  - PACIFICv2: OP859(1V/V) + THS4509(2.9V/V) with 0.95V/V resistor divider,
  - PACIFICv3: ADA4857(1V/V) + THS4501(1V/V) with 0.95V/V resistor divider.
- Results show good linearity and $<10\%$ rise time loss in all cases.
- PACIFICv2 has limited input range and noise density out of specs.
- All boards under test at SPS, analysis and comparison to lab results shortly.



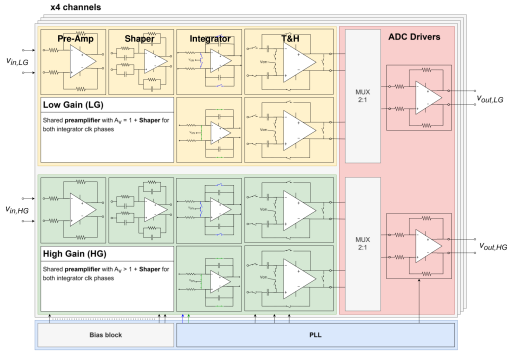
Board	Range [V]	Gain[V/V]	t_{rise}[ns]	Noise[$\mu V/\sqrt{Hz}$]
PACIFICv1	>0.25	3.199	2.244	211
PACIFICv2	1.75	0.517	2.181	1165
PACIFICv3	>2	0.505	2.186	193.569

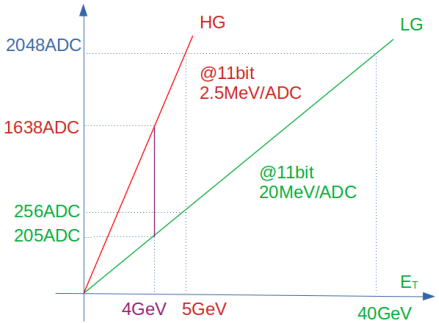
Reference pulse has 2.187ns rise time

using same AWG and oscilloscope

ICECAL65: Energy ASIC

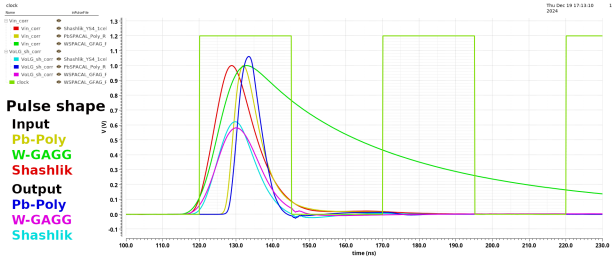
- Two 11bit processing paths with factor 8 between their gains.
- Automatic internal selection of gain with fast comparator.
- Common acquisition and filtering per gain path with double time interleved switched section for integrator reset.
- Per channel clock phase selection to synchornize and set ADC sampling.





ICECAL65: Energy ASIC

- Differential PZ filter designed and adjusted for all pulse shapes fulfilling:
  - $\pm$1ns plateau around maximum BX0 signal with $<$1% variation,
  - $<$1% spillover in previous and following BXs throughout full plateau,
  - limited R$<$2Ω(noise) and C$<$7pF(area) except W-GAGG,
  - equalized output BX0 area (not amplitude) for all cases (PVT + modules).
- Awainting chip production (TSMC65nm) to test block.

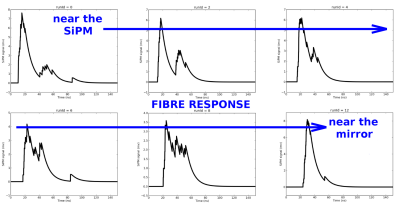


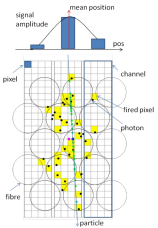
Module	Corner	Amp[mV]	A BX0[nVs]	palteau[ns]
W-GAGG	FAST	550	7.432	3.83428
	NOM	565.6	7.77	3.78906
	SLOW	521.4	7.247	3.72878
Pb-Poly	FAST	990.3	7.265	10.8467
	NOM	979.5	7.14	10.9098
	SLOW	913.7	7.882	7.96332
Shashlik	FAST	636.8	7.703	4.32604
	NOM	577.6	7.971	3.82629
	SLOW	608.6	7.789	3.80251

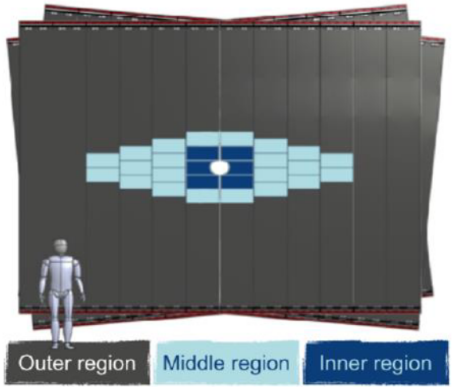
1V peak input pulse; baseline corrected

SciFi Electronics

- Mighty Tracker: three stations with four layers each in XUVX configuration, CMOS MAPS (Si pixel) inner region/scintillating fibers + SiPMs outer region.
- Aiming at 99% hit efficiency with <100μm resolution with 250μm granularity.
- Waveform and delay depend on position, shaper + integration to get charge.
- SiPMs not matched with fibres, clustering process required.
- Introduce <1ns time measurement.

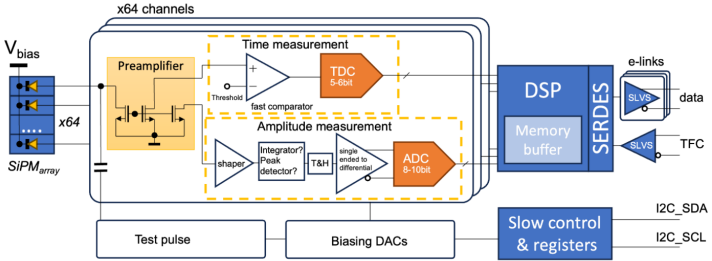






PACIFIC++

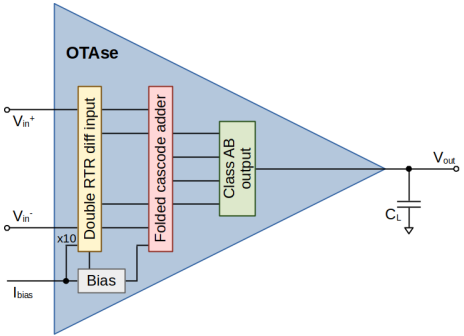
- SiPM readout ASIC with anode DC coupling and current mode input.
- Two processing paths with 10bit ADC and 6bit TDC respectively.
- Integrated digital processing (cluster) and Gbps serialized output.
- Double interleaved scheme for integrators to allow continuous operation.
- Low power single-ended and differential OTAs required for analog chain. (power 1-2mW; GBW 250MHz; SR 200mV/ns; noise 500µV)



Parameter	PACIFIC++
Technology	**65 nm**
Number of channels	64
Channel connection	Single ended, DC coupled
Signal polarity	Positive
Gain	4 different gains
Sensor bias	**Not needed**
Power consumption	1.2V 0.5 W + 2.5V 0.5 W
Shaping	Tuneable tail cancelation
ADC	**ADC 10 bits**
TDC	**≈0.4 ns, 6 bits**
Calibration	Integrated charge injection
DSP	**Clustering and raw output**
I/O interface	**eLinks @ 1.28 Gbit/s**
Slow control / TFC	I2C / eLink

OTAse in PACIFIC++

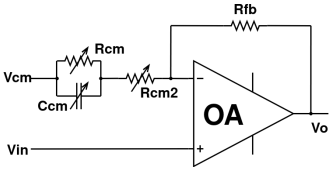
- Rail-to-rail differential input with equalized g_m across common mode range.
- Folded cascode for amplification and Class AB output for rail-to-rail swing.
- Selectable capacitor (4 values) for the Miller compensation network.
- Schematic available and tested in extreme corners with 100fF and 1pF load.

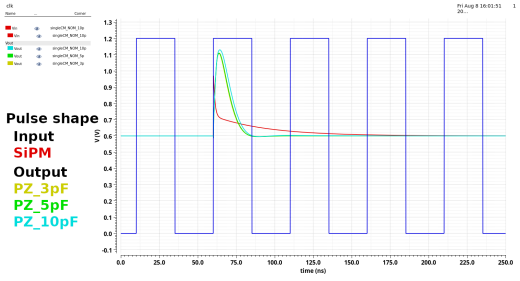


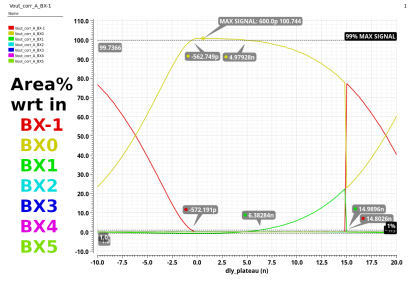
Corner	NOM	SS	FF
Ibias [µA]	10	10	14
Power [µW]	775.7	662.7	1221
GBW 100fF [MHz]	291.8	257.1	290.9
GBW 1pF [MHz]	289.4	255.5	289.6
Φ_M 100fF [°]	69.33	69.08	76.01
Φ_M 1pF [°]	61.33	59.92	72.26
A_M 100fF [dB]	11.2	9.484	14.75
A_M 1pF [dB]	7.416	6.211	10.02
Slew Rate 100fF [MV/s]	222.1	214	225.6
Slew Rate 1pF [MV/s]	222.5	215	225.9
$RMS_{1Hz\text{-}1GHz\ 1pF}$ [uV]	334.1	391.3	232.1
$RMS_{1Hz\text{-}1GHz\ 100fF}$ [uV]	394.7	461.5	254.9

PZ Shaper

- Single PZ non-inverting filter based on OTAse:
  - PZ network filters out the slow tail component,
  - OTA GBW filters out the input fast component.
- Schematic available with digital C selection, performance under test at extreme corners.
- Test common mode to extend dynamic range.
- Inverting alternative available with ideal RC.







Outlook

- IFIC contributes to photosensor readout electronics for LHCb Upgrade II

- After testbeam analysis, new PAC prototype design for collaboration use.
- Introduce clipping circuit to new prototype for evaluation.
- ICECAL65 in production, preparing test for PZ shaper evaluation.

- Create and adjust integrator schematic to add to analog chain.
- Design fully differential amplifier to adapt signal for ADC.
- Move on the layout phase.

Thanks a lot for your attention!