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Porting MADGRAPH to FPGA Using High-Level Synthesis (HLS)

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The escalating demand for data processing in particle physics research has spurred the exploration of novel technologies to enhance the efficiency and speed of calculations. This study presents the development of an implementation of MADGRAPH, a widely used tool in particle collision simulations, to FPGA using High-Level Synthesis. This research presents a proof of concept limited to a single, relatively simple process (e+ e- > mu+ mu-). The experimental evaluation methodology is described, focusing on performance comparison between traditional CPU implementations, GPU acceleration, and the new FPGA approach. This study describes the complex process of adapting MADGRAPH to FPGA using HLS, focusing on optimizing algorithms for parallel processing. These advancements could enable faster execution of complex simulations, highlighting FPGA's crucial role in advancing particle physics research. The encouraging results obtained in this proof of concept prove potential interest in testing the performance of the FPGA implementation of more complex processes.

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