

Signal reconstruction firmware of the ATLAS Tile Calorimeter for the HL-LHC

martes, 16 de septiembre de 2025 11:10 (15)

The High Luminosity Large Hadron Collider (HL-LHC) upgrade at CERN will increase luminosity, resulting in higher proton-proton interaction rates per bunch crossing at the Tile Calorimeter of the ATLAS detector. This phenomenon is known as signal pile-up and, to mitigate its impact, more complex signal reconstruction algorithms based on deep learning are required. The processing will be made using Field-Programmable Gate Arrays (FPGAs) due to their low and deterministic latency for signal synchronization. Furthermore, the signal reconstruction needs to be made using more sophisticated algorithms, such as deep-learning methods. This work aims to design and implement the FPGA firmware for signal reconstruction, operating at 40 MHz to process data before the first level of trigger, ensuring optimal performance in the HL-LHC era.

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Clasificación de la sesión : Electrónica

Clasificación de temáticas : Electrónica