



Signal Reconstruction Firmware for ATLAS-TileCal

Jornadas Tecnológicas IFIC

16/09/2025

Francisco Hervás Álvarez, Alberto Valero Biot, Luca Fiorini, Héctor Gutiérrez Arance,
Fernando Carrió, Sonakshi Ahuja, Francesco Curcio



GOBIERNO
DE ESPAÑA

MINISTERIO
DE CIENCIA, INNOVACIÓN
Y UNIVERSIDADES



Financiado por
la Unión Europea
NextGenerationEU



Plan de Recuperación,
Transformación y
Resiliencia



AGENCIA
ESTATAL DE
INVESTIGACIÓN



Introduction

LHC calorimeter read-out

- In the **LHC**, **Bunch Crossings** (BC) happen at **40 MHz** (25 ns)
- The **processing** happens after the **Level-1 Trigger**, at **100 kHz** (10 us)
- Signals are processed online using the **Optimal Filtering** (OF) algorithm
 - The processing is made using **Digital Signal Processors** (DSPs)
 - Therefore, it is **sequential**
 - **Fixed point** arithmetic is used

Optimal Filtering Algorithm

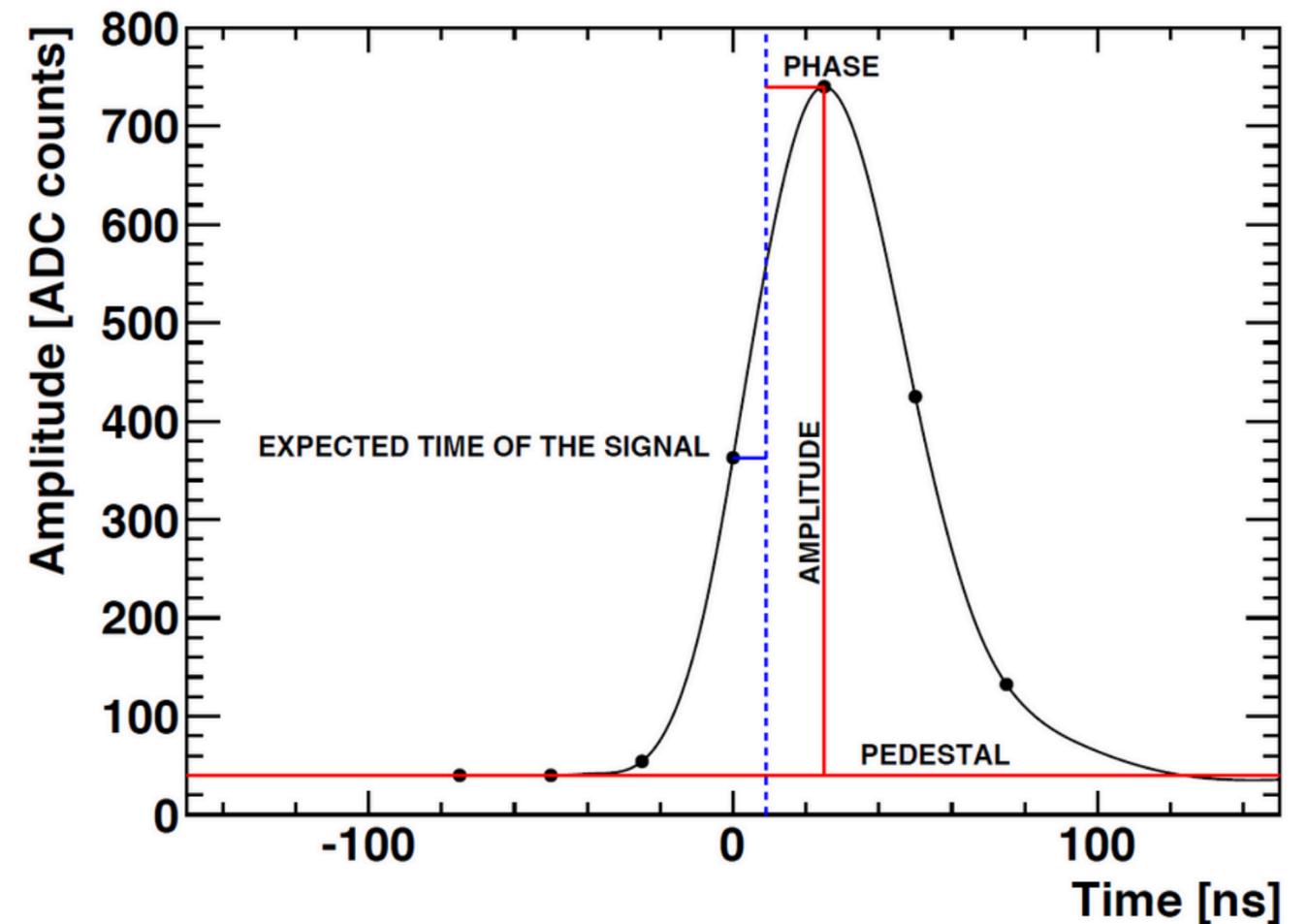
$$A = \sum_{i=1}^n a_i (S_i - p)$$
$$\tau = \frac{1}{A} \sum_{i=1}^n b_i (S_i - p)$$
$$\chi = \frac{1}{A} \sum_{i=1}^n |((S_i - p) - Ag_i)|$$

DSP Online Algorithms for the ATLAS TileCal Read-Out Drivers

Publisher: IEEE [Cite This](#) [PDF](#)

A. Valero; J. Abdallah; V. Castillo; C. Cuenca; A. Ferrer; E. Fullana; V. Gonzalez; E. Higon; J. Poveda; A. Ruiz-Marti... [All Authors](#)

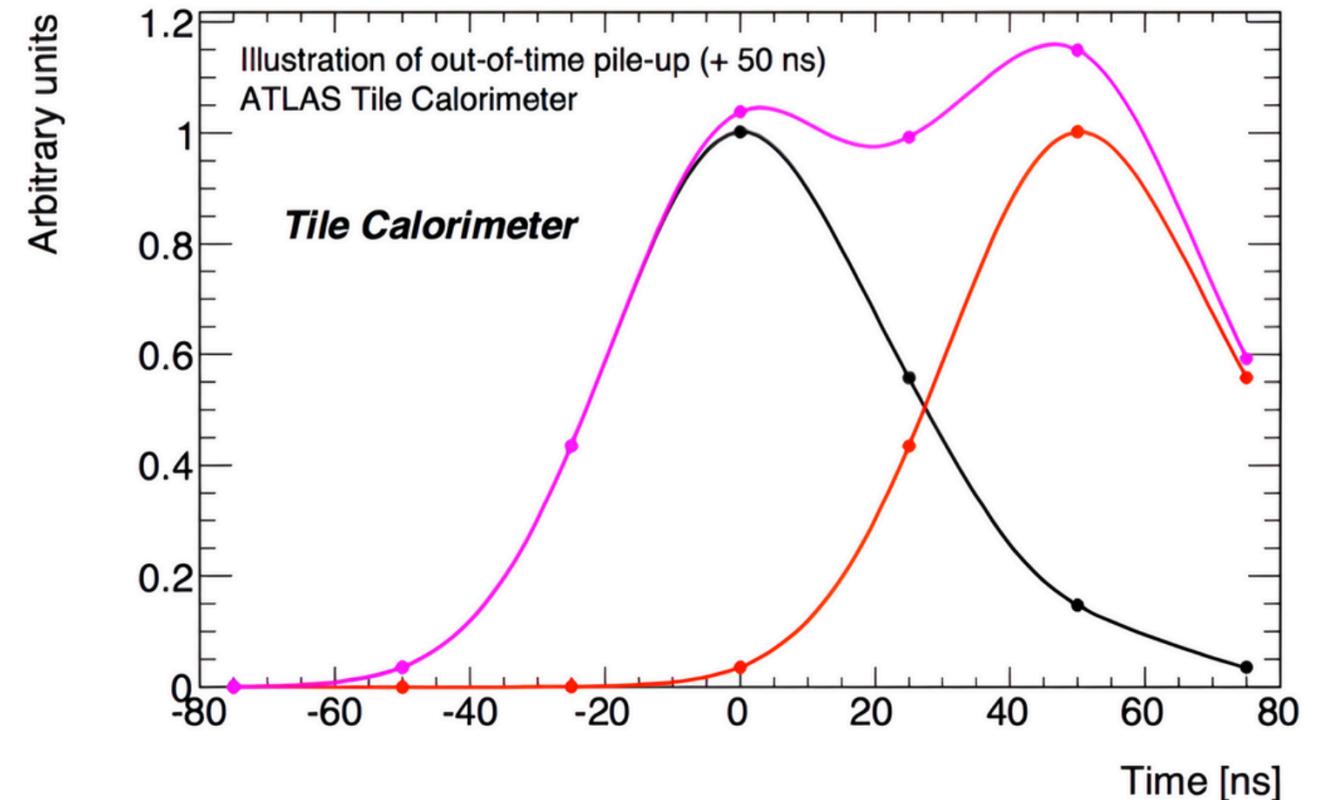
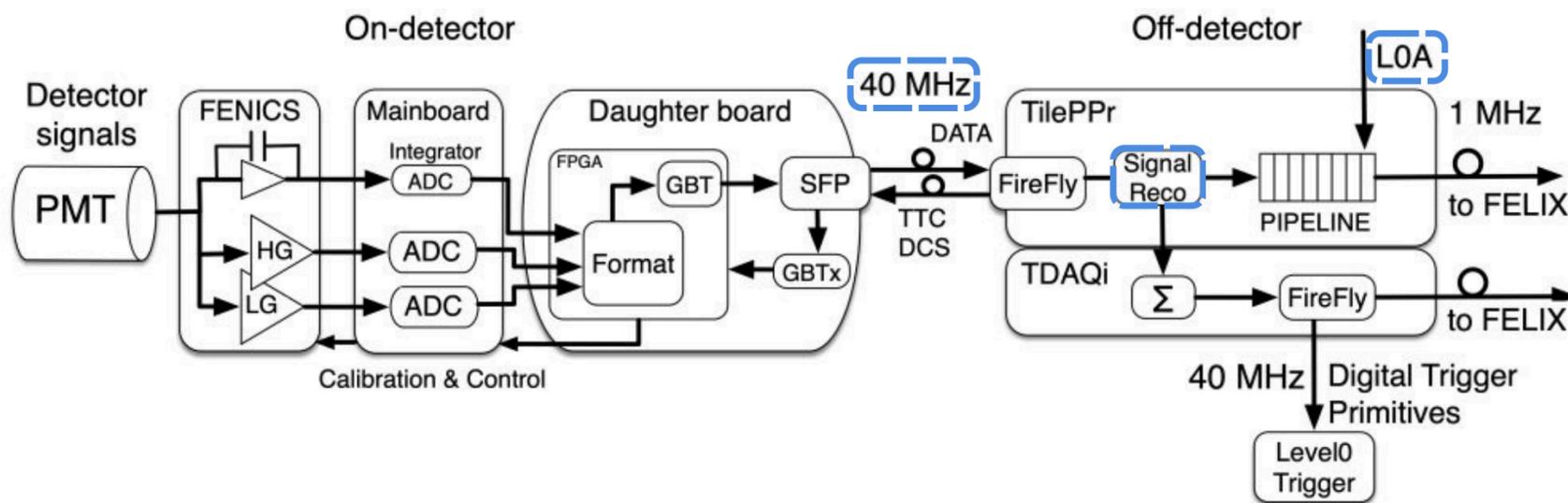
Click on the image for reading more on the topic



Introduction

HL-LHC calorimeter signal reconstruction

- In the **HL-LHC**, signals will be **reconstructed for every BC at 40 MHz (25 ns) before the trigger**
 - Signals need to be processed by **FPGAs** due to their **low and deterministic latency** for signal synchronization
 - Multiple **simultaneous signals** will produce **pile-up**
- There is a need for more sophisticated algorithms for signal reconstruction
 - **Deep learning** algorithms (**Neural Networks**)

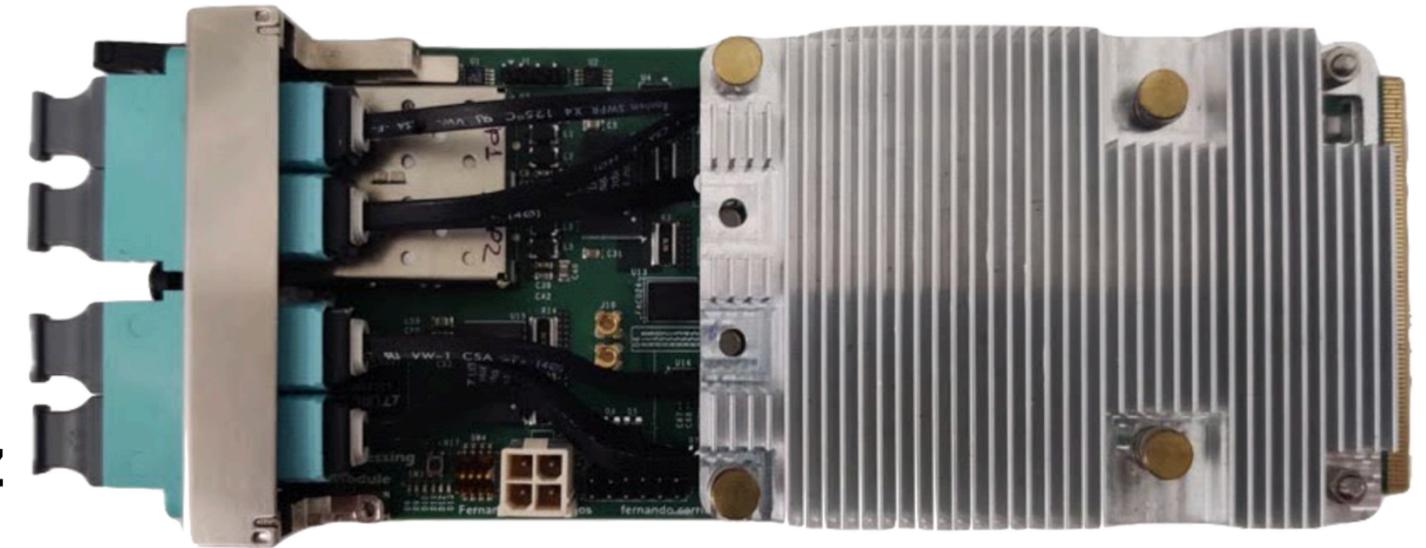


Introduction

Signal Reconstruction FPGA

Firmware requirements:

- Device: xcku115-flva1517-2-e
- **Bunch Crossing** frequency: **40 MHz**
- **Signal Reconstruction** frequency: **400 MHz**
- **Maximum latency: 10 BCs** (250 ns)
- **Maximum window size: 9 events**
 - Implies: 5 BCs
 - We have $10 - 5 = 5$ **BCs left for processing**
- Maximum absolute resources in the device:
 - **DSPs: 5520**
 - FFs: 1326720
 - LUTs: 663360
 - BRAMs: 4320



The PreProcessor module for the ATLAS Tile calorimeter at the HL-LHC

A. Valero*, F. Carrió, L. Fiorini, A. Cervelló, D. Hernandez and A. Ruiz Martinez

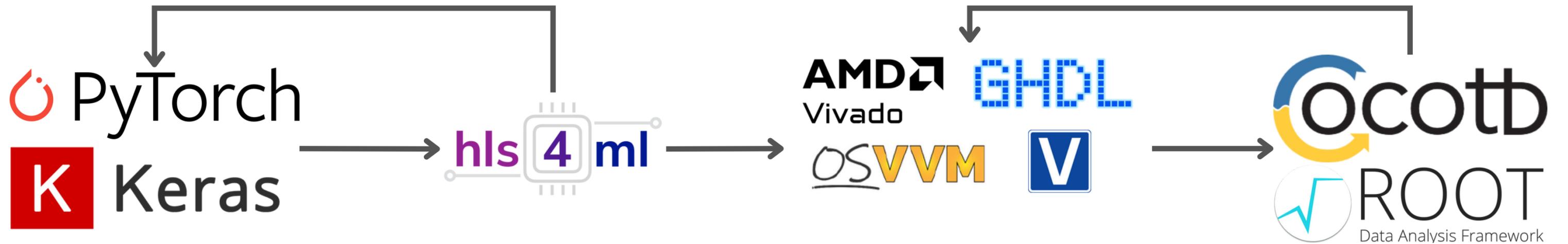
Instituto de Física Corpuscular, University of Valencia—CSIC, Valencia, Spain

Click on the image for reading more on the topic



Developing Workflow

Algorithm Elaboration Chain



SW Dev & Train

- Developing and training of ML models in SW

FW Prototyping

- Prototype models in FW
- Analysis of resources, bit widths and latencies

FW Fine-tuning

- Fine-tuning in RTL (VHDL) of the selected model
- Pre-post-processing
- Logic wrapping the ML model
- Formal verification

Physics Analysis

- FW/SW Cosimulation
- Physics data analysis
- Cosimulation made in containerised environment (Docker)

ML Models

Neural Networks

Type	Parameters	Window Size	Status
MLP	12	9	Physics Analysis
MLP	120	9	FW Prototyping
MLP	148	9	FW Prototyping
CNN	147	9	FW Fine-tuning

Open Access Article

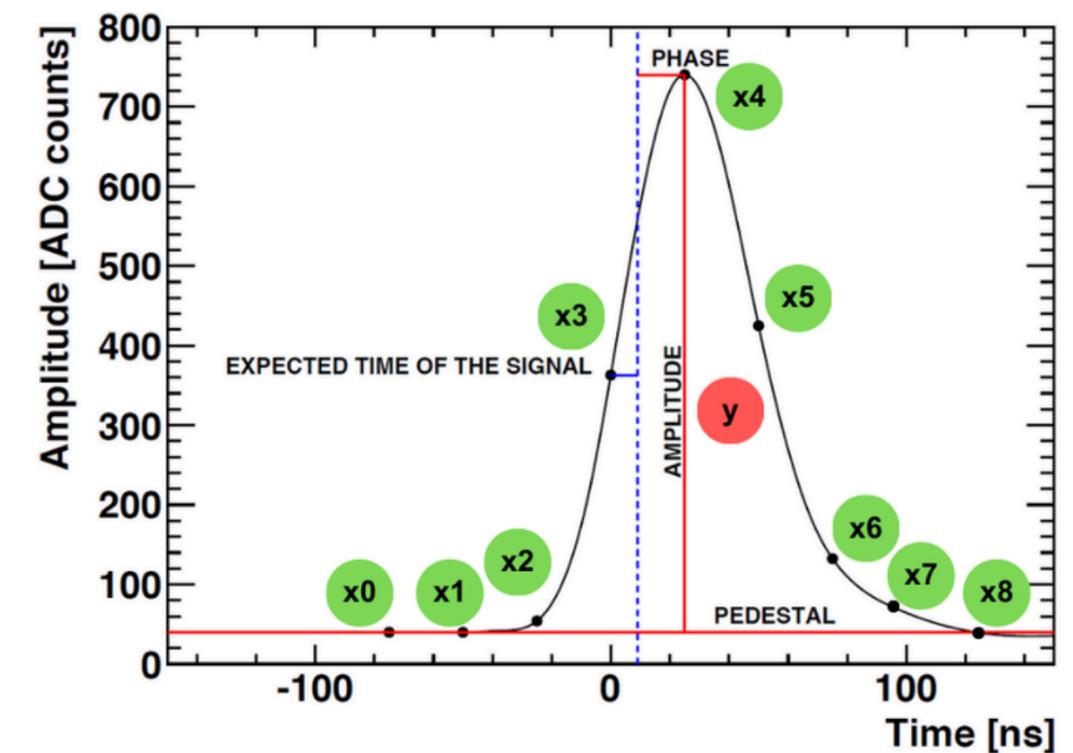
Versal Adaptive Compute Acceleration Platform Processing for ATLAS-TileCal Signal Reconstruction

by Francisco Hervás Álvarez ^{*}, Alberto Valero Biot, Luca Fiorini, Héctor Gutiérrez Arance, Fernando Carrió, Sonakshi Ahuja and Francesco Curcio

Instituto de Física Corpuscular (CSIC-UV), catedratic José Beltran 2, 46980 Paterna, València, Spain
^{*} Author to whom correspondence should be addressed.

Particles 2025, 8(2), 49; <https://doi.org/10.3390/particles8020049>

Submission received: 3 February 2025 / Revised: 28 February 2025 / Accepted: 19 April 2025 / Published: 1 May 2025



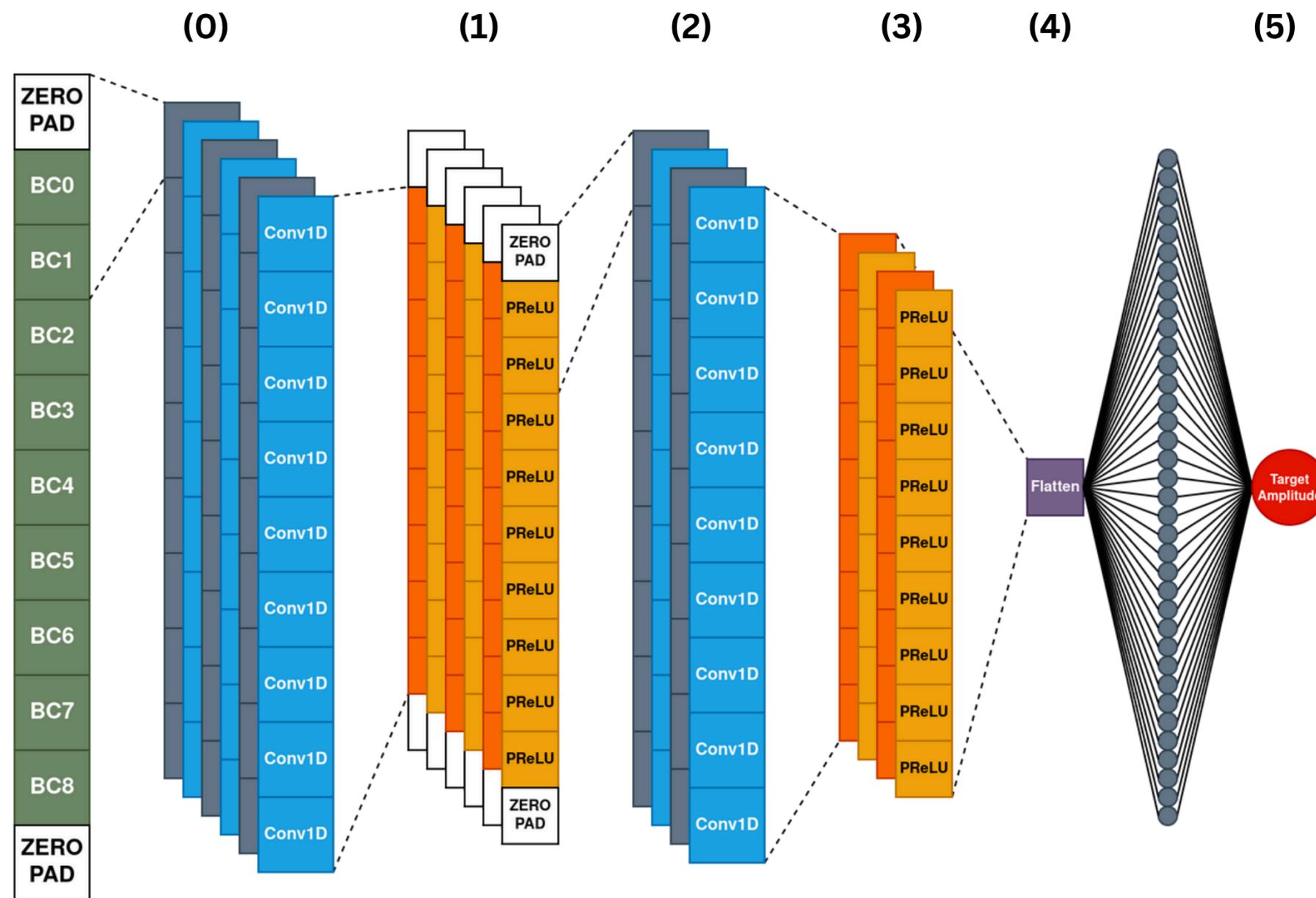
Limited to 9 because of the latency:
• WS9 = Minimum latency of 5BCs

CNN 147P WS9

Software Model

++++
Model type: CNN
Cells: A1
Window size: 9
Loss: hybrid
Date: 2025-05-29
Time: 15:45:56
Parameters: 147
++++

Sequential(
(0): Conv1d(1, 6, kernel_size=(3,), stride=(1,), padding=(1,))
(1): PReLU(num_parameters=6)
(2): Conv1d(6, 4, kernel_size=(3,), stride=(1,), padding=(1,))
(3): PReLU(num_parameters=4)
(4): Flatten(start_dim=1, end_dim=-1)
(5): Linear(in_features=36, out_features=1, bias=True)
)



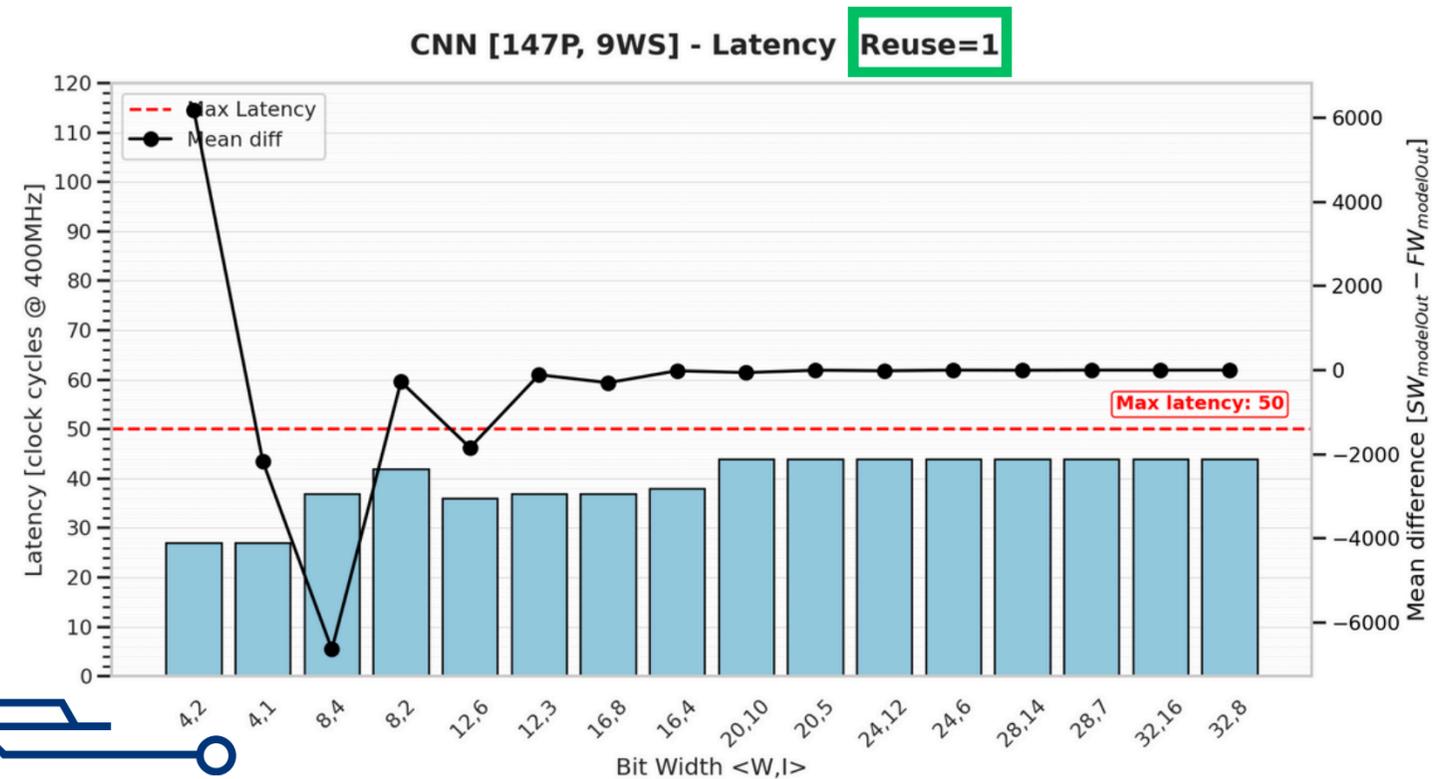
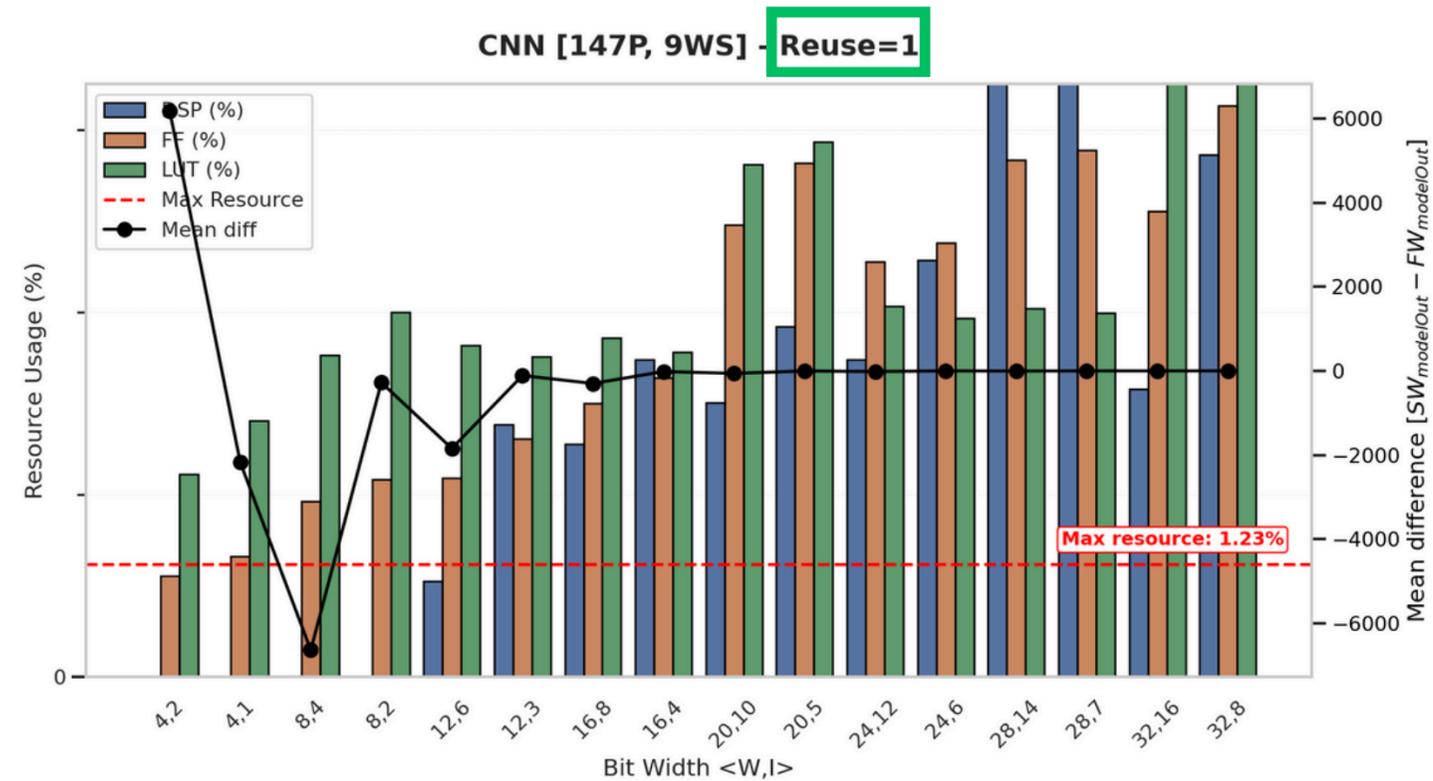
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**



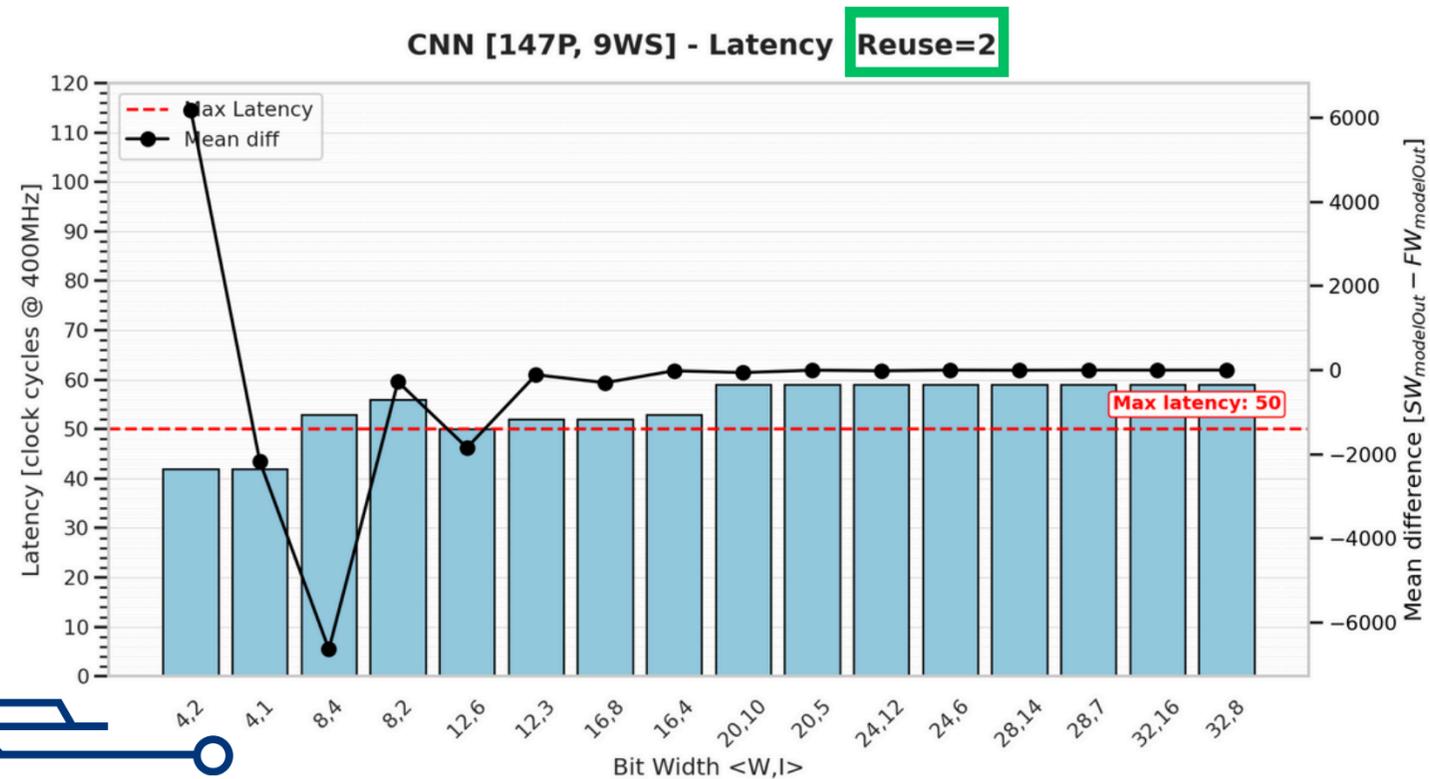
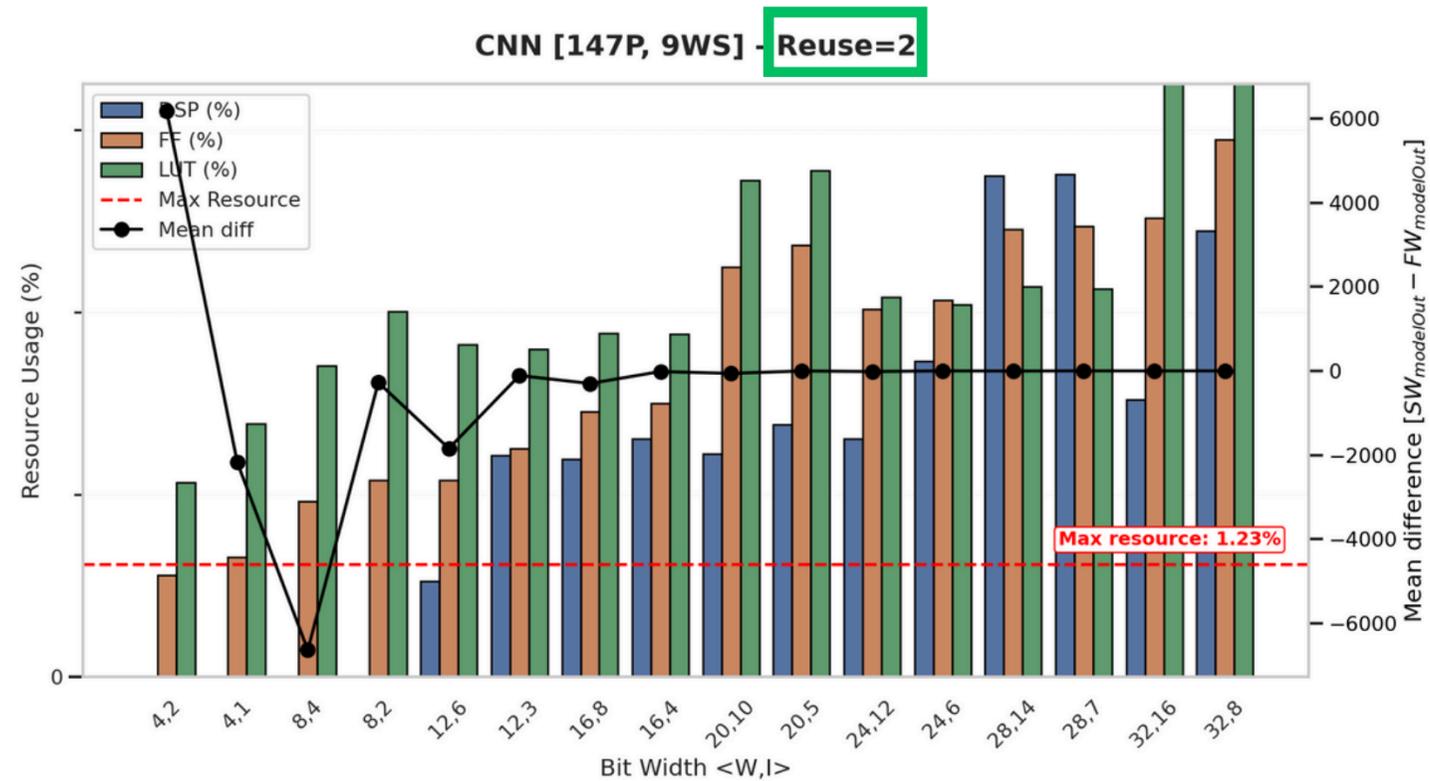
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**



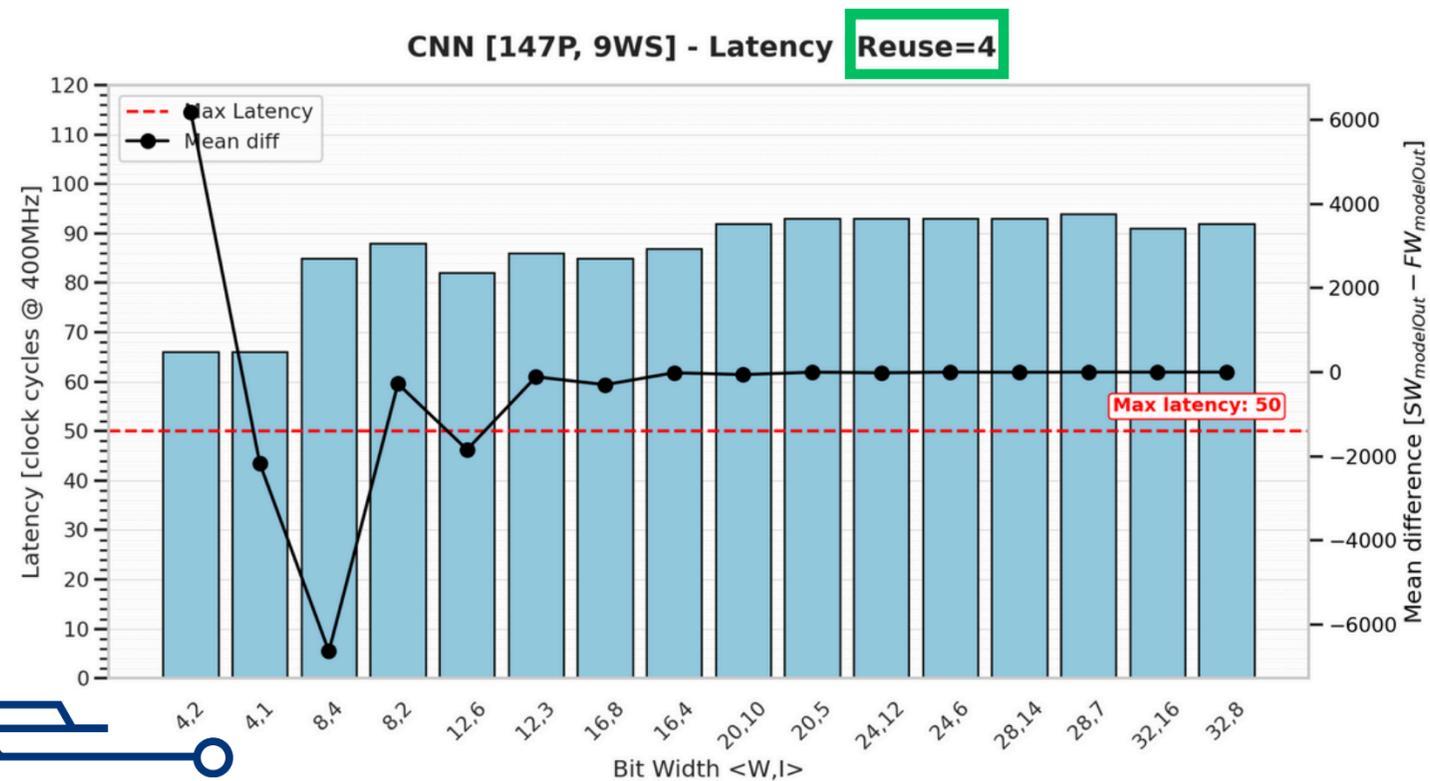
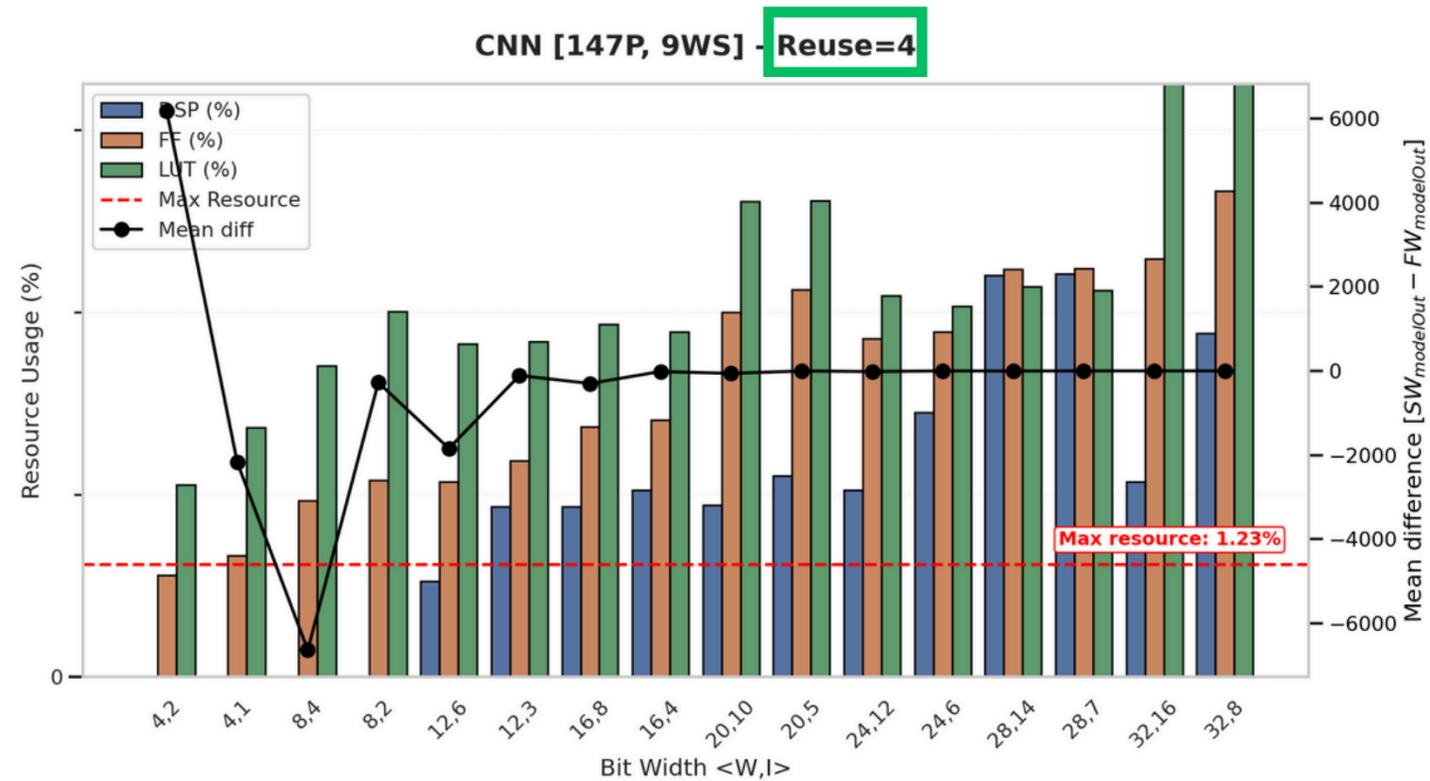
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**



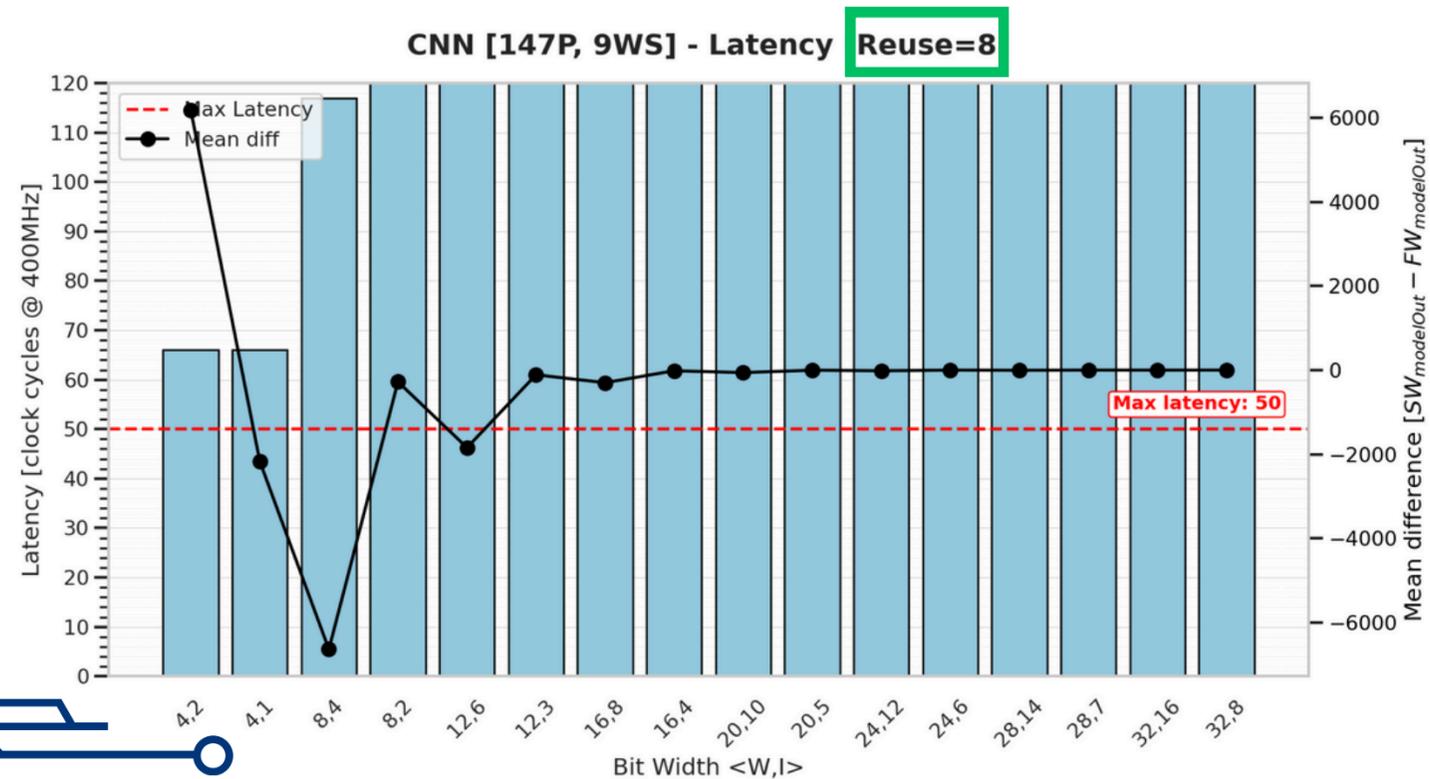
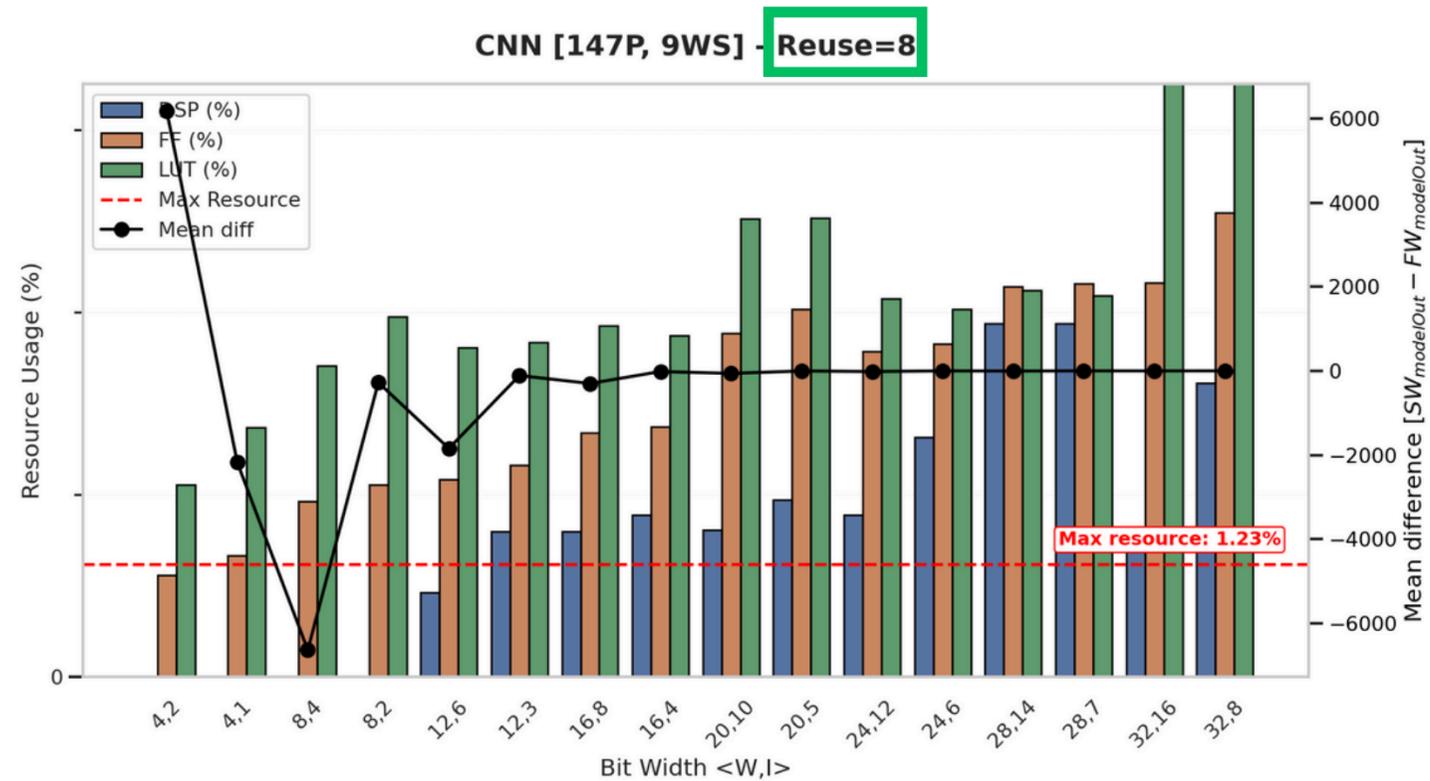
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**



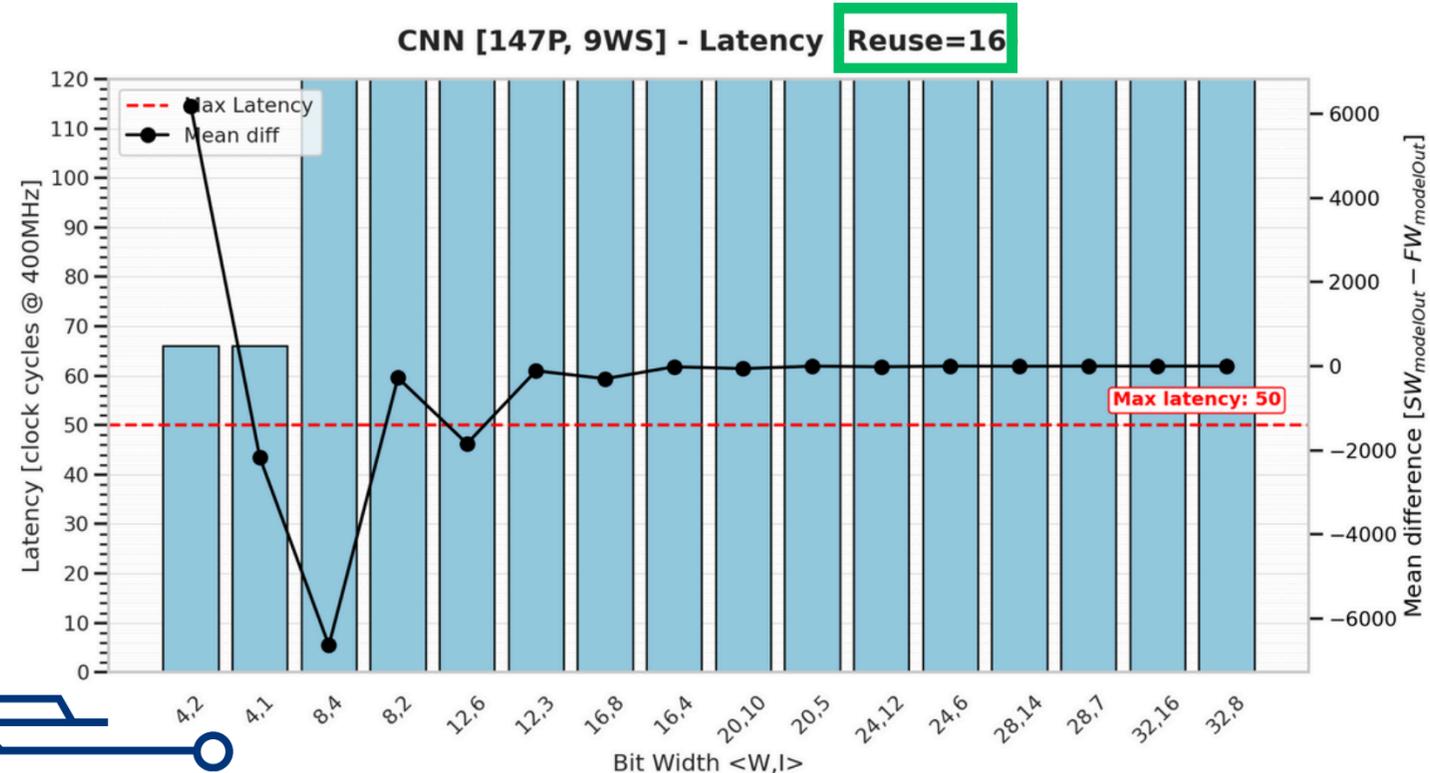
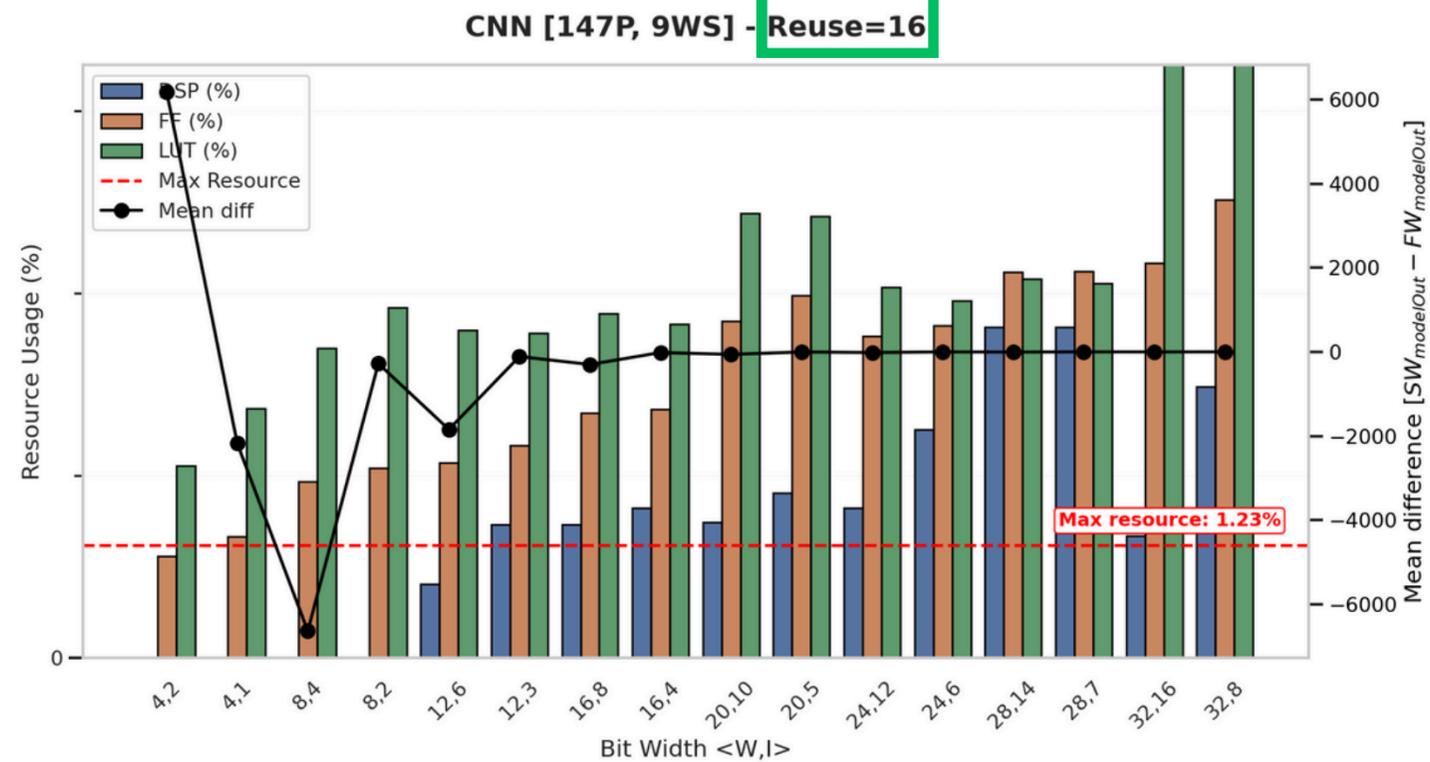
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**



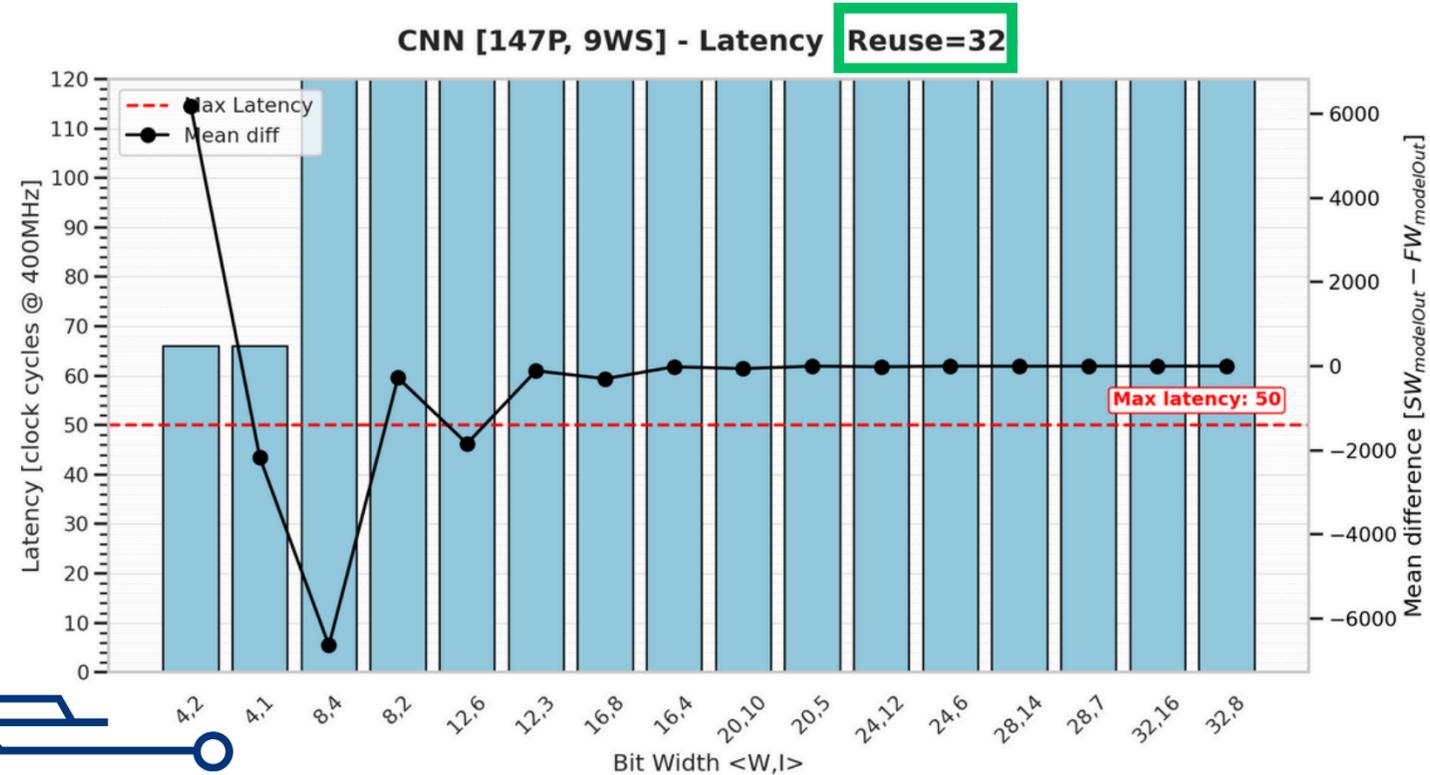
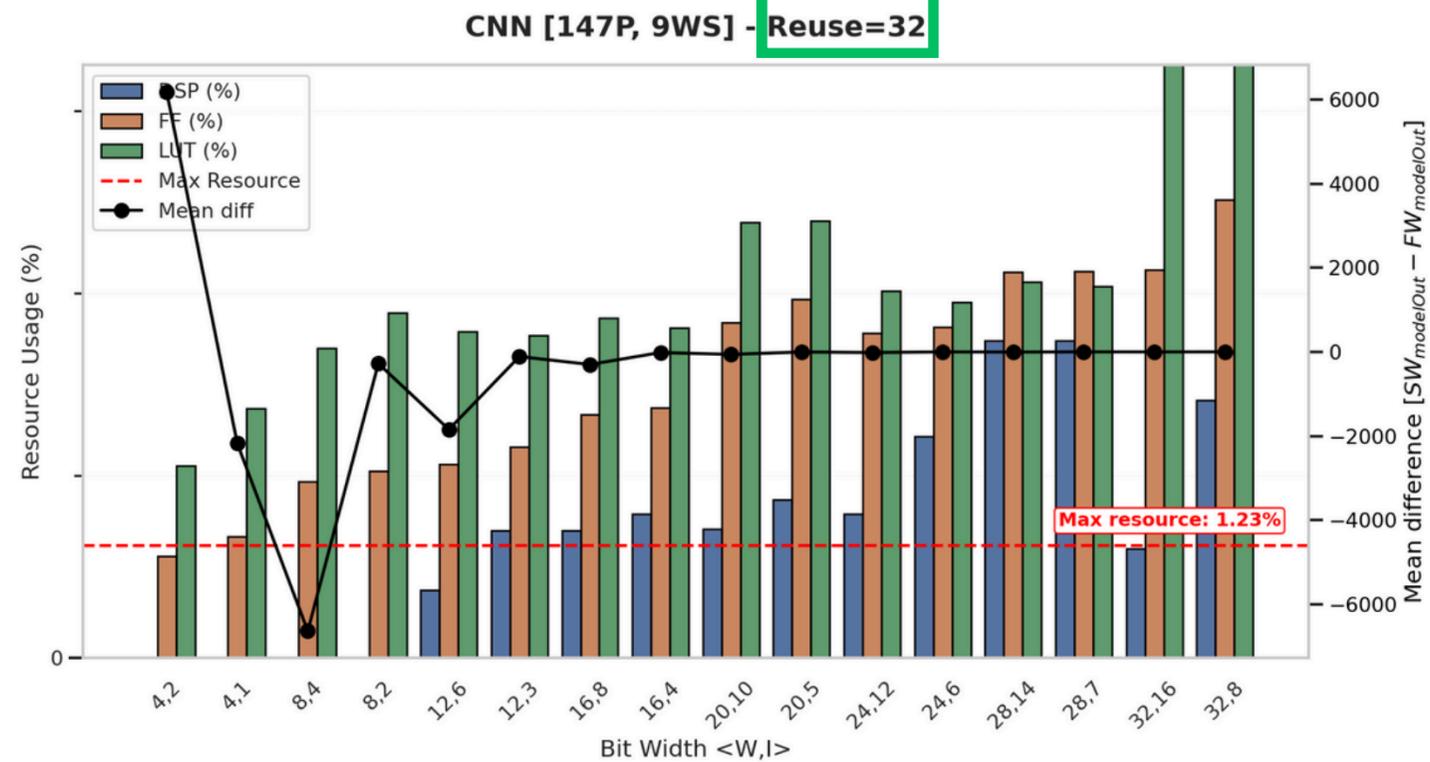
CNN 147P WS9

Firmware Prototyping



- The more reuse, the less resources, the more latency
- The more bits, the more resources and the more accurate
- Red line: maximum number of resources and latency per channel
- Increase number of test cases to look for the best implementation

**50 processing cycles =
5 BCs**

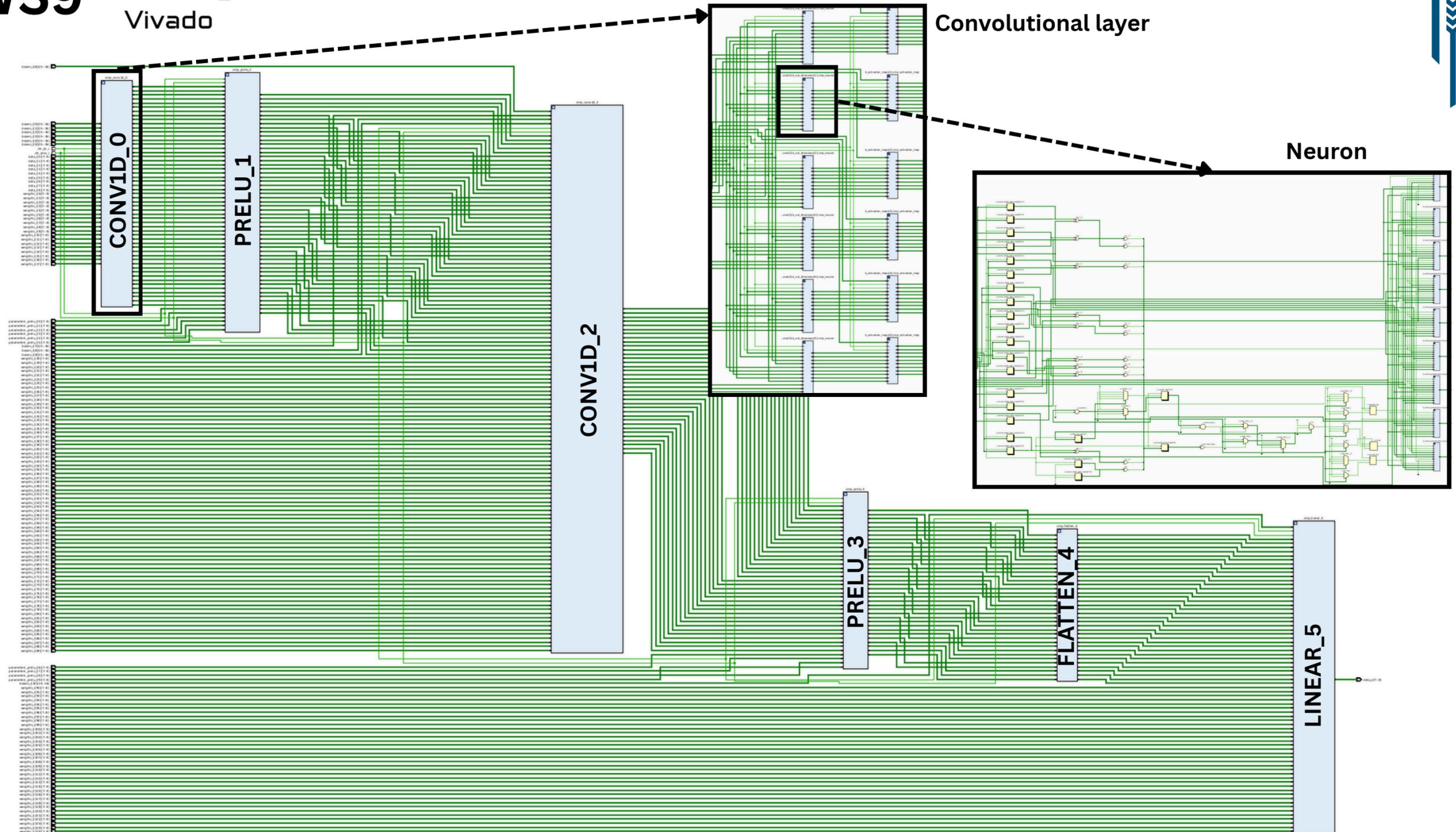


CNN 147P WS9



RTL Schematic

- RTL Schematic
- VHDL Code → Netlist
- Syntax check
- Visualizing the design
- Coded using VHDL 2008 standard
- Use of fixed point arithmetics
- Structural and hierarchical RTL code



CNN 147P WS9

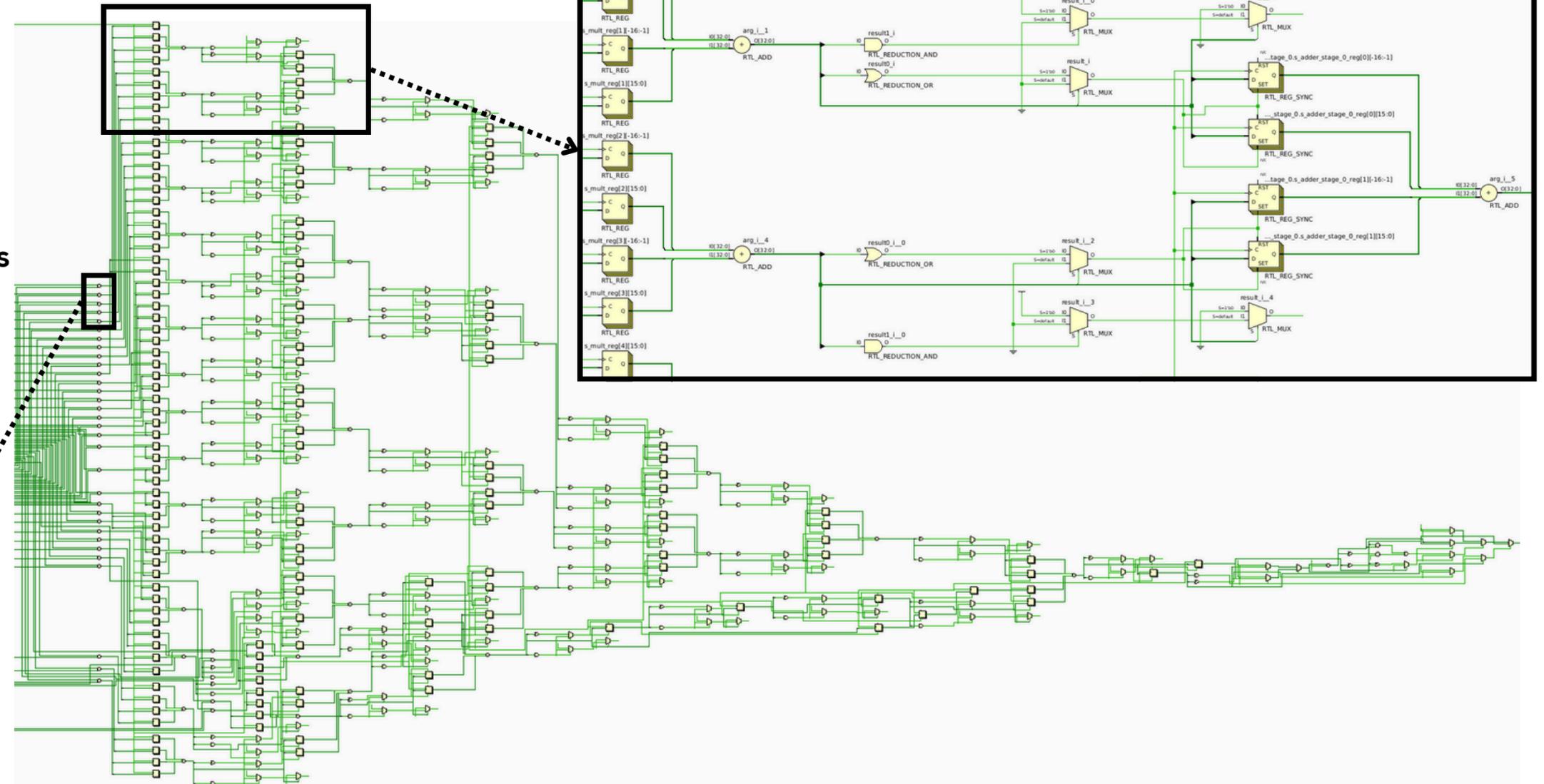
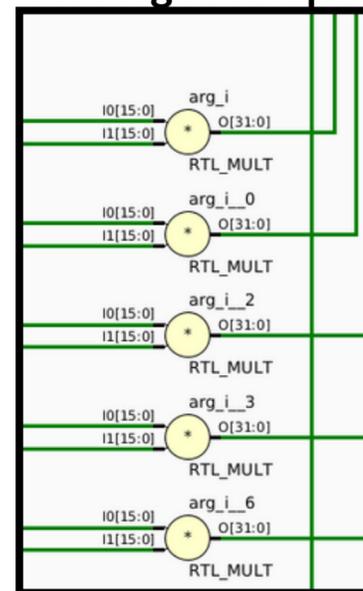


Component Example - Adder Tree

- Adder tree
- Multiply 2 vectors, and sum the resulting vector
- Latency optimized
 $L = 1 + \log_2(N)$
- Resource intensive (A lot of sums and mults)

$$r = \sum_{i=0}^{N-1} a_i b_i$$

First stage multipliers

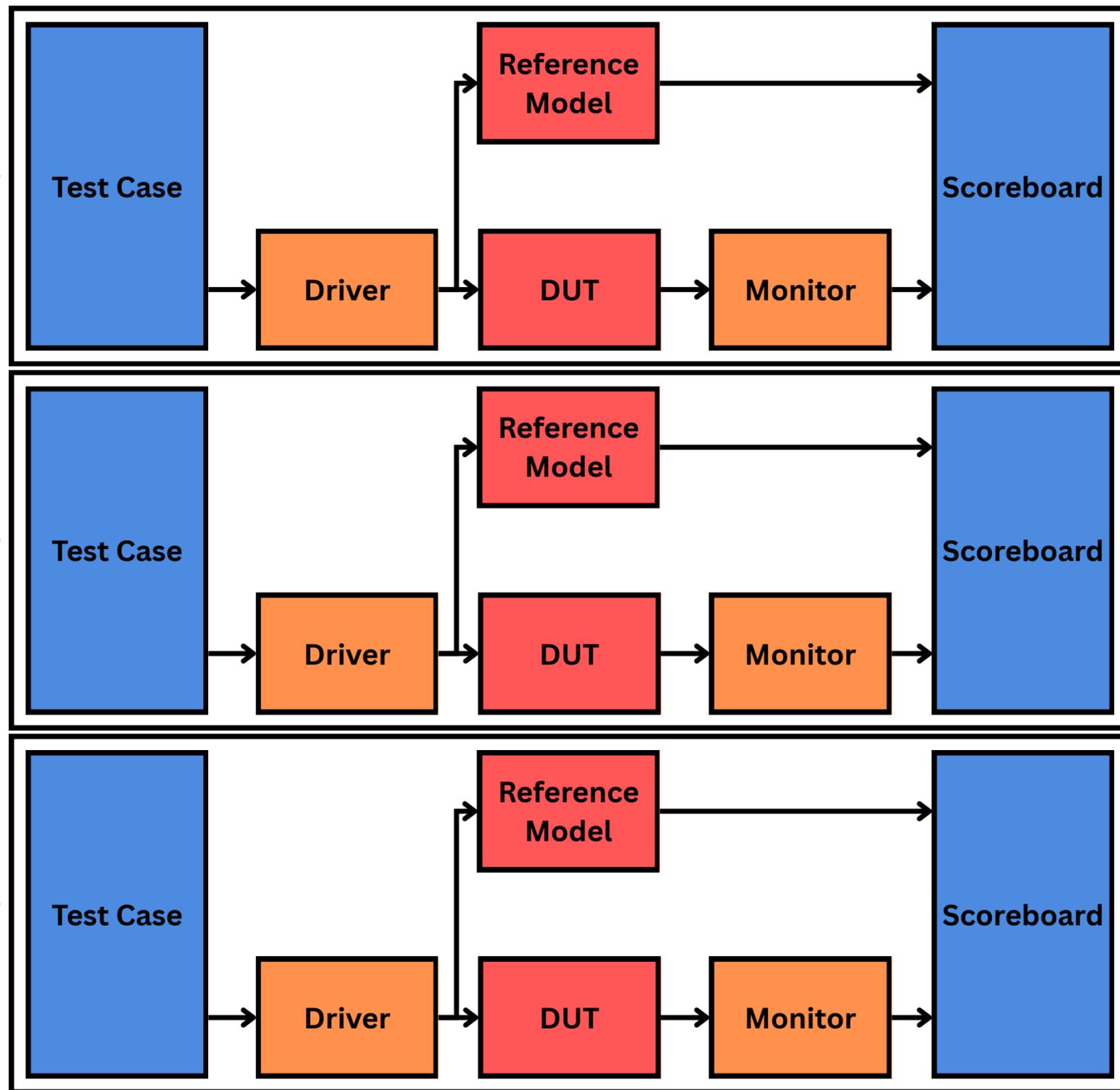
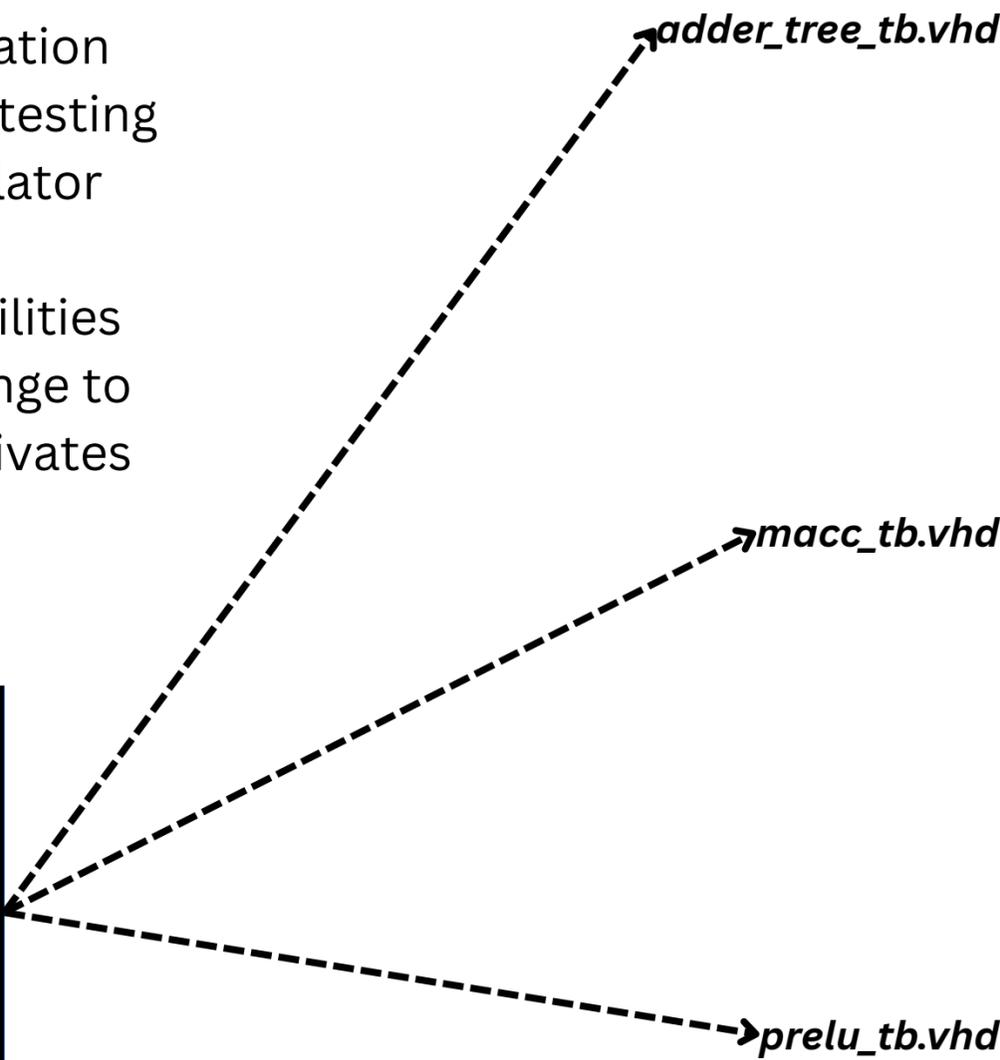


CNN 147P WS9

Unit Testing



- Formal verification
- VUnit for unit testing
- GHDL as simulator
- OSVVM for verification utilities
- Each new change to the RTL, reactivates the testing





Next steps

- Complete the FPGA chain (Synthesis, Implementation, STA, Bitstream, HW Verification)
- Study new ML algorithms, apply pruning and quantization
- Select the best algorithm for the signal reconstruction task
- Study implementation of different algorithms wrapping the signal reconstruction algorithm (noise cancelling)



Funding

“This work is supported by Ministerio de Ciencia, Innovación y Universidad con fondos Next Generation y del Plan de Recuperación, Transformacionales y Resiliencia (project - TED2021-130852B-100)”





Signal Reconstruction Firmware for ATLAS-TileCal

Jornadas Tecnológicas IFIC

16/09/2025

Francisco Hervás Álvarez, Alberto Valero Biot, Luca Fiorini, Héctor Gutiérrez Arance,
Fernando Carrió, Sonakshi Ahuja, Francesco Curcio



GOBIERNO
DE ESPAÑA

MINISTERIO
DE CIENCIA, INNOVACIÓN
Y UNIVERSIDADES



Financiado por
la Unión Europea
NextGenerationEU



Plan de Recuperación,
Transformación y
Resiliencia



AGENCIA
ESTATAL DE
INVESTIGACIÓN

