Technology Transfer Case

Novel Timing and Synchronization Strategies in Medical and Industrial Tomography

Application of White Rabbit Technology

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on behalf of the Instrumentation ITA Team

Instituto Tecnológico de Aragón

Agenda

- Our research
- Motivation for Timing techniques / technologies
- Reference distribution approaches
- White Rabbit for tomography
- Our Proof-of-Concept prototype

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FRONT-END AND DAQ ELECTRONICS

"Digital Electronics"

Our expertise covers also

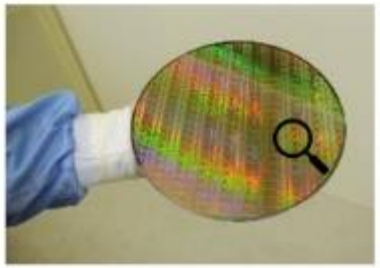
"Analog" Electronics

(See F. Arteche talk)

- Sensors / Transducers / Actuators
- Signal Conditioning – amplification, filtering, impedance matching, isolation…
- Data-Acquisition & Control Hardware – digitizers, ADCs, DACs, and embedded controllers
- Software & Firmware – DSP, algorithms for instrument control, data reduction, visualization, and automation

Our Technologies

Highly specialized electronic cards based on high performance SoCs



More than Moore devices

SoCs (MPSoCs, RFSoCs)

CPUs, FPGA, ADC, DAC, Memories…

Hardware, Gateware, Firmware, Software…

Our Application Domains

RF instrumentation

communications, industrial heating, quantum computing, EMI/EMC…

HEP Detectors (Electronics, Powering, EMI-EMC, Timing)

RF, tomography, timing, communications, medical imaging, synchronization…

Planes Complementarios

CAPA Centro de Astropartículas y Física de Altas Energías Universidad Zaragoza

IAXO

RADES

Technology Transfer from Science to other applications: Industrial, Medical…

Timing and electronics…

4D Detector Prototype based on LGAD sensors and ETROC2

Projects; CMS-ETL, DRD7, TOMULGAD-4D, PROTECT…

Collaboration;

Instrumentation: Timing and Synchronization

-Scalable timing/clocking distribution system

-Self calibrating and mitigating perturbations

-Using as Commercial Off-The-Shelf (COTS)

White Rabbit COLLABORATION

High Accuracy Default PTP Profile of IEEE1588-2019

Experience And Efforts With WR Technology

Preliminary Results Performance And Usability

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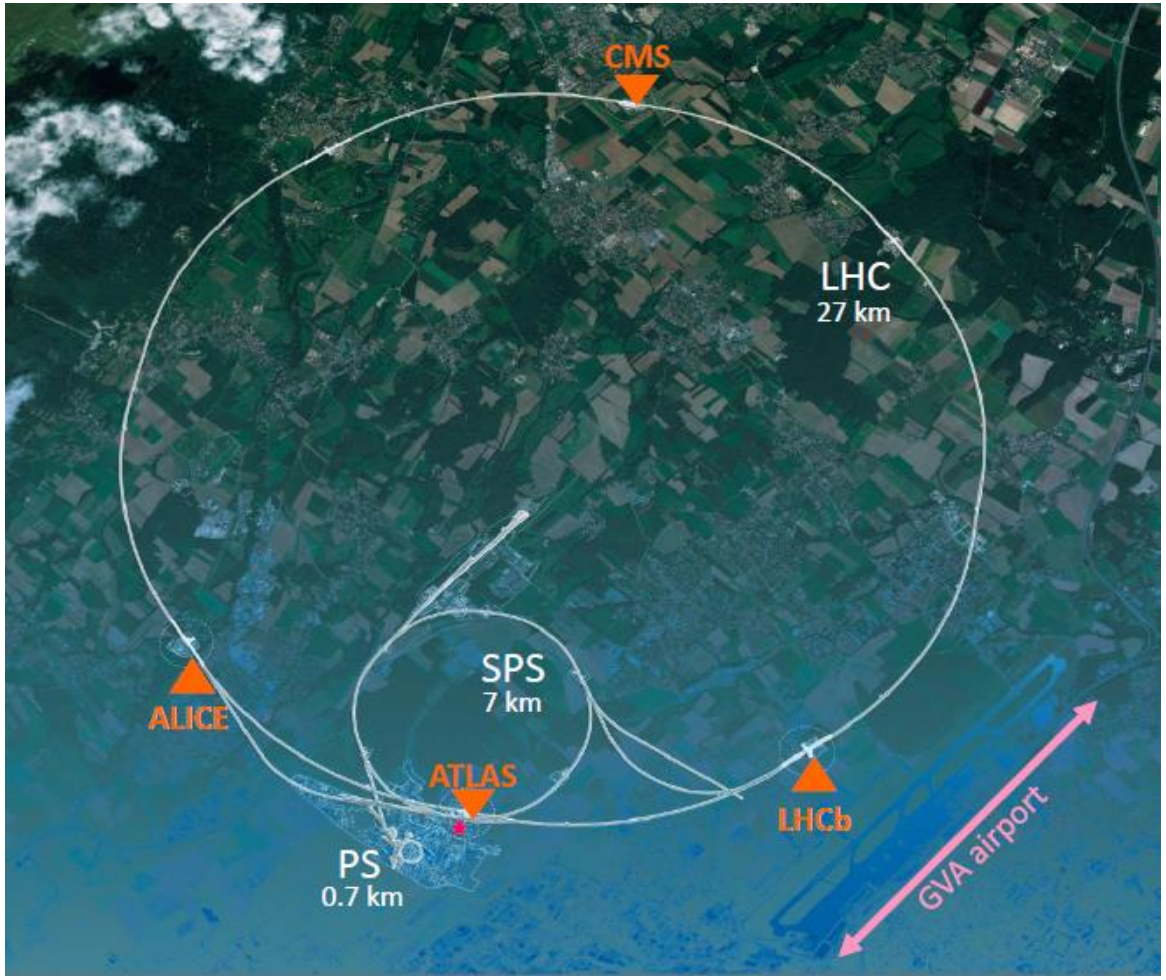
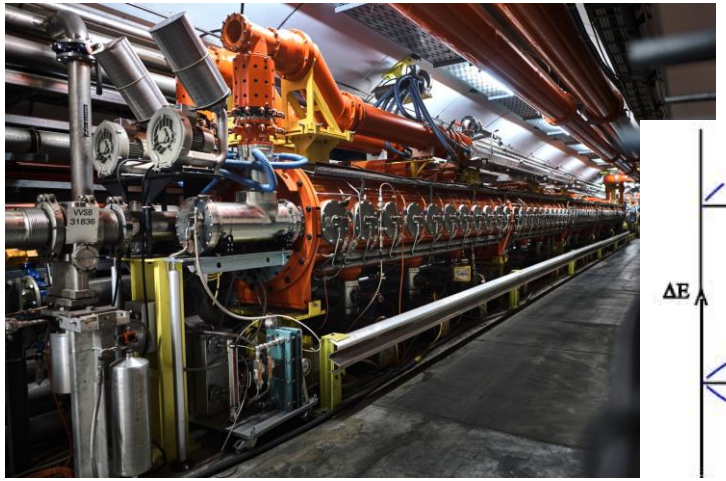
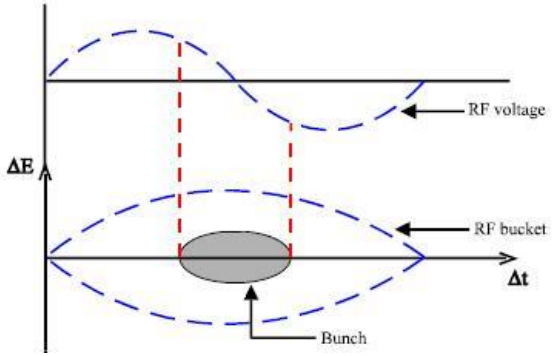
Accelerators: The need for a Reference

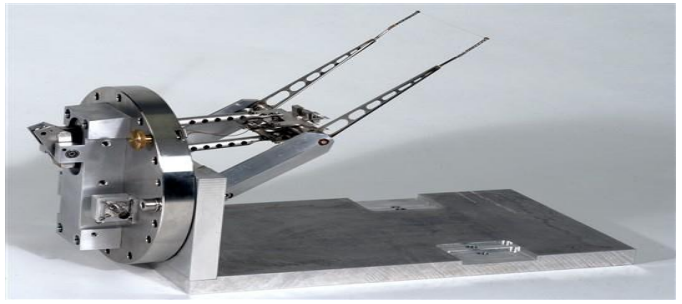


RF Acceleration





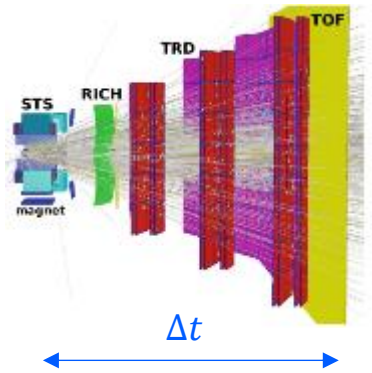
Beam Monitors (Size, position, intensity…)



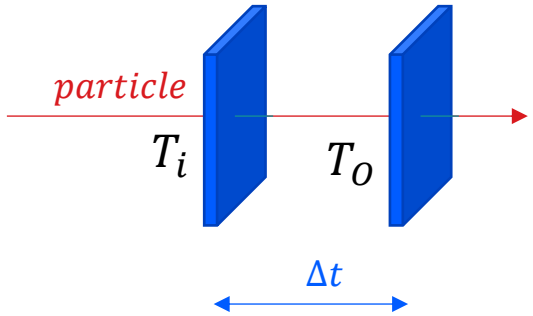
Reference: Controls / measurements need to be synchronized

Detectors; need for Reference in Time Measurements

Colliders



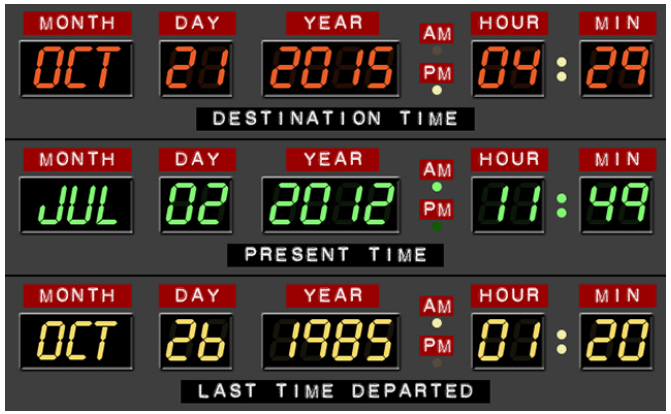
Multi-plane detectors



Absolute notion of time

Both times T_o and T_i need a common REFERENCE

How do we measure Time?

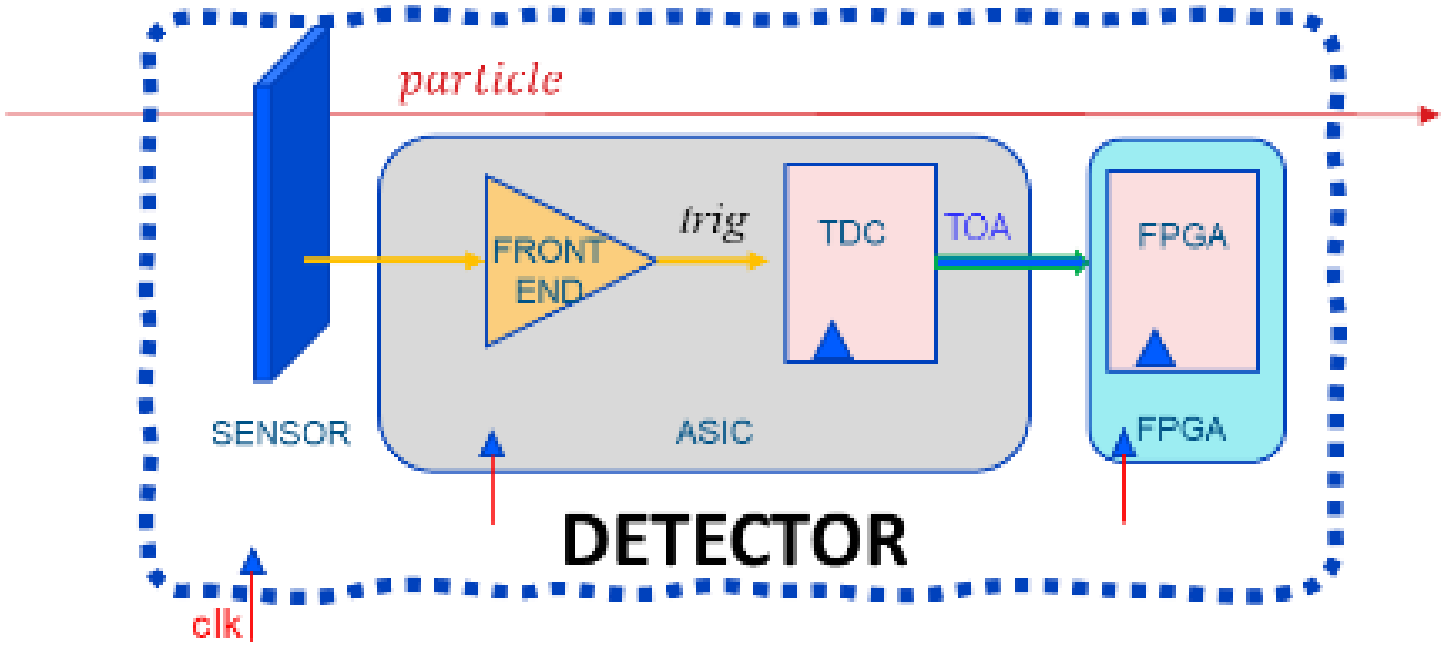


We usually refer to a Time Difference

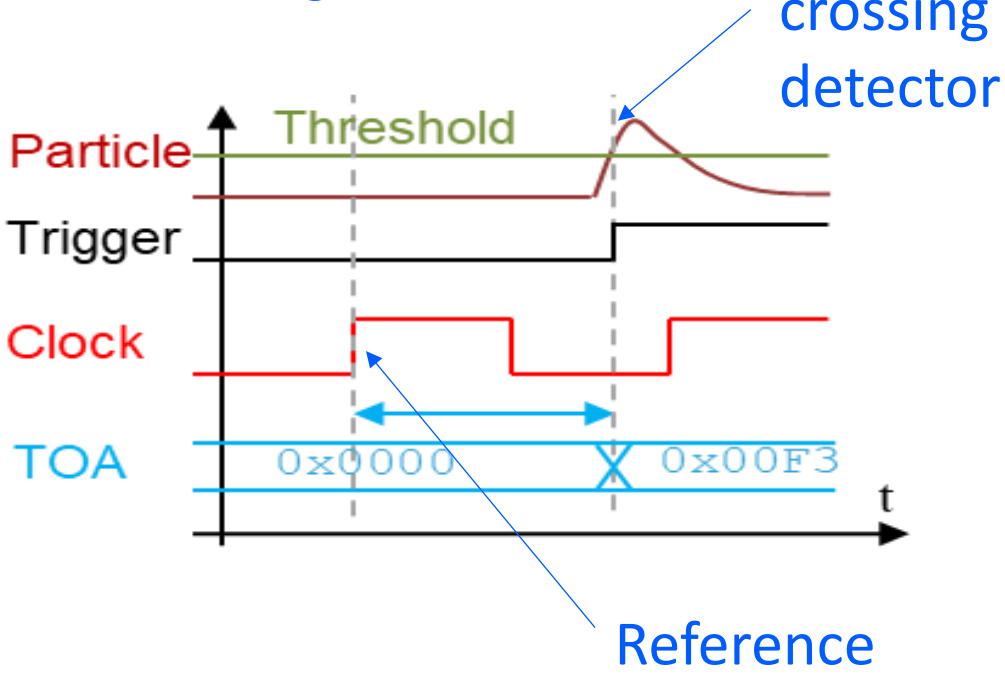
$\Delta t = T_o - T_i$

Timing: The need for a Reference

System Architecture



Chronogram….



Absolute time

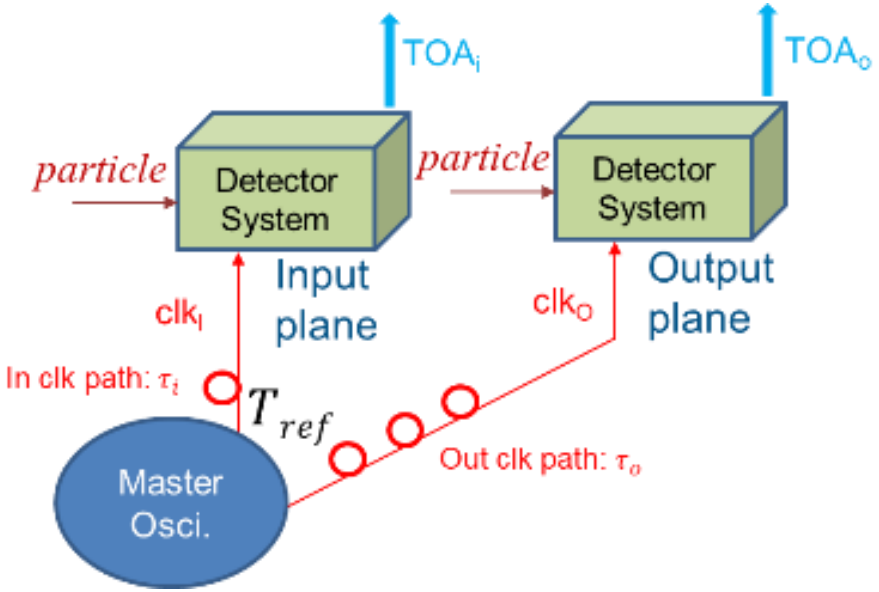
$$T_x = T_{ref\ x} + TOA_x$$

Multiple Detectors

T_{ref} needs to be a common synchronized reference among all nodes

Timing: The problem when you gets larger…

Multiple Detection Planes

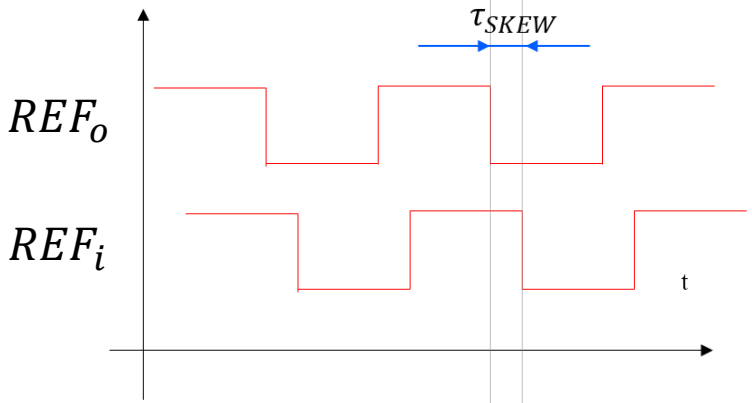


Absolute time concept:

T_{ref} / clock phase

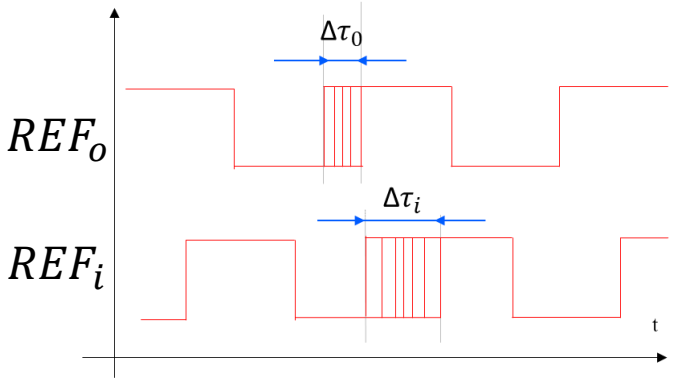
Time and Space maters… propagation

SKEW *You can Calibrate it*



$$\tau_{SKEW} = (T_{refo} - T_{refi})$$

JITTER *Unavoidable*



$$\Delta\tau_{jitter} = (\Delta\tau_0 - \Delta\tau_i)$$

Technologies for Reference distribution / synchronization

The Local Oscillator and Distribution Network

“Classic” distribution networks

“Open loop” systems that turned a complex “Closed Loop” system

Cope the problems at Design Phase

High Accuracy Default PTP Profile of IEEE1588-2019

White Rabbit

CERN

Based on

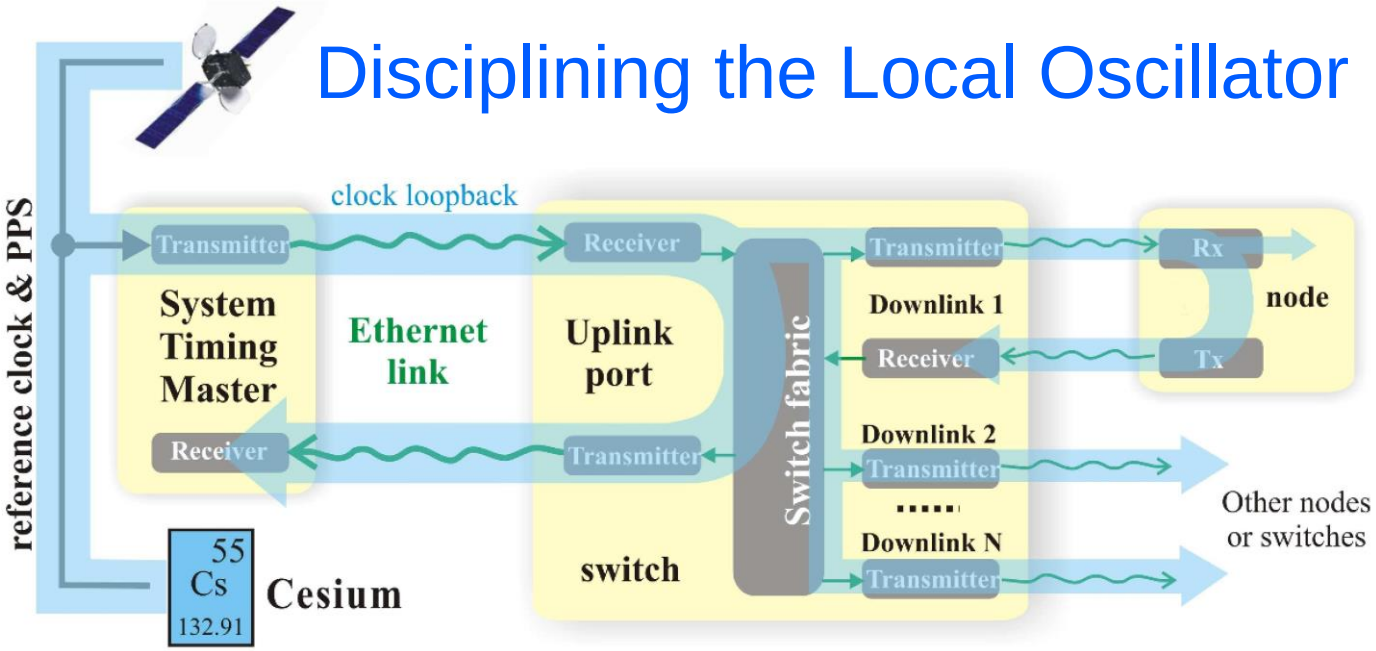
- Gigabit Ethernet over fibre
- IEEE 1588 Precision Time Protocol

Enhanced with

- Layer 1 syntonisation
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model

White Rabbit Principles

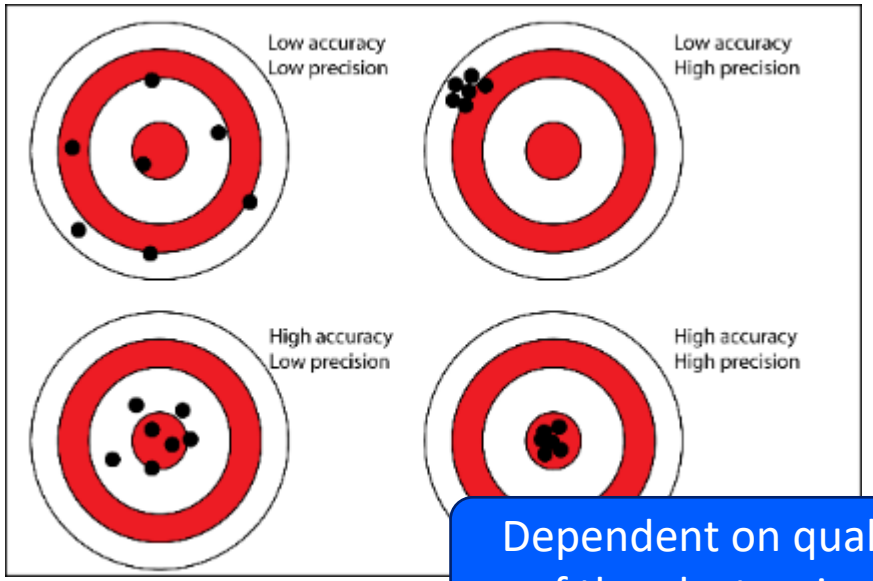
Disciplining the Local Oscillator



Clocking Performance

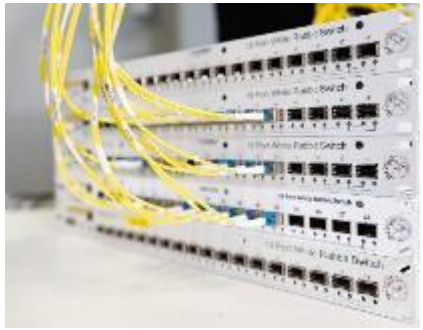
Accuracy: repeatability of the reference edge in the slaves with respect to an ideal master (skew)

Precision: dispersion of reference edge (jitter)

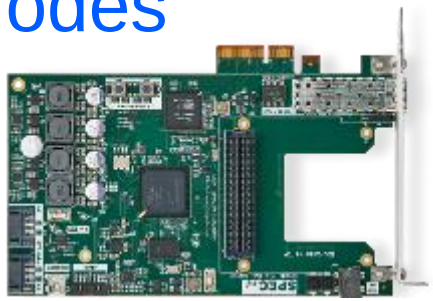


Dependent on quality of the electronics…

WR Switches



Nodes



Hardware; Carrier, FMC

Gateware; WR PTP Core

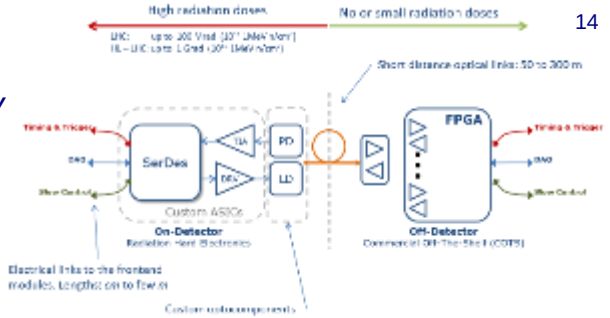
Firmware; Controls C code

And now…
Our 4D Detector

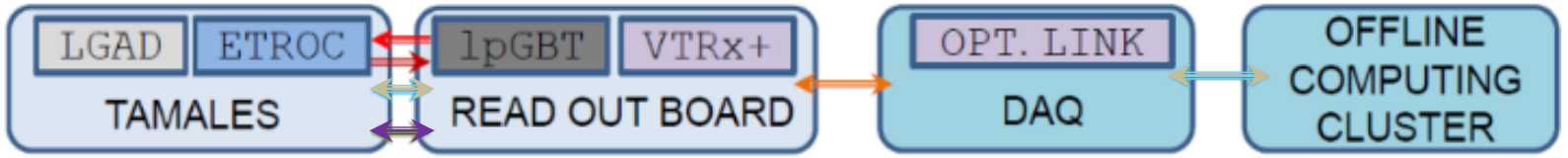
Base on ETROC2 and…

The ETROC2 Based Electronics…

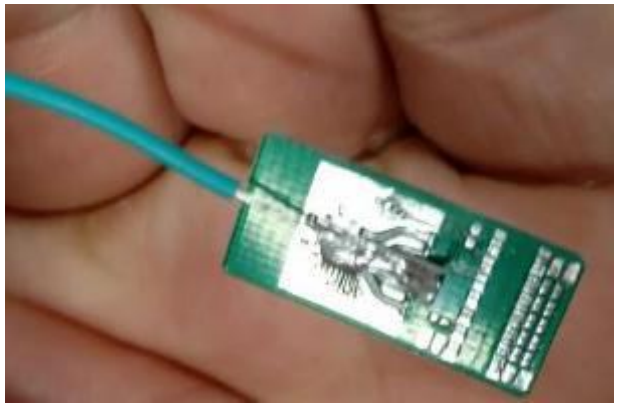
CERN GBT and VTR ASIC Family



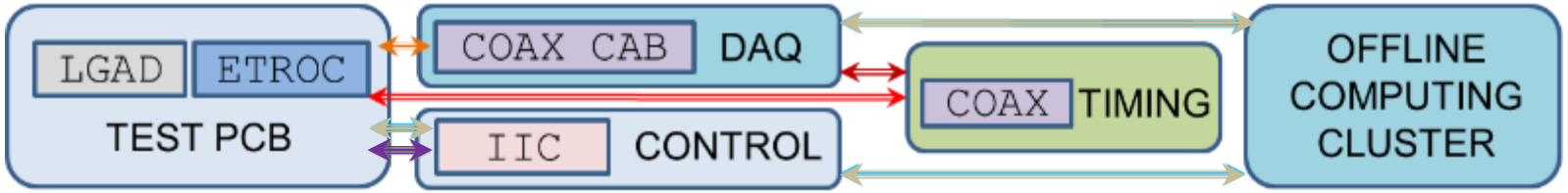
CMS – ETL Electronics



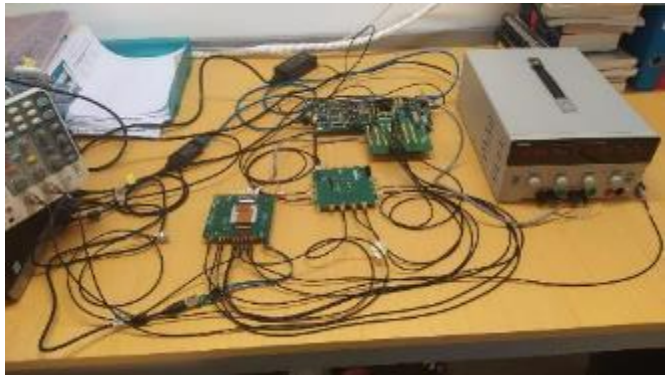
Based on CERN GBT ASICs (optical data/clock link)



TOMULGAD-4D Electronics

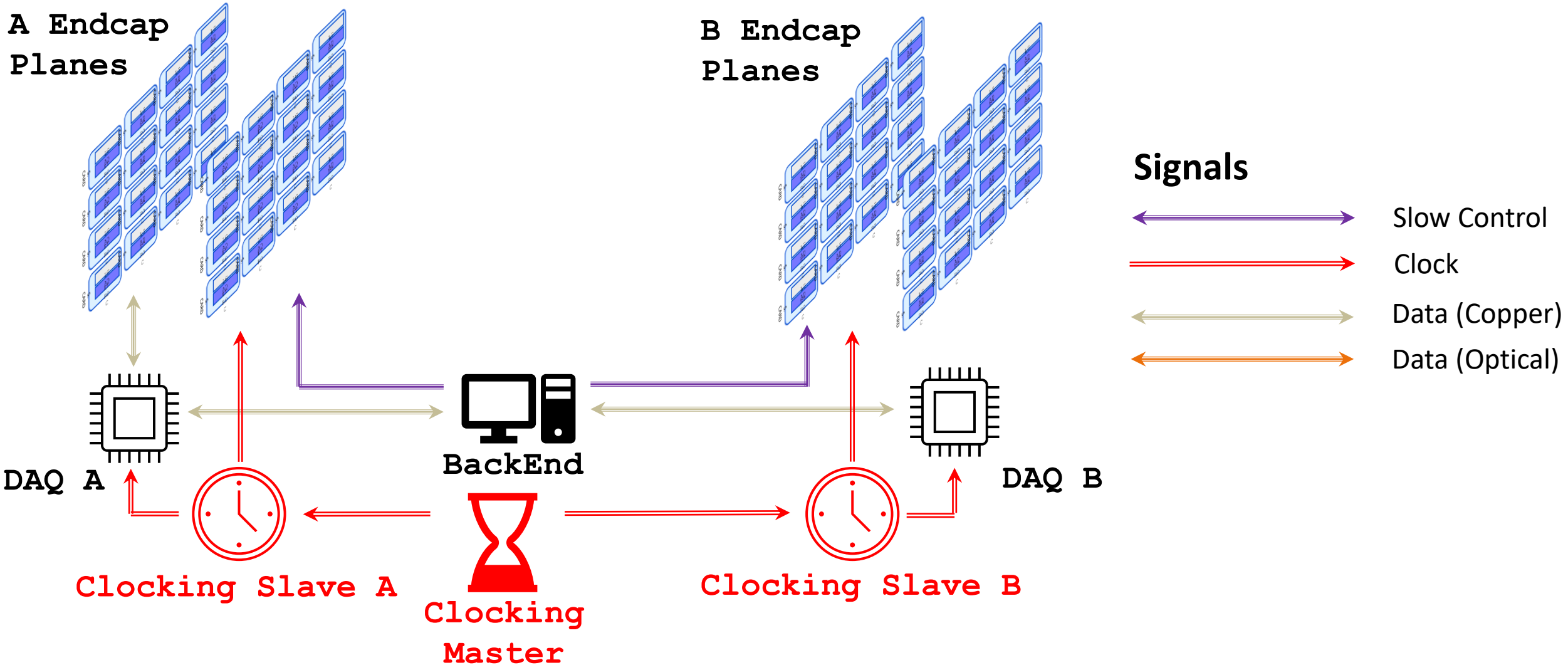


No access to GBTs… we decouple data, clocking, controls

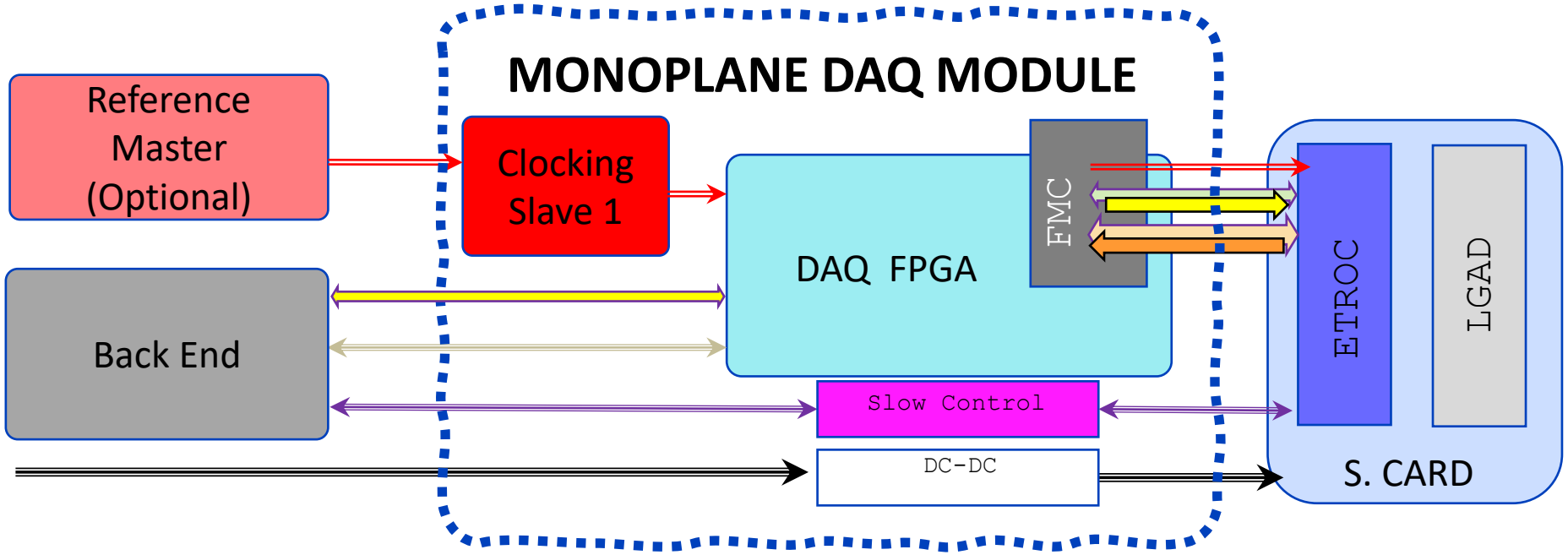


↔ clocking ↔ controls ⇆ data

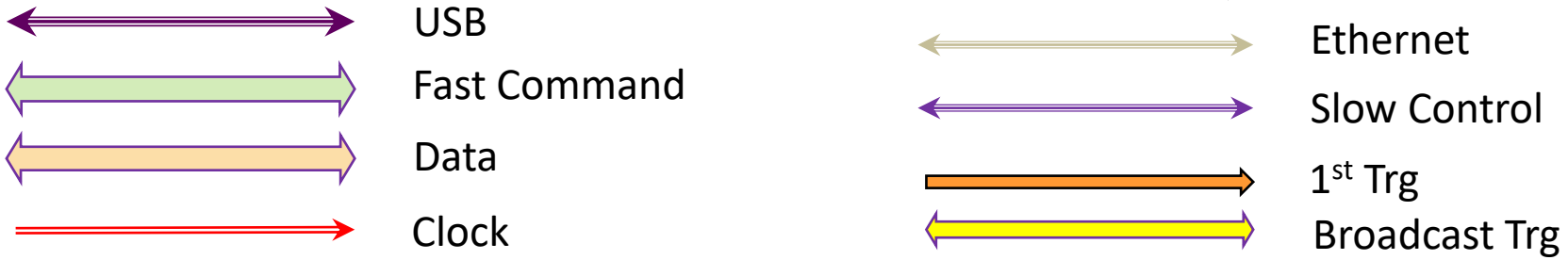
The Multiplane Detector Architecture



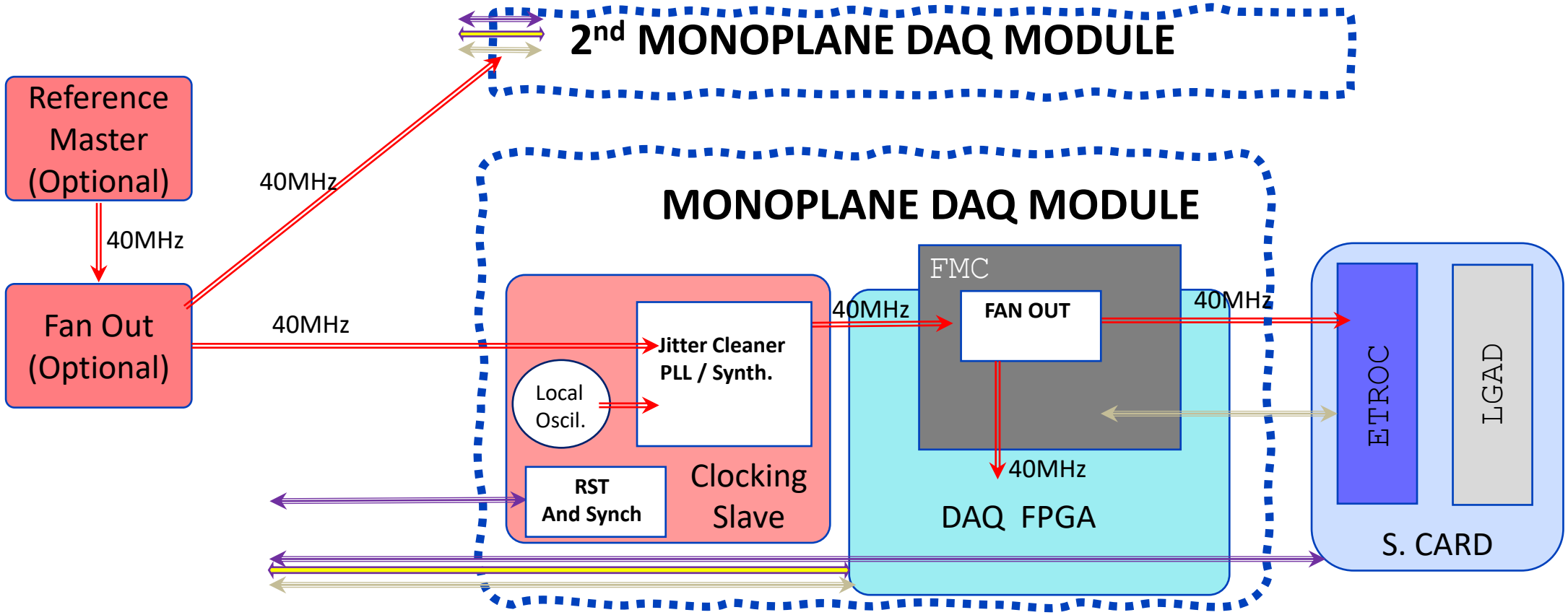
The Detection Plane Reference Architecture



Signals



Open Loop Clocking Architecture with multiple Planes



Signals

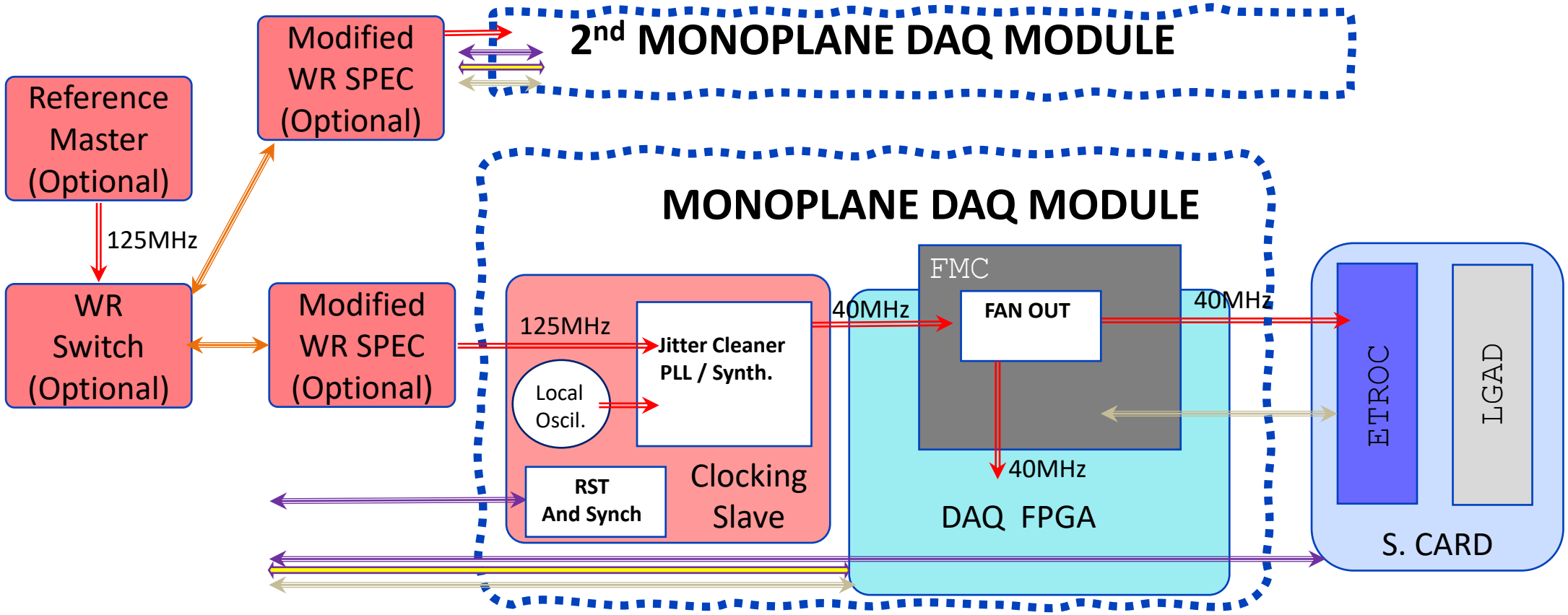
Slow Control

Data (Copper)

Trigger (local/global)

Clock

Close Loop WR based Clocking Architecture



Signals

Slow Control

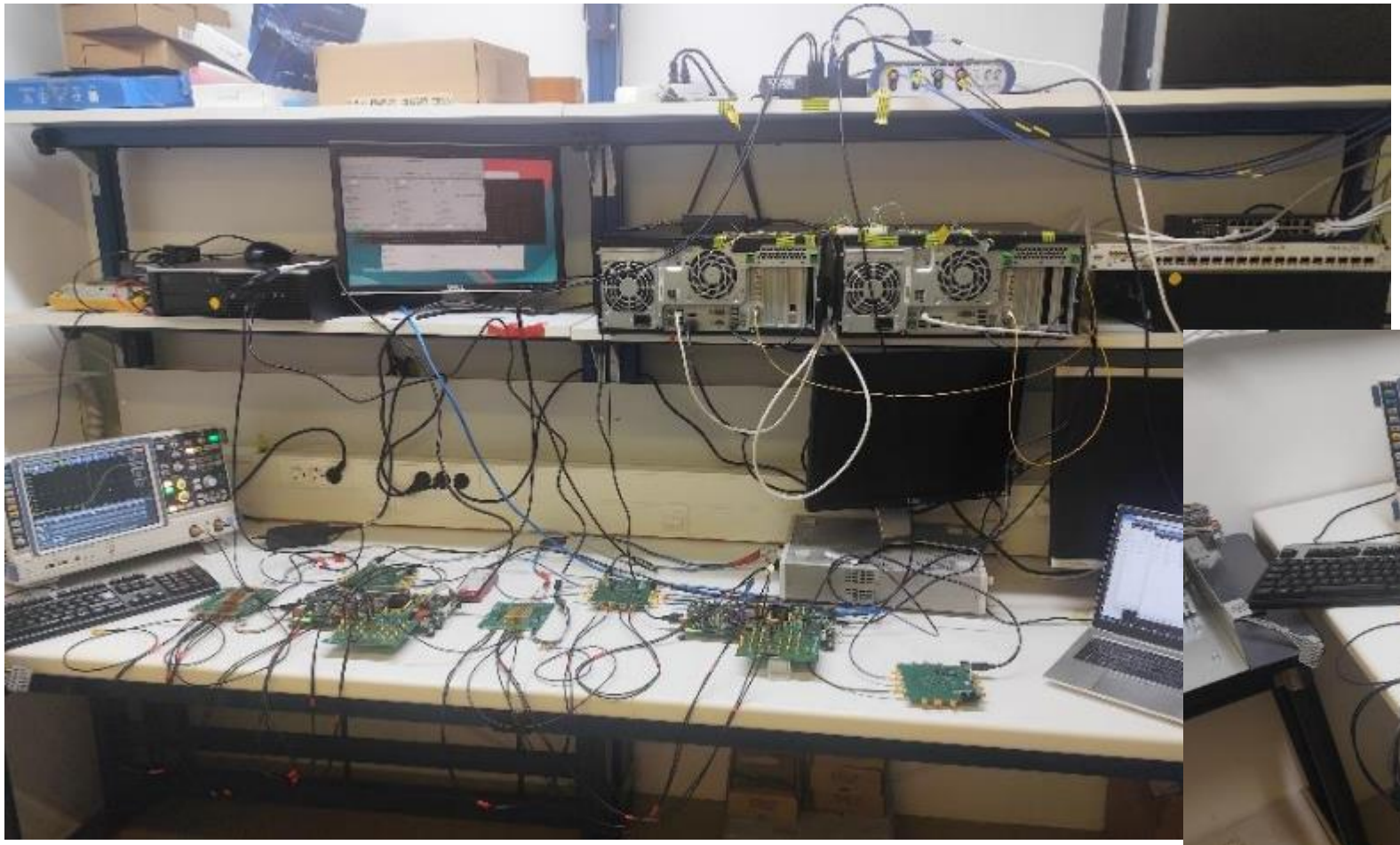
Data (Copper)

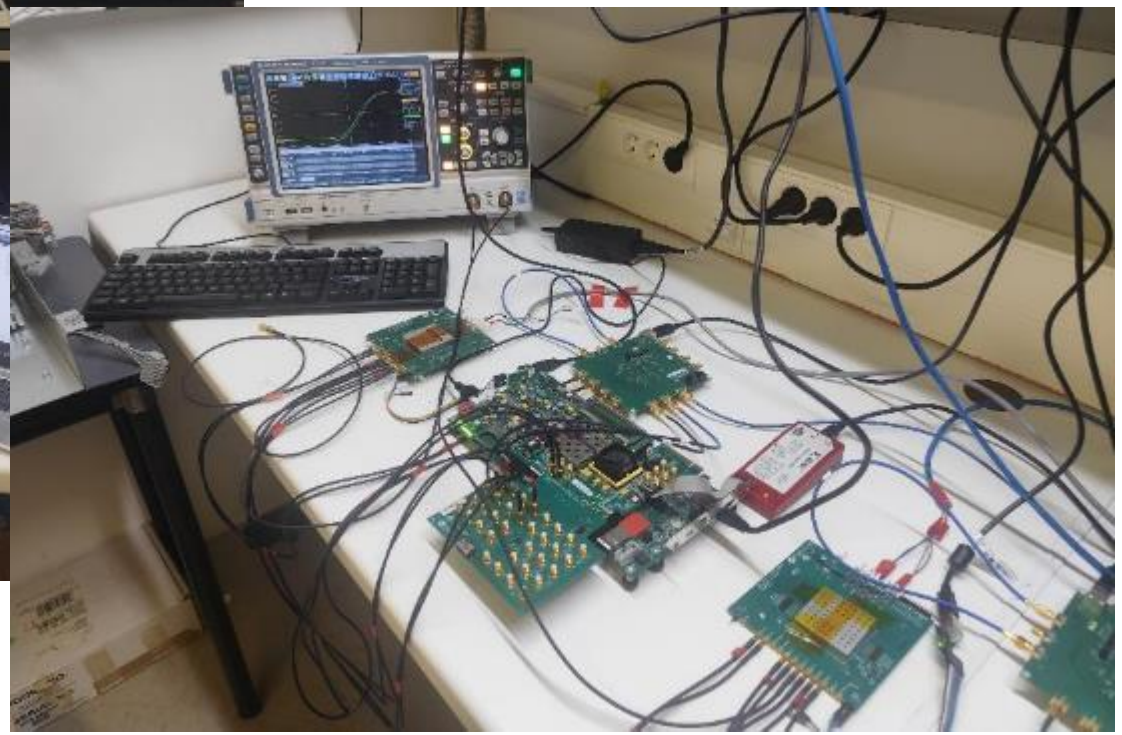
Trigger (local/global)

Clock

Data (Optical)

The meshy setup…

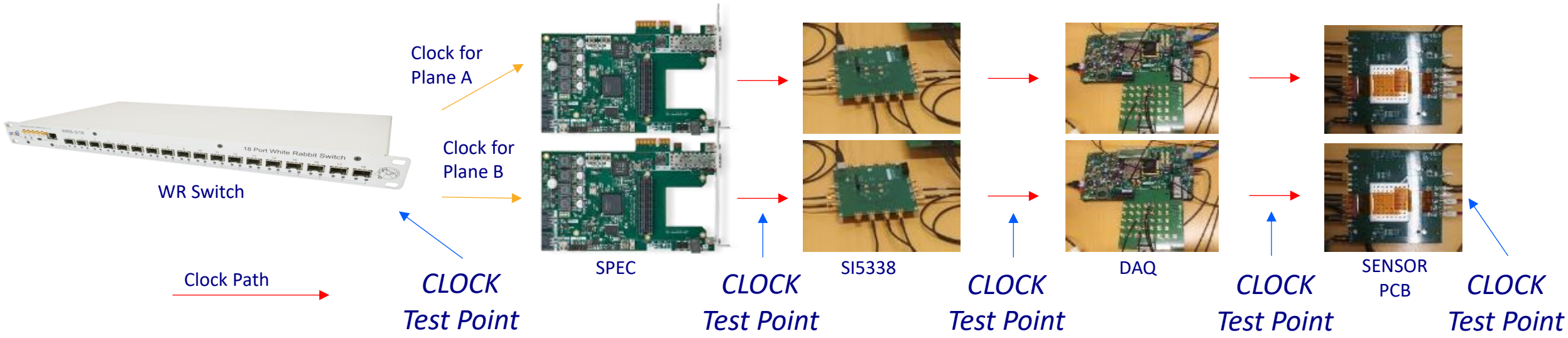




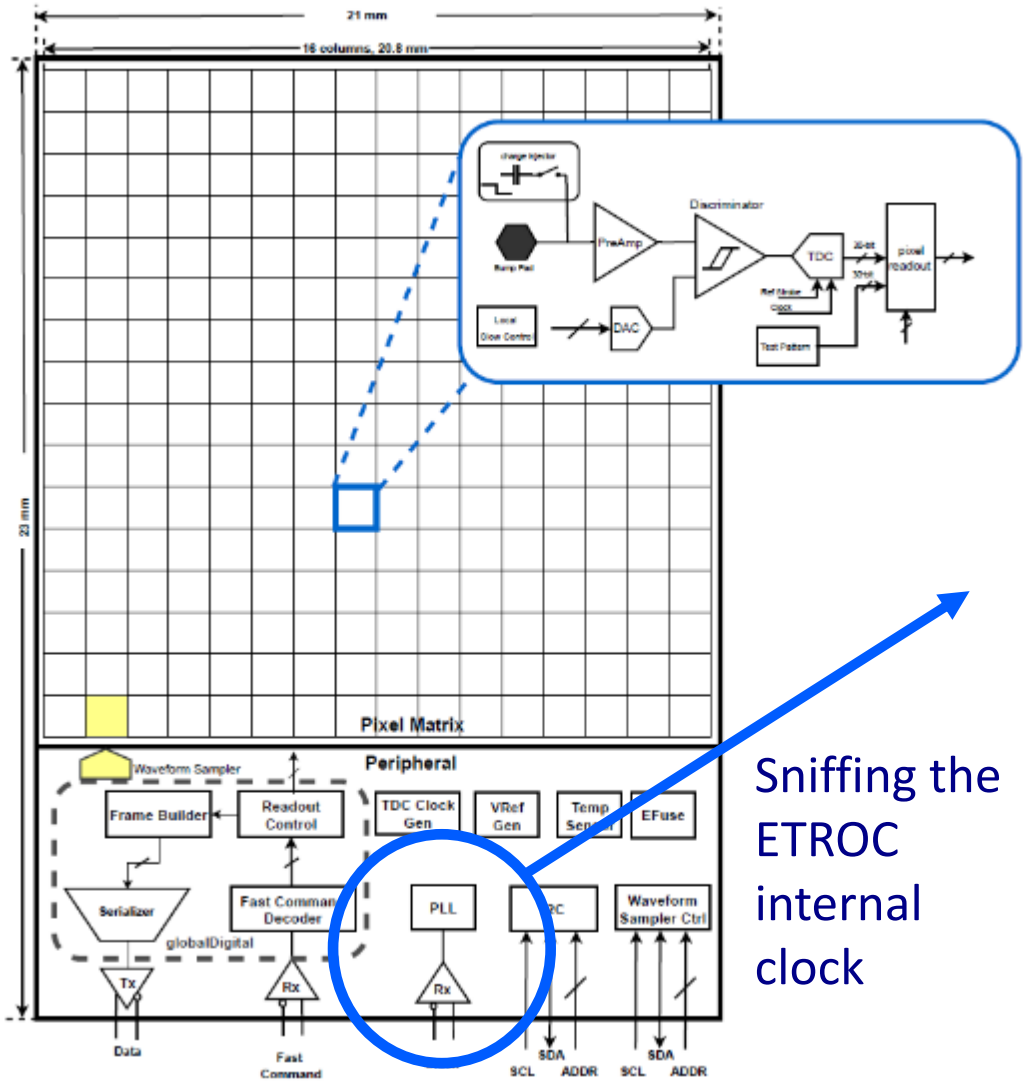
The WR initial evaluation

Phase A: Coaxial clock distribution with external clock synthesizer (40 MHz) using the Si5338 as 1:N fanout (transparent)

Phase B: WR based clock (125MHz) slaves using the SI5338 to synthesize and derive 40 MHz outputs to DAQ and sensor card



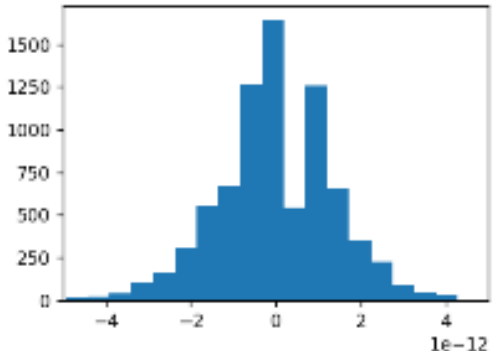
TIE Jitter Performance; 40 MHz analog vs WR based distribution



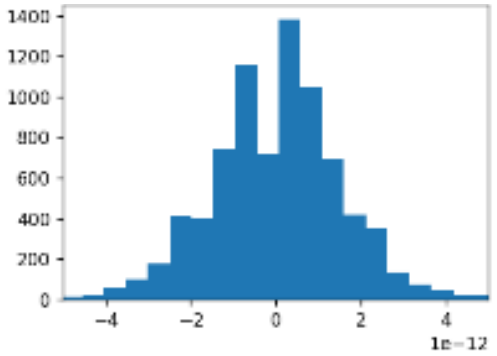
Sniffing the ETROC internal clock

40 MHz Ideal Clocking

Detector Plane A



Detector Plane B

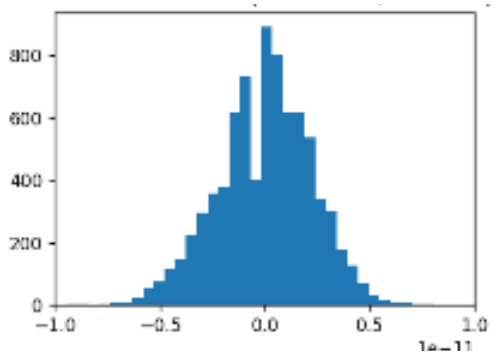


Plane A RMS jitter = 1.3658 ps

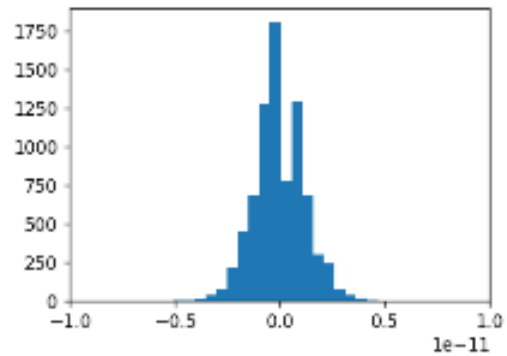
Plane B RMS jitter = 1.504 ps

White Rabbit Based Clocking

Detector Plane A



Detector Plane B

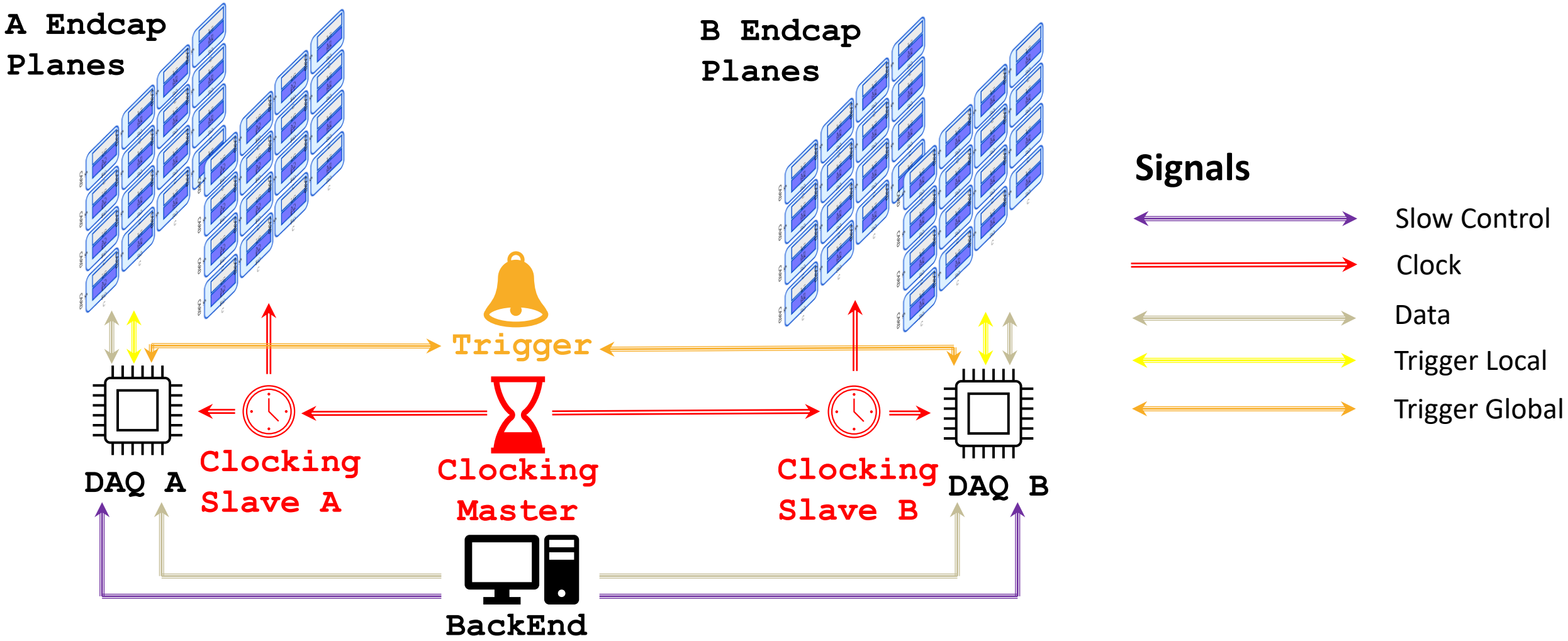


Plane A RMS jitter = 2.2489 ps

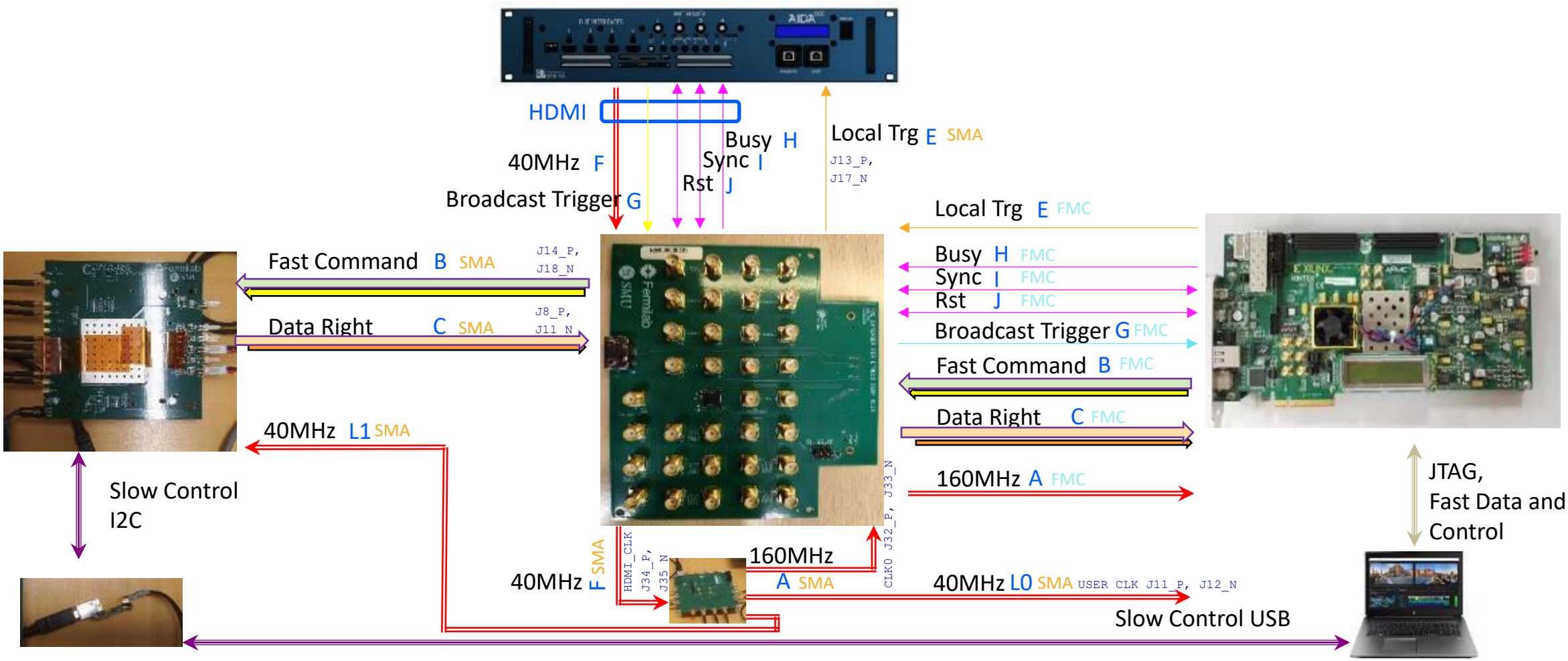
Plane B RMS jitter = 1.1864 ps

Close to Golden Reference System

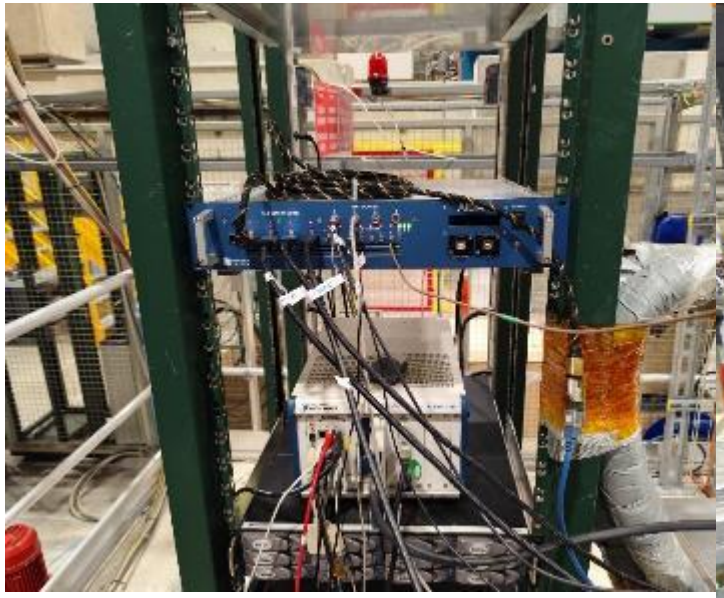
System Level Validation: The Multiplane Detector Architecture

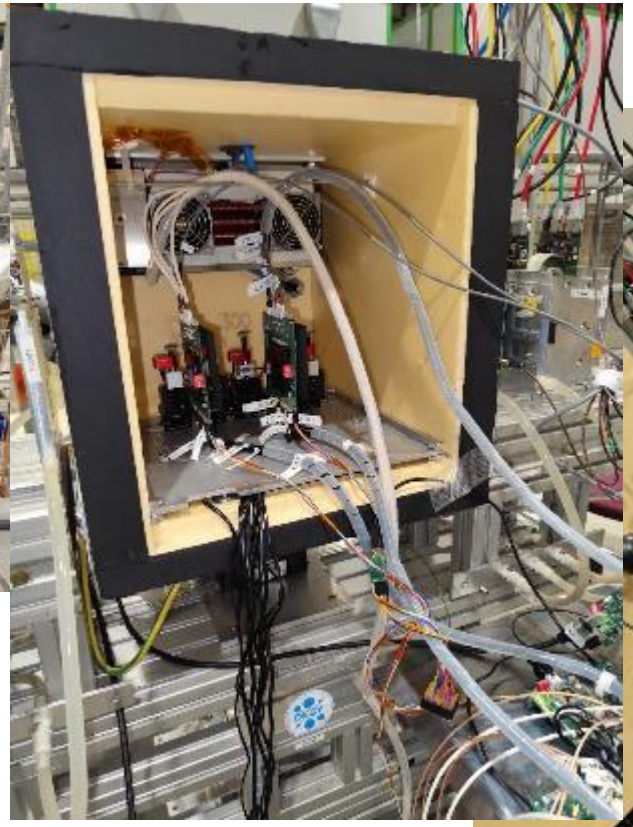


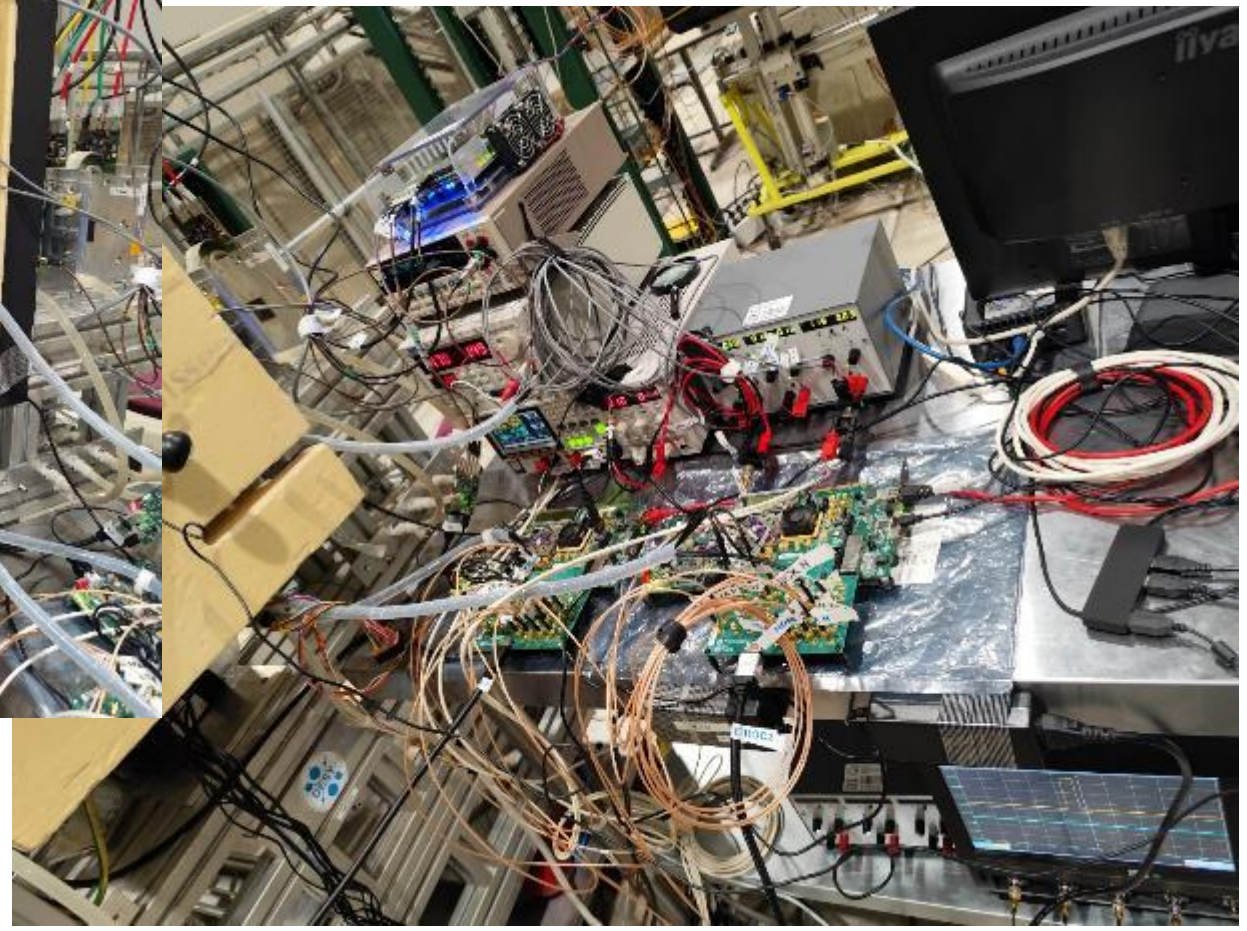
VALIDATION: TLU CLK@40MHz With 2 DAQ, 1 ETROC, 1 Data channel



Multiplane test, Clocking, Synchronization and Performance



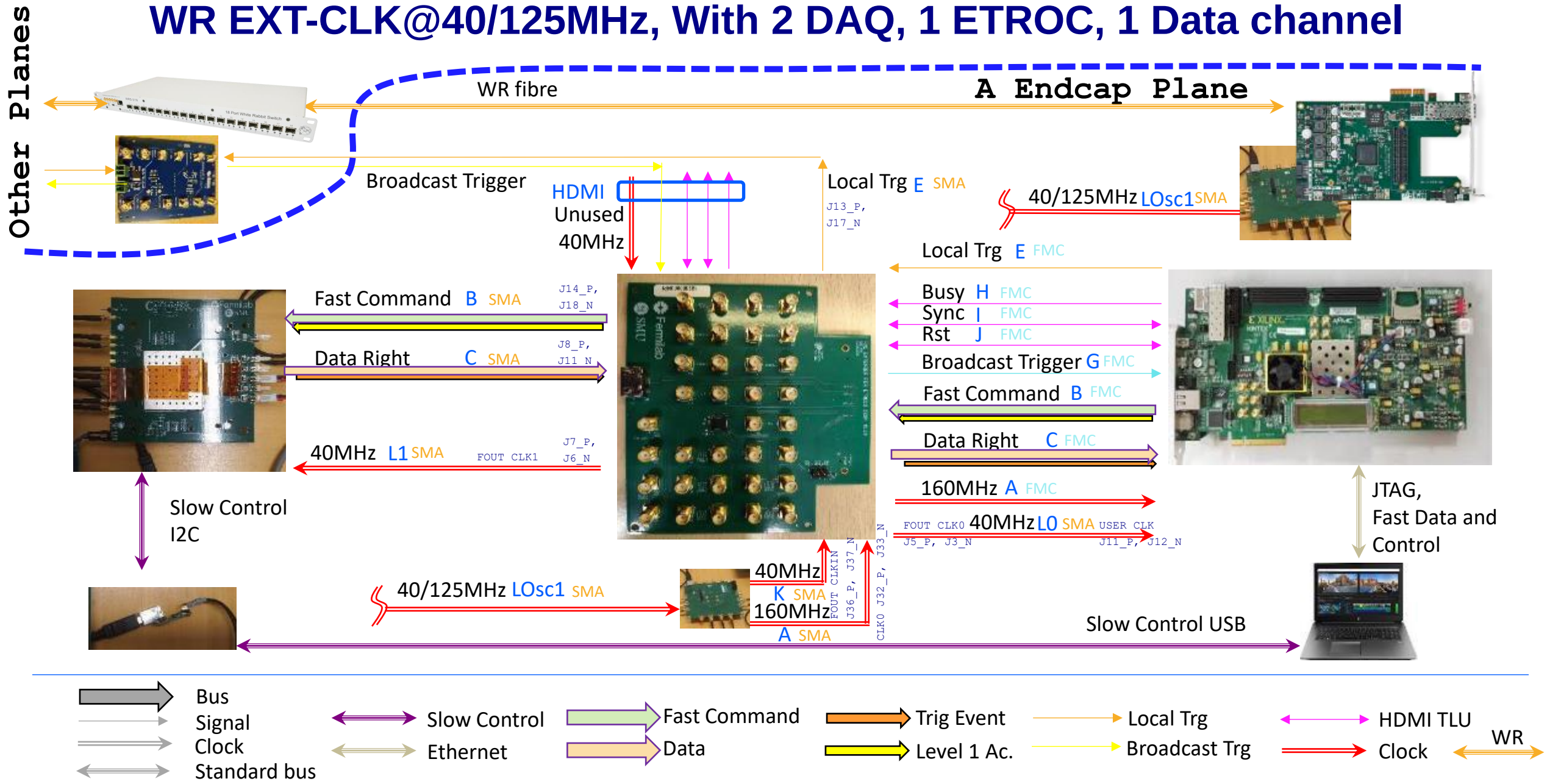




40 MHz Analog Clocking

AIDA TLU for distribution and Multiplane Synchronization

WR EXT-CLK@40/125MHz, With 2 DAQ, 1 ETROC, 1 Data channel



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¡Muchas gracias!

DAQ Interfaces