Advanced Instrumentation for Next Generation HEP Experiments

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IFIC – Instituto de Física Corpuscular

IFIC → Joint center between:

- Spanish National Research Council
- University of Valencia

Funded in 1950, it is a Physics Institute, covering activities in:

- **Particle Physics**
- Nuclear Physics
- Astroparticle and neutrino Physics
- Medical Physics
- GRID

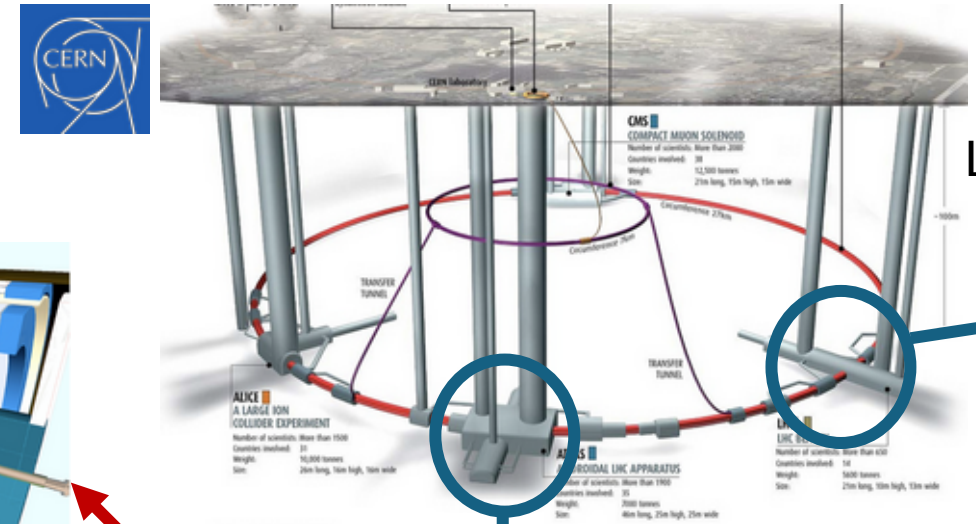
Approaching 400 members

Awarded with the ‘Severo Ochoa’ accreditation as center of excellence in Spain

IFIC – Instituto de Física Corpuscular

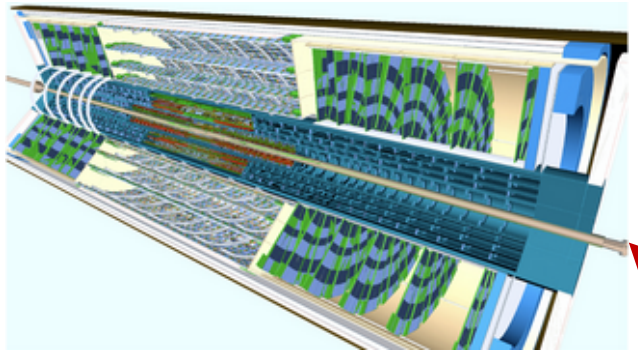
Instrumentation Activities at IFIC

IFIC at CERN's LHC

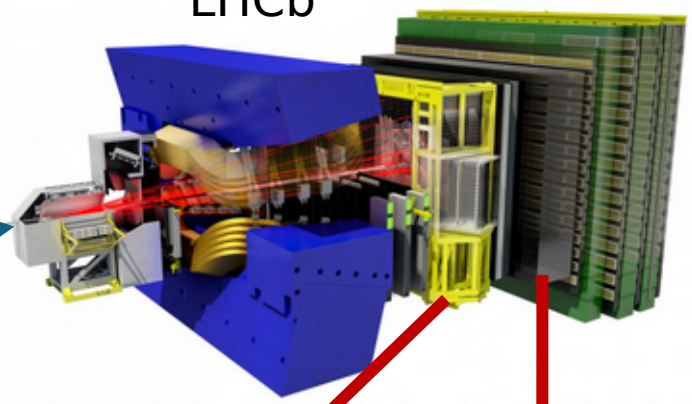


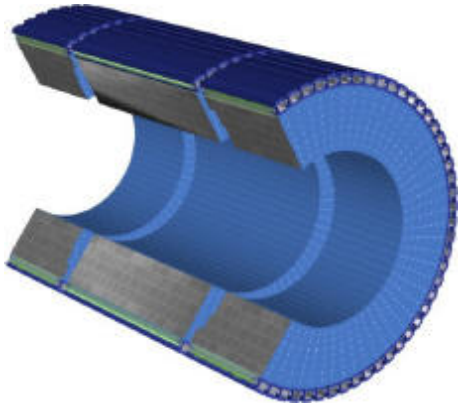
LHC

Inner Tracker

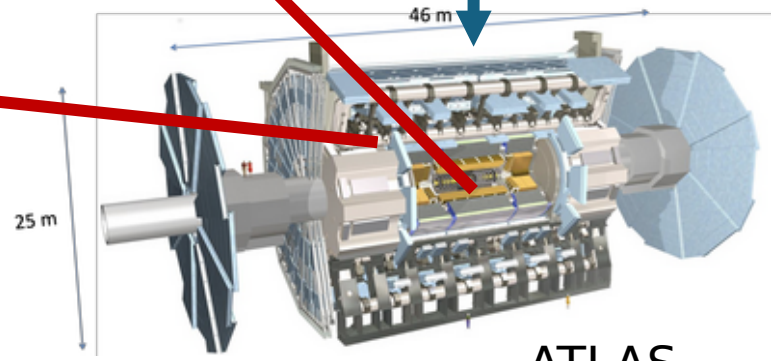


LHCb



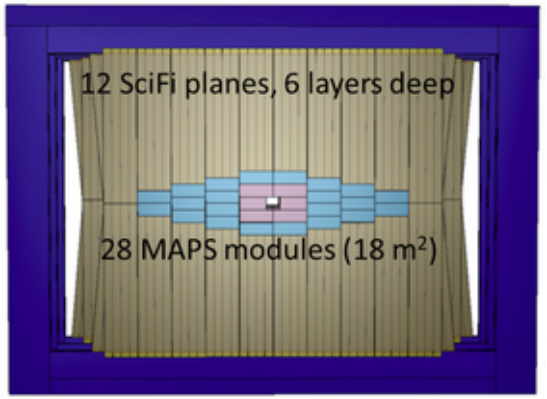


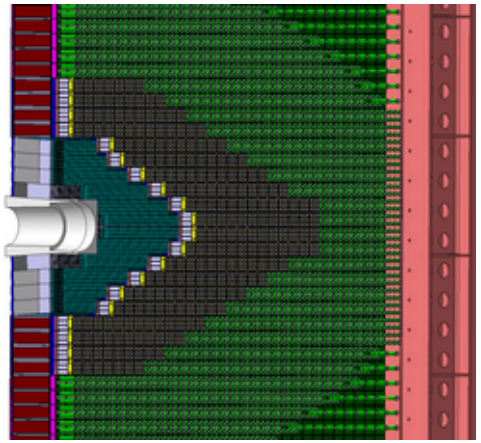
Tile Calorimeter



ATLAS

Mighty Tracker

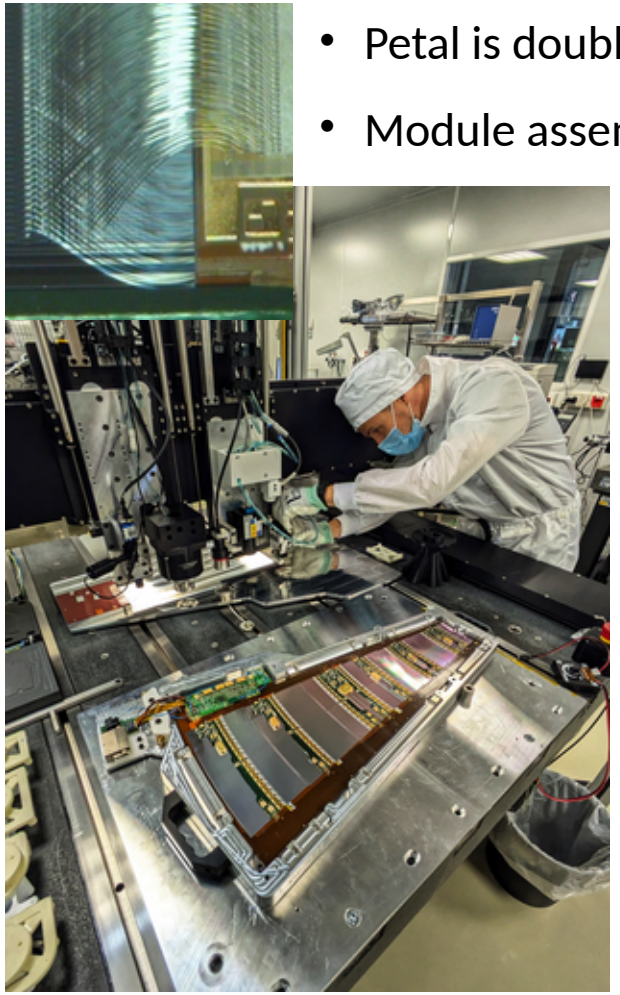




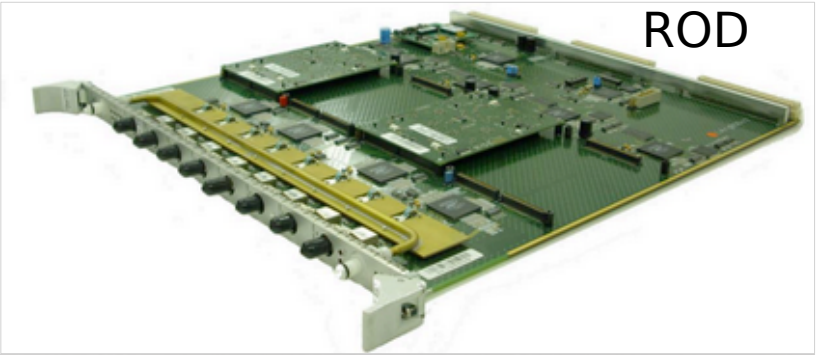
PicoCal

ATLAS Upgrade Activities

ITk: most inner detector in ATLAS based on Si sensor, with pixel and strip layers.
Leading role in detector management (Carlos Lacasta)



- Petal is double sided object 9 modules 10x10cm2 per side.
- Module assembly in IFIC's clean room (25% of production).
- Assembly process on local support.
- Sensor wire bonded in 4 layer scheme up to 1.5m of wire per module.



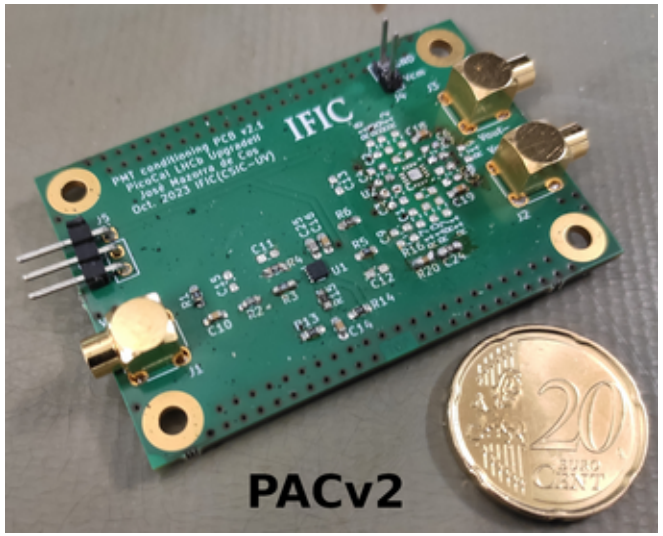
TileCal: central hadronic calorimeter in ATLAS,
10k PMTs sampled at LHC 40MHz clock.

- Current Read-Out Driver (ROD) interfaces FE to HLT and DAQ chain.
  - → ROD: VME 9U board with 165Gbps maintained and upgraded by IFIC.
- ROD to be substituted by PreProcesor (PPr) during Upgrade (2026-2030).
  - → PPr: ATCA board with 40Tbps throughput, IFIC fully responsible.
  - → PPr provides E reconstruction with NN in FPGA on real time for all channels.

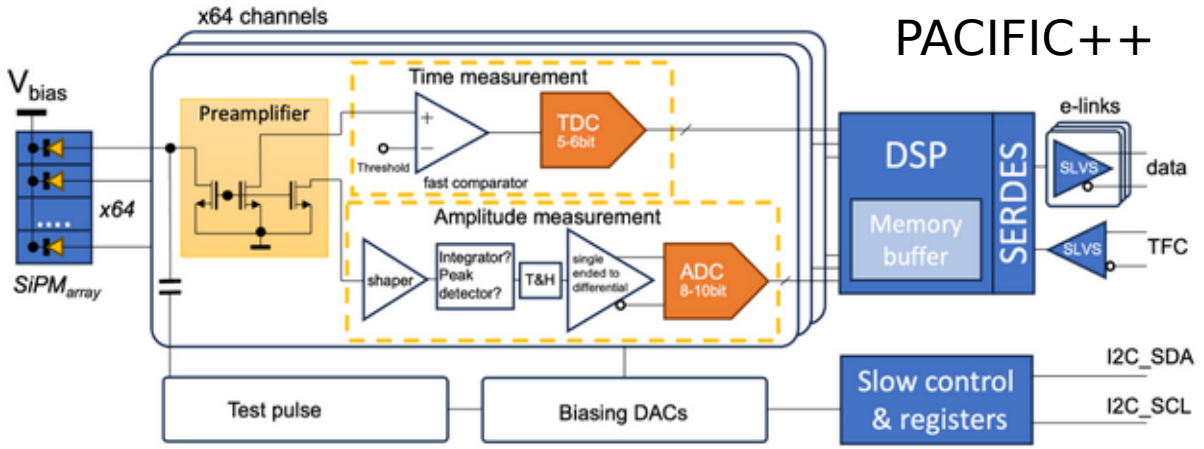
LHCb UpgradeII Activities

PicoCal: heterogenous sampling calorimeter with rad-hard crystal scintillators and precise timing.

- Chipset with energy(ICECAL65) and time(SPIDER) ASIC.
  - → Contributions to ICECAL65 design and test.
- Interface with PMT through COTS circuit (PAC).
  - → High bandwith (250MHz) and amplitude range (2V).
  - → Design, test and production at IFIC.

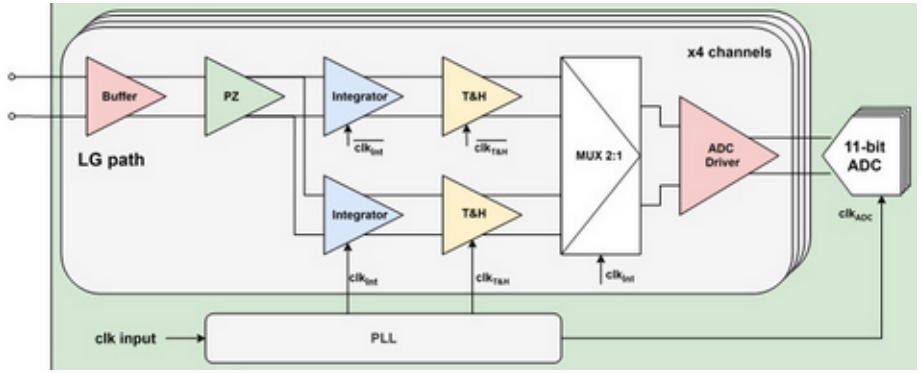


PACIFIC++



Mighty Tracker: multi-technology downstream tracker. (SciFi with SiPMs + HV-CMOS)

- PACIFIC++: SiPM readout chip w. digitization and timing.
  - → Contributions to design, production and test.



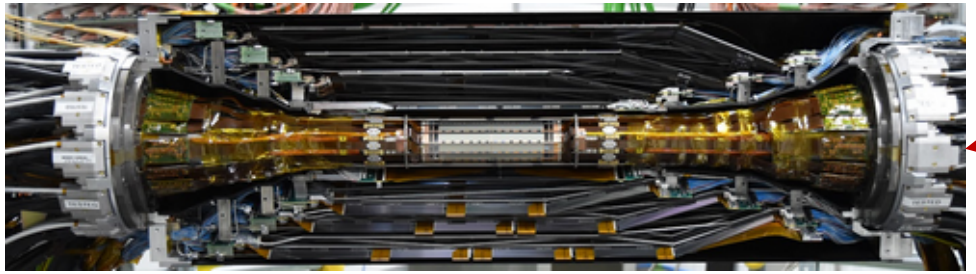
ICECAL65

IFIC at SuperKEKB's Belle II

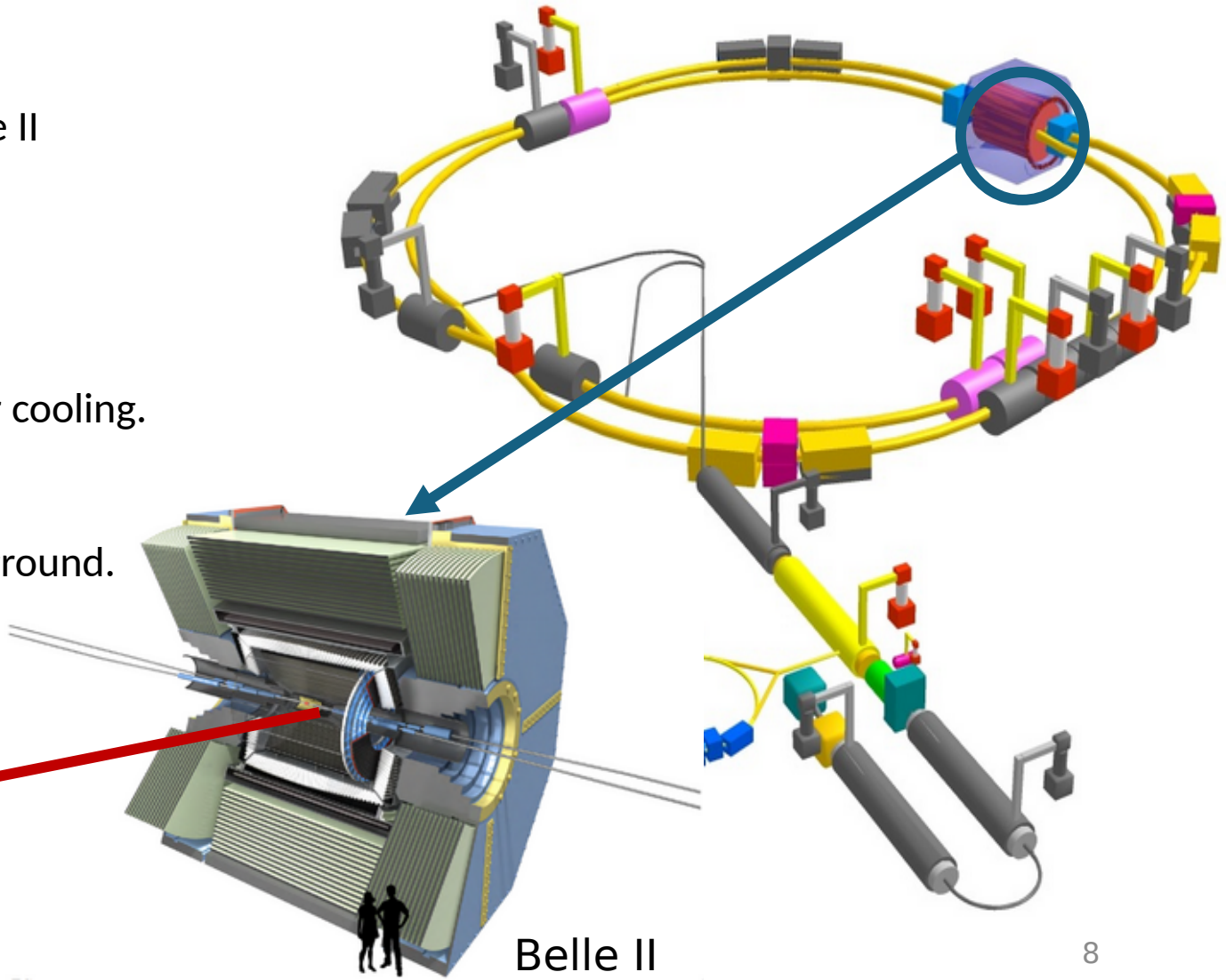
Leading role in Belle II upgrade (Carlos Mariñas).

VXD/VTX: vertexing detector at the inner part of Belle II using silicon strip and pixel sensors.

- Upgrade to all CMOS DMAPS.
  - New ASIC design (OBELIX) with 33μm pixel pitch.
  - All Si ladder inner layer (material budget) with air cooling.
  - CF structure for outer layers with water cooling.
  - Aim: maintain performance with increased background.



VXD/VTX

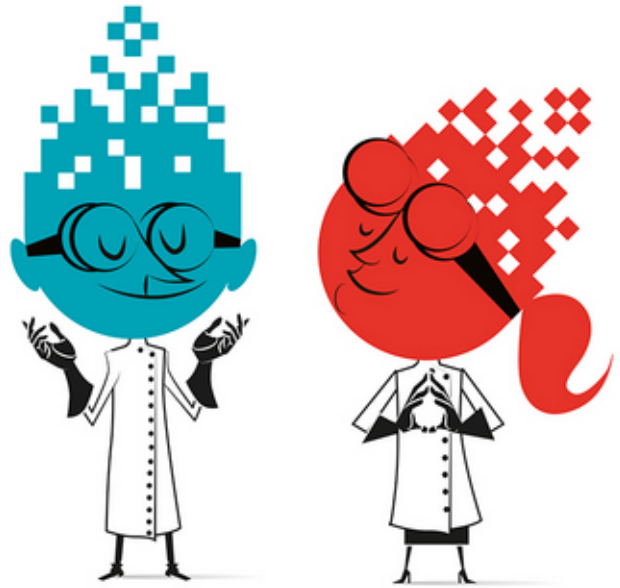


Belle II

Main Detector R&D Areas

Activities aligned with the DRDs of the European Strategy, mainly on:

- DRD3 – Solid state detectors
  - Monolithic CMOS
  - Large area DMAPS
- DRD7 – Electronics and on-detector processing
  - Data transfer
  - DAQ and TRG systems
  - Silicon photonics, transceivers, …
- DRD8 - Integration
  - Ultra lightweight mechanics
  - Cooling systems



→ Silicon detector developments are the strongest focus of our interest

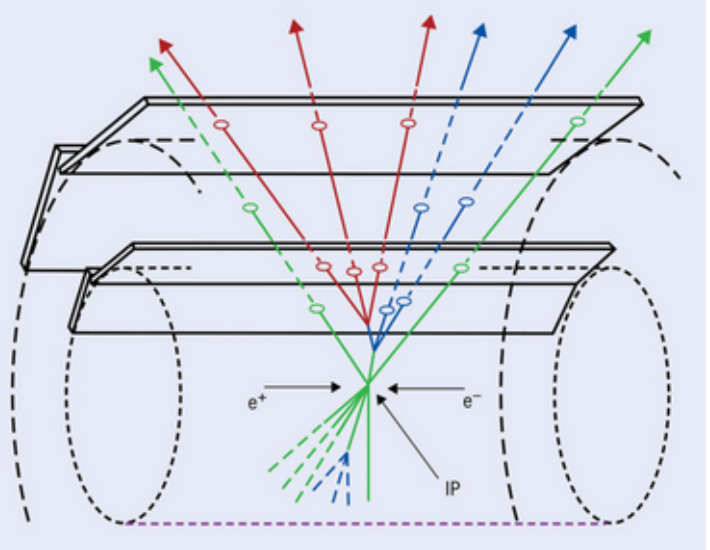
Silicon Pixel Sensors

Vertex Resolution

- Vertexing is key to the performance of detectors in HEP experiments

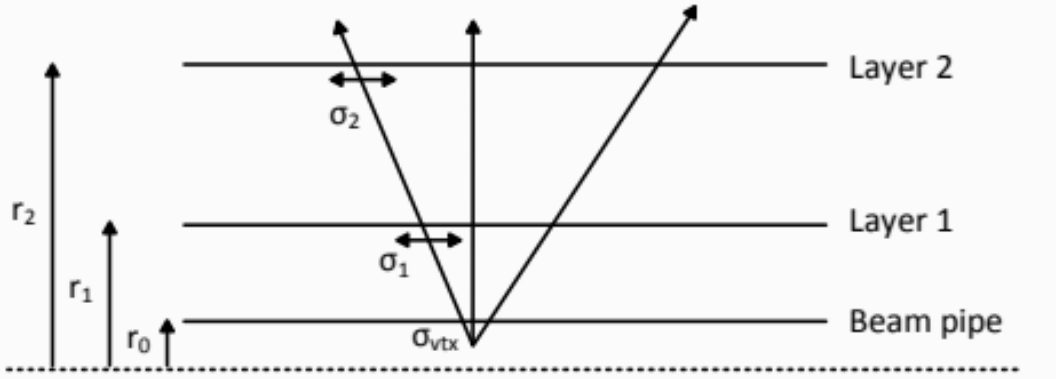
Vertex resolution

$$\sigma_{vtx} = \sqrt{\left(\frac{r_1}{r_2 - r_1} + 1\right)^2 \sigma^2 + (2r_1 - r_0)^2 (13.6\,\mathrm{MeV})^2 \frac{x}{X_0} \frac{1}{p^2}}$$



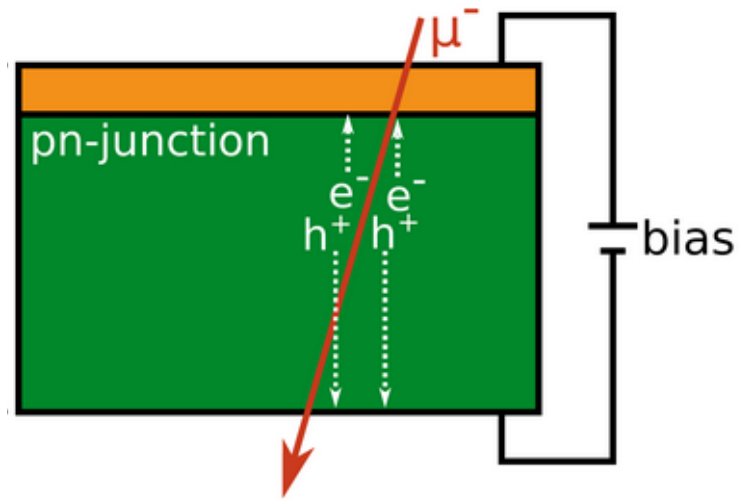
Detector requirements

- Fine segmentation
- Low material (beam pipe and detector layers)
- First layer as close as possible to the beam pipe
- Large lever arm



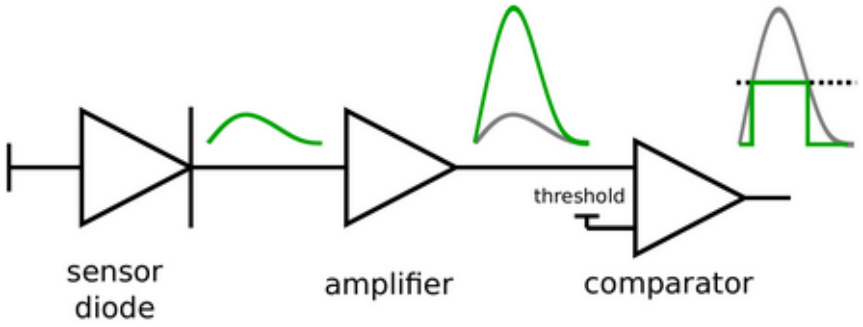
Silicon Pixel Sensors

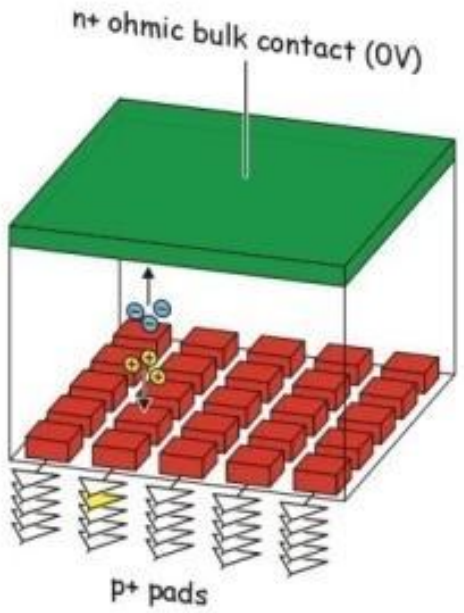
- Particles flying through the bulk produce ionization
- Ionization creates charges in the detector volume:
  - Electron-hole pairs in a semiconductor detector
- Electric field applied to move the charges and ‘induce’ an electric current



- Simplest detector: pn-junction
  - Operated in reverse bias → Depletion region
  - Traversing particle → Ionization = signal carriers in the silicon
  - Typical thickness 50 – 300 μm

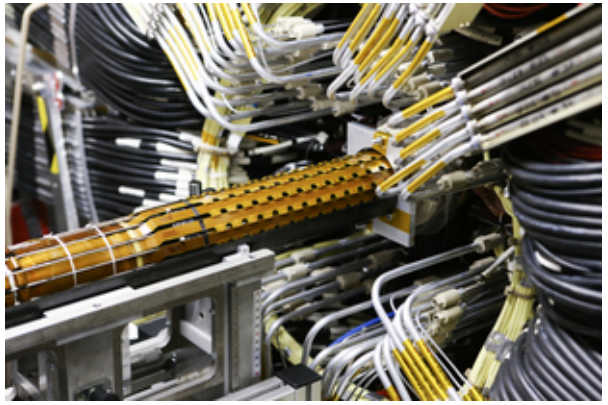
- Pixelated structures inherently offer 2D information:
  - Fine resolutions typically available
  - Compact solutions, low material
  - Requires more electronics



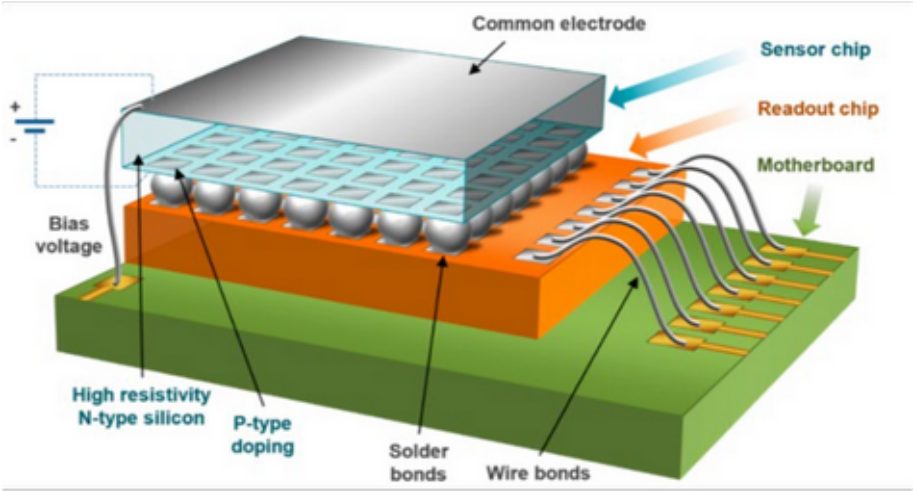


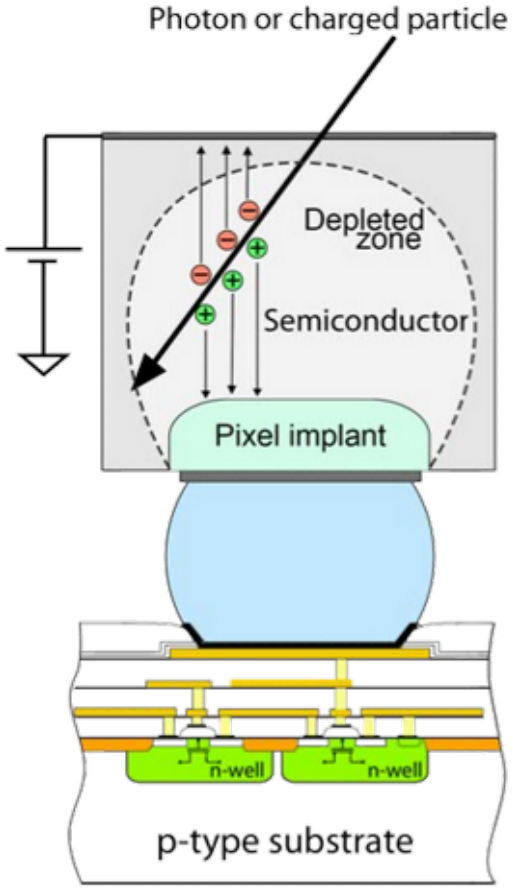
State-of-the-art of LHC Detectors

All based on **Hybrid Pixel Detectors**



ATLAS IBL

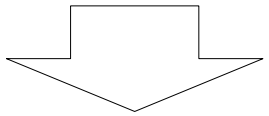




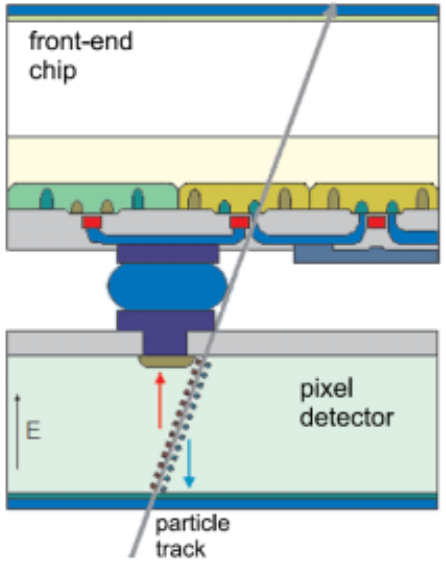
LHCb Velo

From Hybrid Pixels to Monolithic

- Standard HYBRID pixels
  - Various sensors: planar-Si, 3D-Si, diamond
  - Mixed signal R/O chip

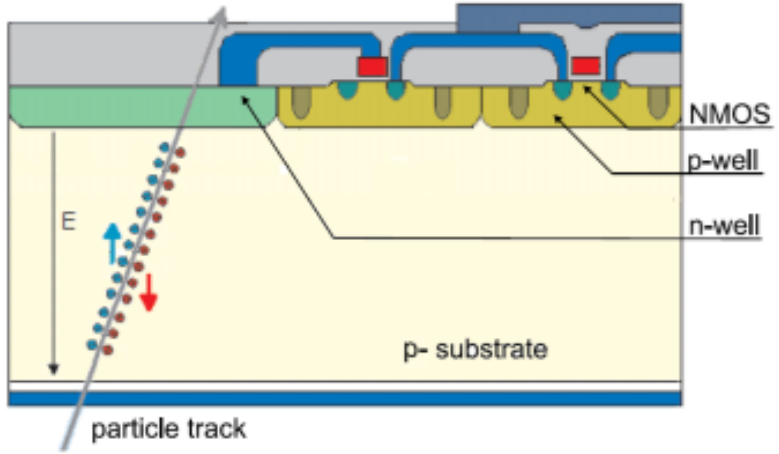


- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion)
  - Depleted DMAPS using HR substrate and/or HV process to create depletion region



Moderate spatial resolution (10-100 µm)
High material budget (few % X_0)
High cost
Radiation hard

High spatial resolution (1 µm)
Low material budget (0.1 % X_0)
Needs modifications for radiation
Simpler readout architecture



CMOS (D)MAPS

CMOS (Depleted) Monolithic Active Pixel Sensors

- Monolithic

Signal generation + readout integrated on a single unit

Low material budget

- Active

Detection and in-pixel amplification and processing

- Depleted

HV process or HR substrate to create depletion region

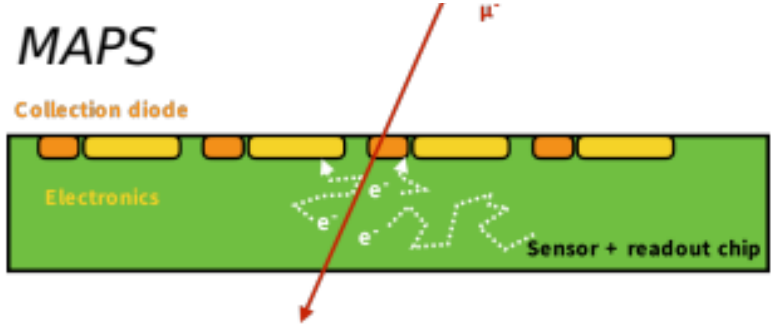
Fast charge collection via drift

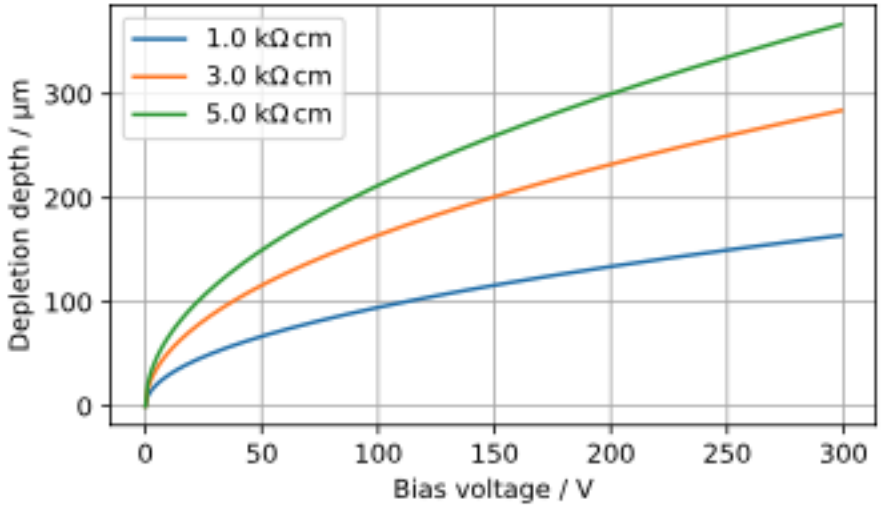
Large depleted volume with large signal

$$d \sim \sqrt{\rho \cdot V}$$

- CMOS (comercial vendors)

Pros	Reduced cost	Large throughput
	Fast turnaround	Large wafers
Cons	Complex layouts	Long term support
	Limited information on processing details	

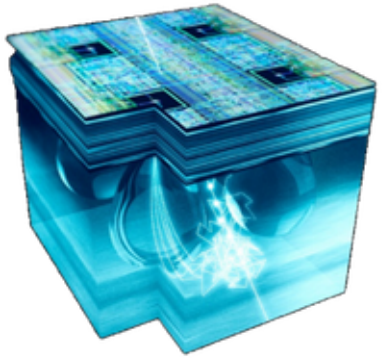




CMOS-MAPS R&D in a Nutshell

- General concepts

2x2 submatrix view
thickness ~50 µm



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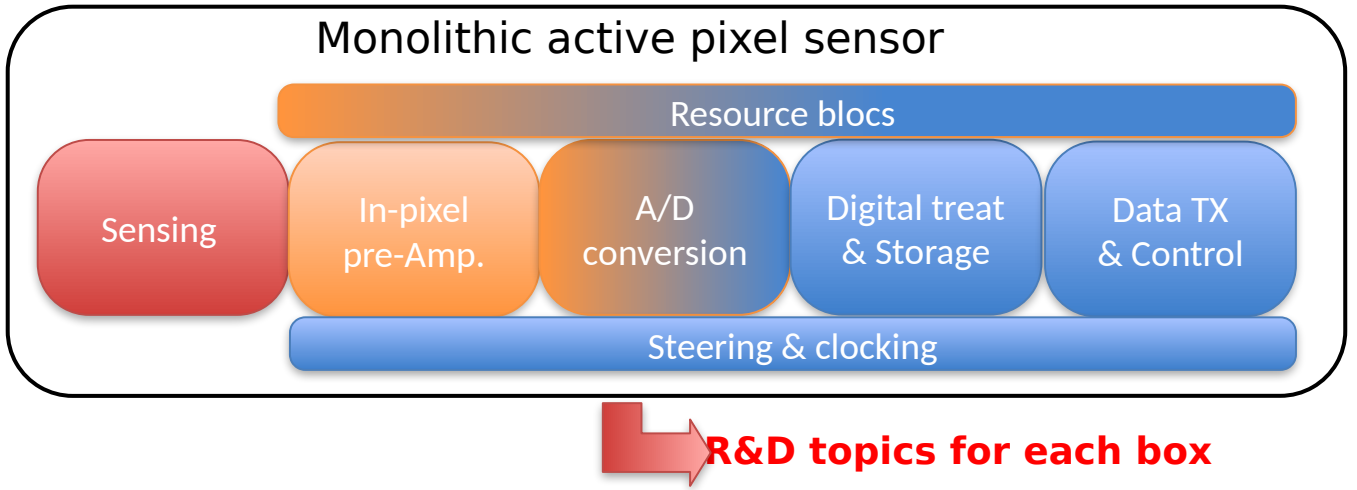
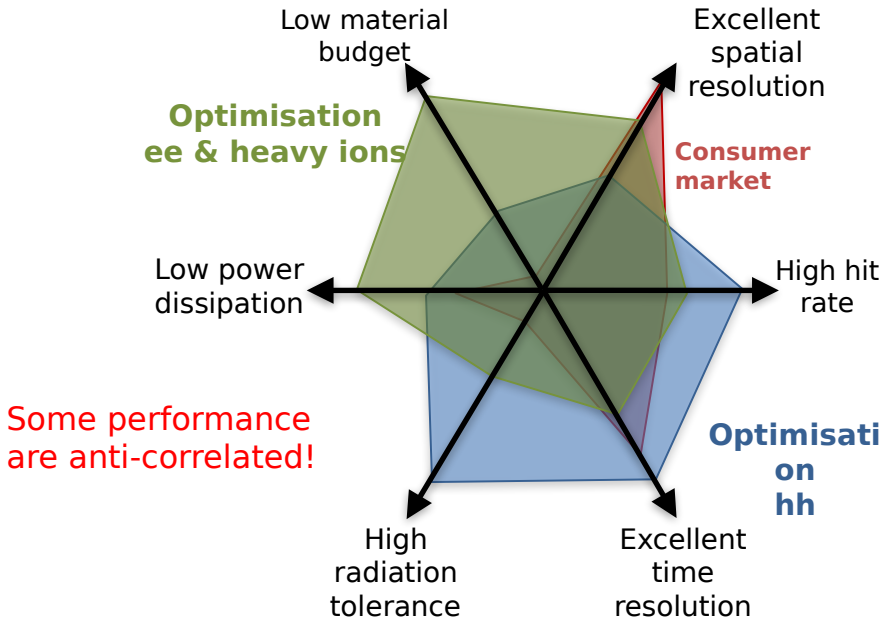


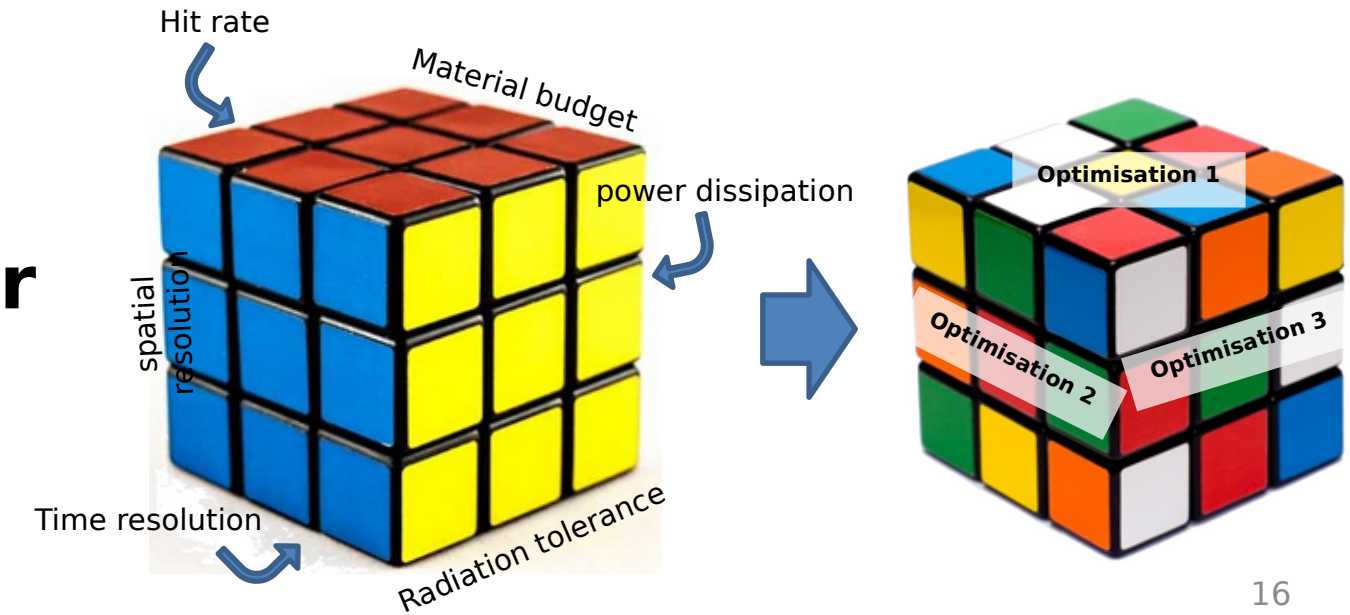
R&D topics for each box

- Performance is a matter of optimisation



Some performance are anti-correlated!

or

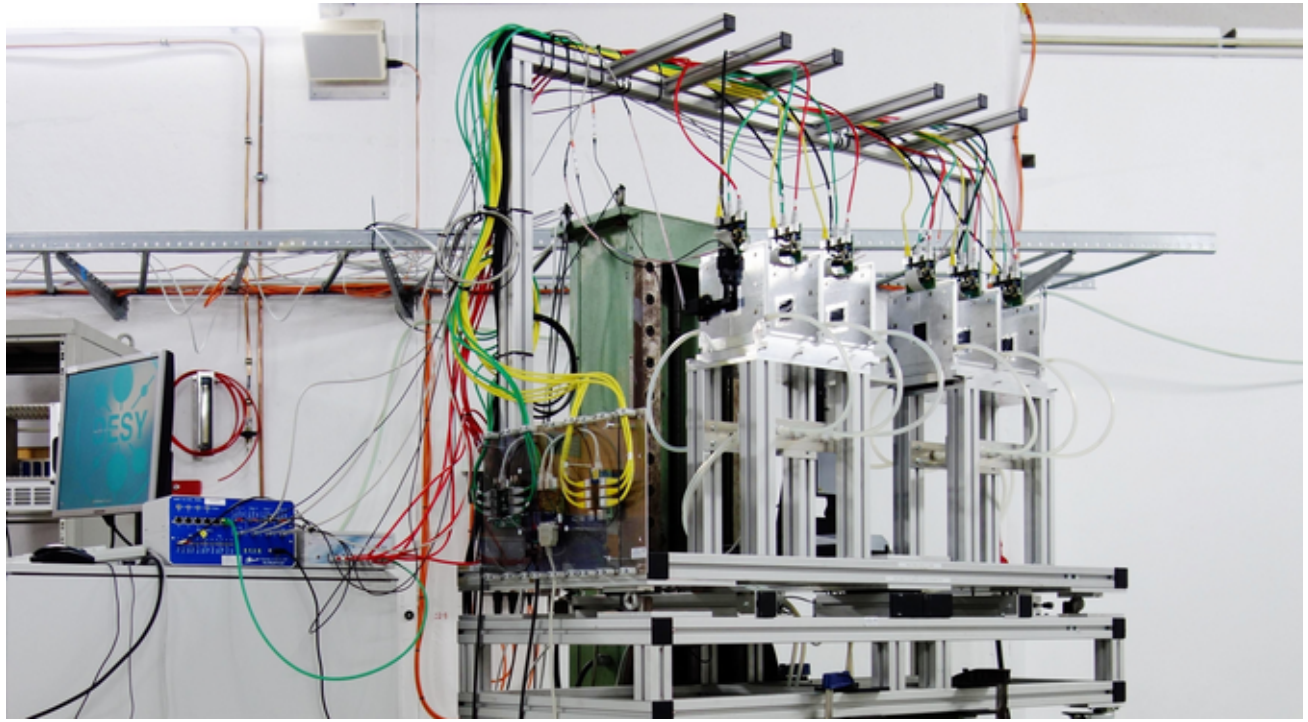


Demonstrator Development at IFIC

Future Vertex Detector Demonstrator

Intelligent, thin, fine-pitch vertex detector prototype in the context of a full demonstrator design

→ In other words: A large area DMAPS particle beam telescope

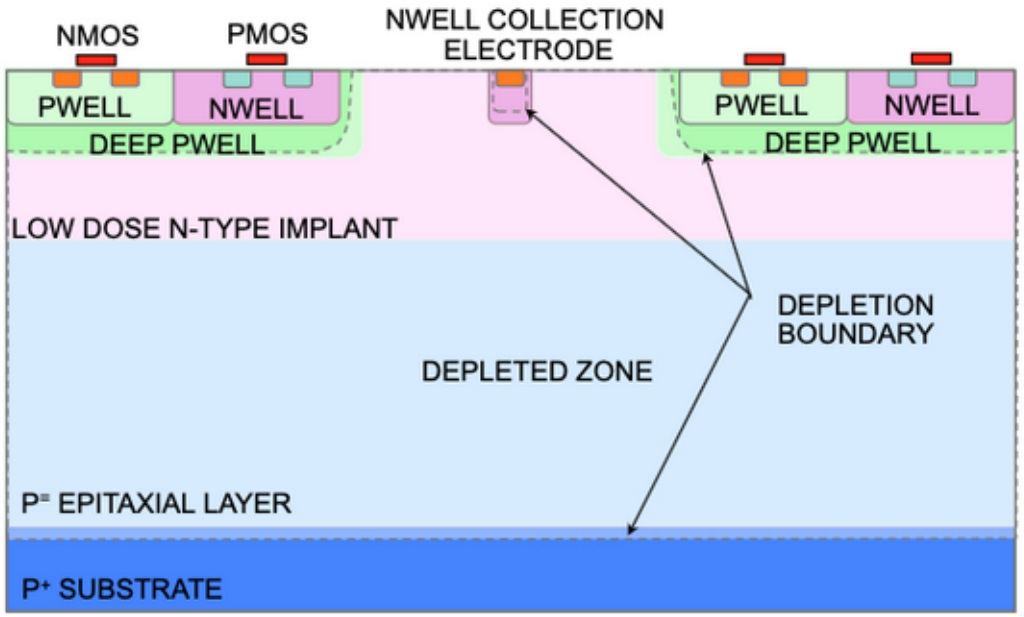


Bring the existing infrastructure to the next level, together with our national and international partners

- 6 large area high-resolution detector planes
- 2 fast planes
- DAQ and TRG
- Compact integration

Small Electrode Sensor Design DMAPS

Monolithic detector: Combine sensor and readout on the same wafer



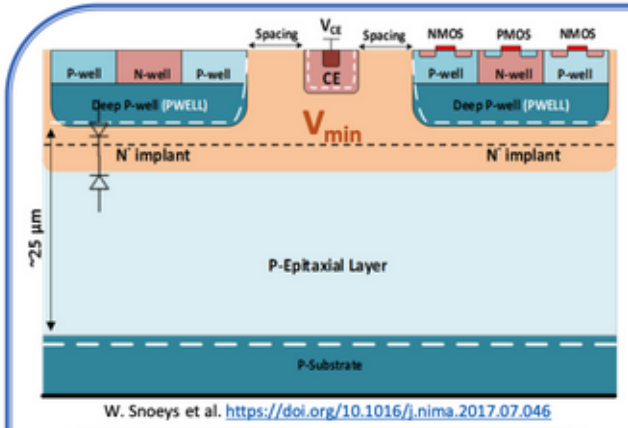
Electronics outside the collection well
Small fill factor

- Very small sensor capacitance
- Low noise and power

TowerJazz 180 nm CIS

- Deep pwell allows for full CMOS in pixel
- High resistivity epi-layer 1-8 kOhm.cm
  epi thickness 18-40 µm
- 3 nm gate oxide for good TID
- Modified process: Additional planar n-type implant
  Full depleted volume
  Fast charge collection
- Derived from LHC developments

TJ-Monopix Family



W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

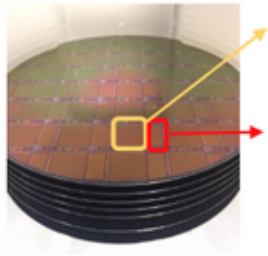
$C_d \leq 3fF$

$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

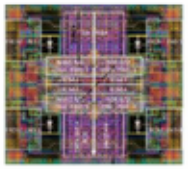
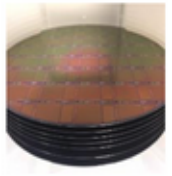
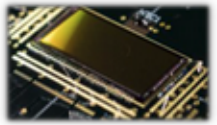
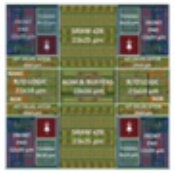
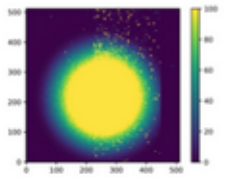
DMAPS in TJ 180 nm: Concept

- Small sensor capacitance (Cd)
  - Key for low power/low noise
- Radiation tolerance challenges
  - Modified process
  - Small pixel size
- Design challenges
  - Compact, low power FE
  - Compact, efficient R/O

Large scale demonstrator chip development



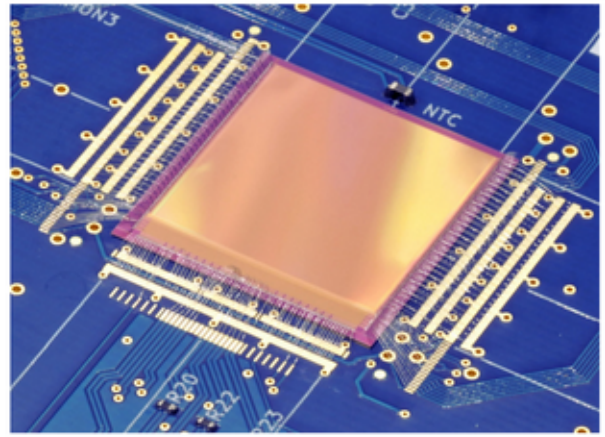
- MALTA
  - Asynchronous readout
- TJ-Monopix1
  - Synchronous column-drain R/O
- Process modification enhancements, Cz substrate ⟹ improved efficiency
- TJ-Monopix2: Improved full-scale DMAPS

TJ-Investigator characterization	*TJ-Monopix1* & MALTA Design	*TJ-Monopix1* & MALTA Submission	Mini-MALTA sub. with process fixes	*TJ-Monopix1* resub. process fixes & Cz	*TJ-Monopix2* & *MALTA2* Design	*TJ-Monopix2* & MALTA2 Submission	*TJ-Monopix2* Characterization	*"OBELIX"* Design
								Full scale System-ready: LDO, CDR, memory etc.
Q2 2016	Q4/2016	Q3/2017	Q3/2018	Q2/2019	Q2/2019	Q3/2020	Present	~~Future plans~~

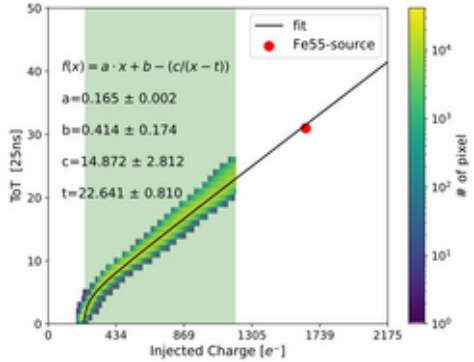
Present

TJ-Monopix2 Characterization

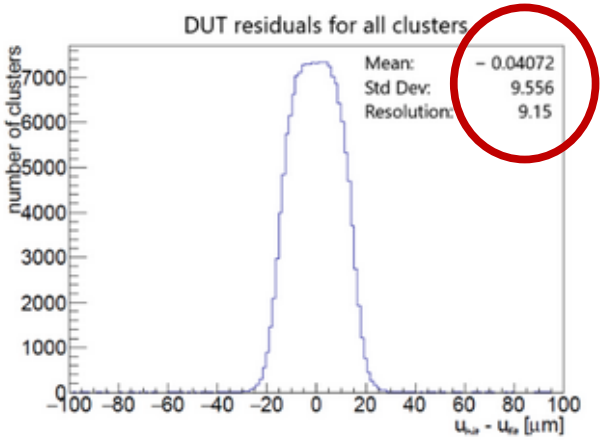
- TJ-Monopix2 as forerunner of OBELIX
  - 33x33 µm² pitch, 25 ns integration, 2x2 cm² matrix
  - 7 bit ToT information, 3 bit in-pixel threshold tuning
  - Various sensing volume thickness (CZ-bulk, epi-30 µm)

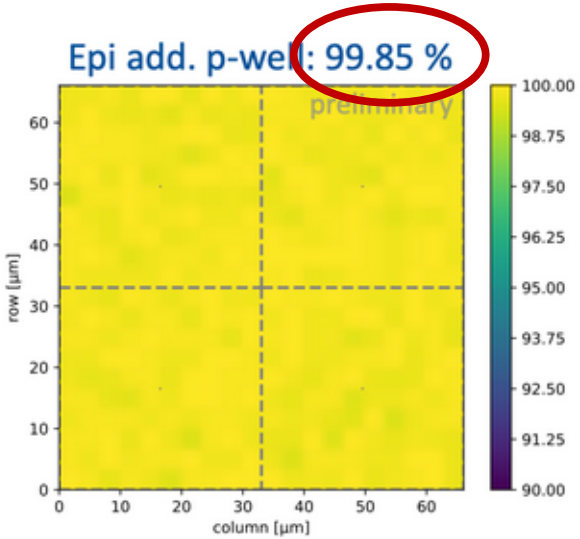


- Detailed characterisation
  - In-laboratory
    - Threshold / noise
    - ToT calibration
  - In-beam (DESY, 5 GeV electrons)
    - Efficiency ~99%
    - Position resolution ~9 µm
  - Irradiated up to $5x10^{14}n_{eq}/cm^2$ without relevant loss of performance



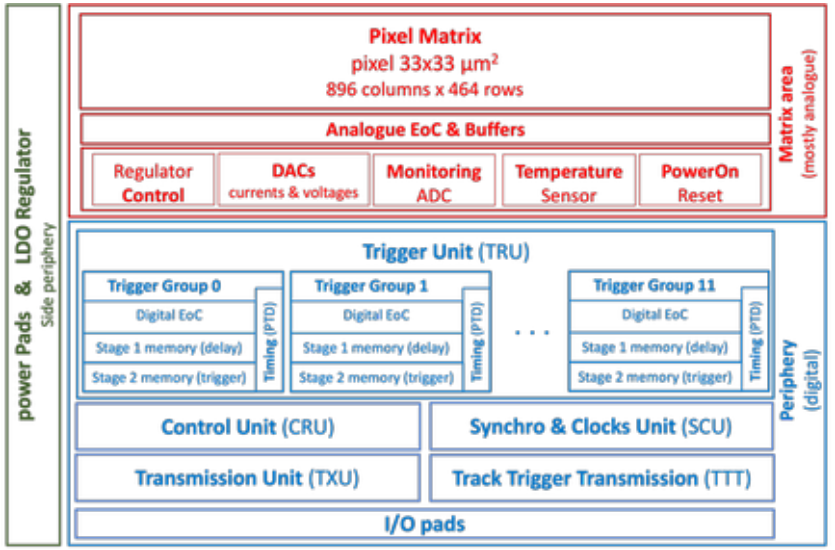
Consistently achieving <300 e^- threshold levels in all samples

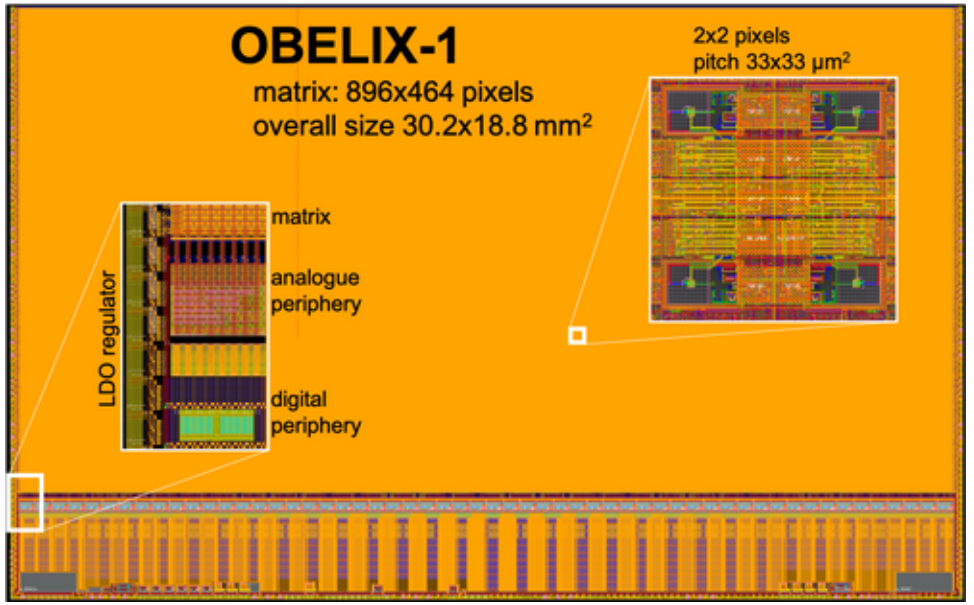




OBELIX

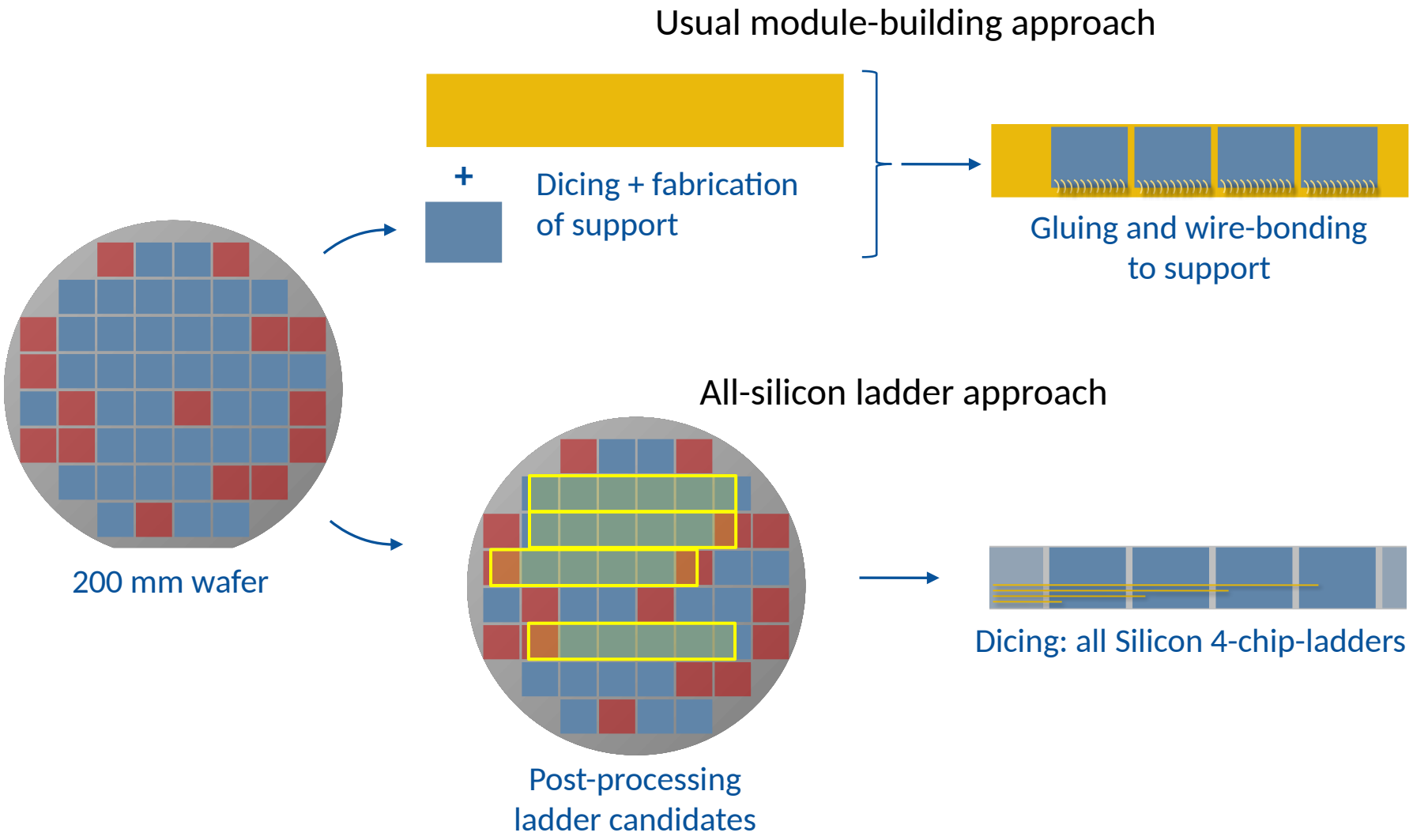
- Matrix design
  - Extended copy of TJ-Monopix2
  - 2 front-end flavours: **DC- and AC- cascode amplifier**
  - Clock for time-binning slowed down: 100ns
- Powering
  - LDO regulator for easier voltage distribution
  - Overall power depends on hit rate: 200-300 mW/cm^2
- Trigger Unit
  - Simulated with realistic inputs: 120 MHz/cm^2
  - Can sustain 600 MHz/cm^2 for 0.5 µs
- Fine time stamping
  - 6 ns achievable with end-of-column fast clock
    - Limited to hit rate $\lesssim$ 10 MHz/cm^2
- Track trigger
  - Reduced granularity to 8 strixels (~4 x18 mm^2)
  - Increased transmission rate: 33 MHz





Production Q3 2025

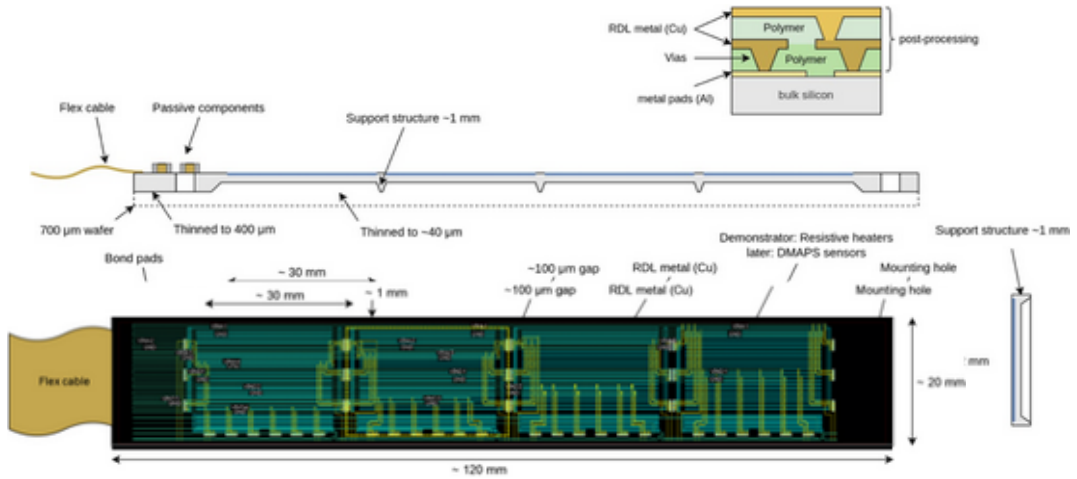
All Silicon CMOS Ladders



All Silicon CMOS Ladder Concept

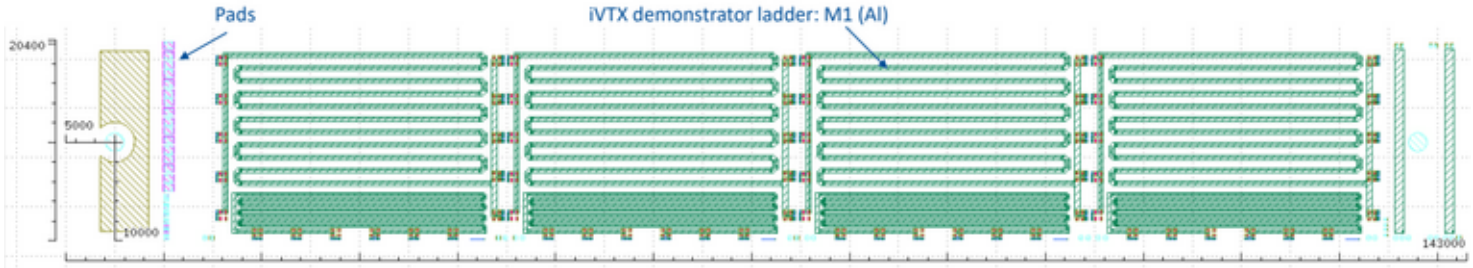
All-silicon module < 0.15 % X_0

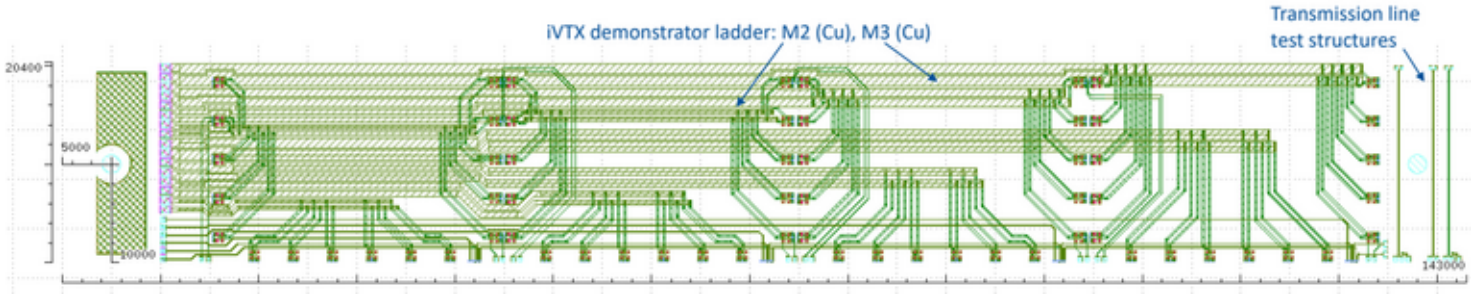
- 4 contiguous sensors diced as a block from the wafer
- Redistribution layer for interconnection
- Heterogeneous thinning for thinness & stiffness



Prototyping (Demonstrator)

First real-size ladders at IZM-Berlin with dummy Si





Metal system:

- Resistive heaters: 1.5 um Al (M1)
- 2 RDL metal layers: 3 um Cu (M2, M3)
- Top metal finish: NiAu (M4)

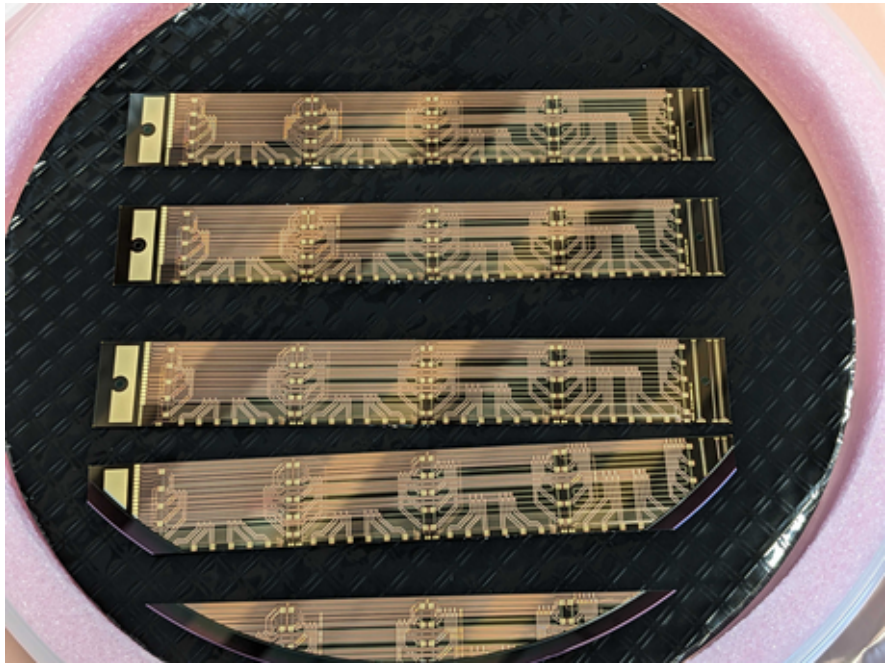
  Wirebonding, SMD soldering

Final ladder dimension: 143 x 20.4 mm^2

Dummy heaters: 30 x 20 mm^2

Prepared for 1.7 mm mounting hole

All Silicon CMOS Ladder Demonstrator



First RDL demonstrators:
8 Wafers (725 µm, 400 µm, 300 µm)

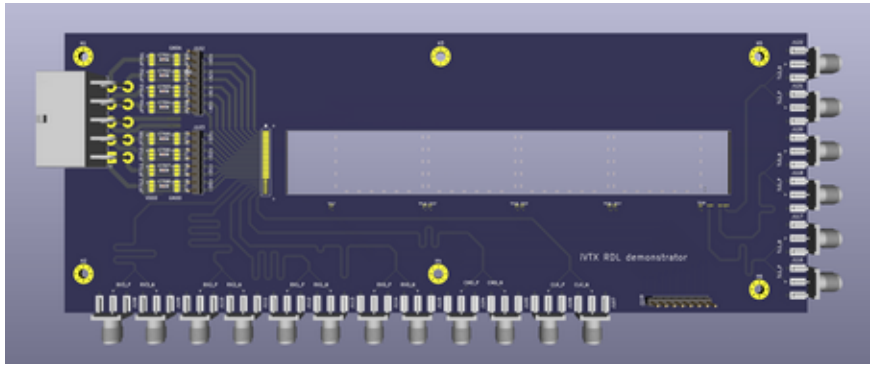
Production finished smoothly

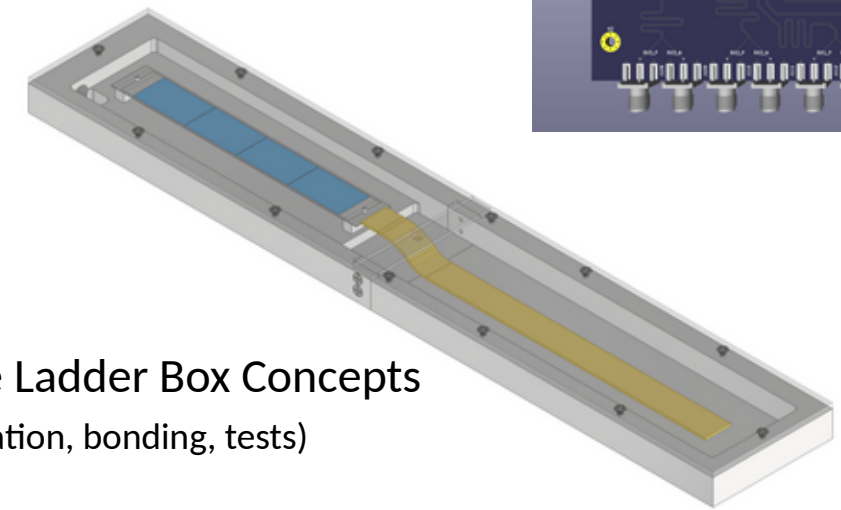
Characterization starting

Configurable power routing and test points for I*R drop measurements

SMA connection for data lanes and TDR measurements

Also preparing a PCB mockup of the ladder to practice soldering etc





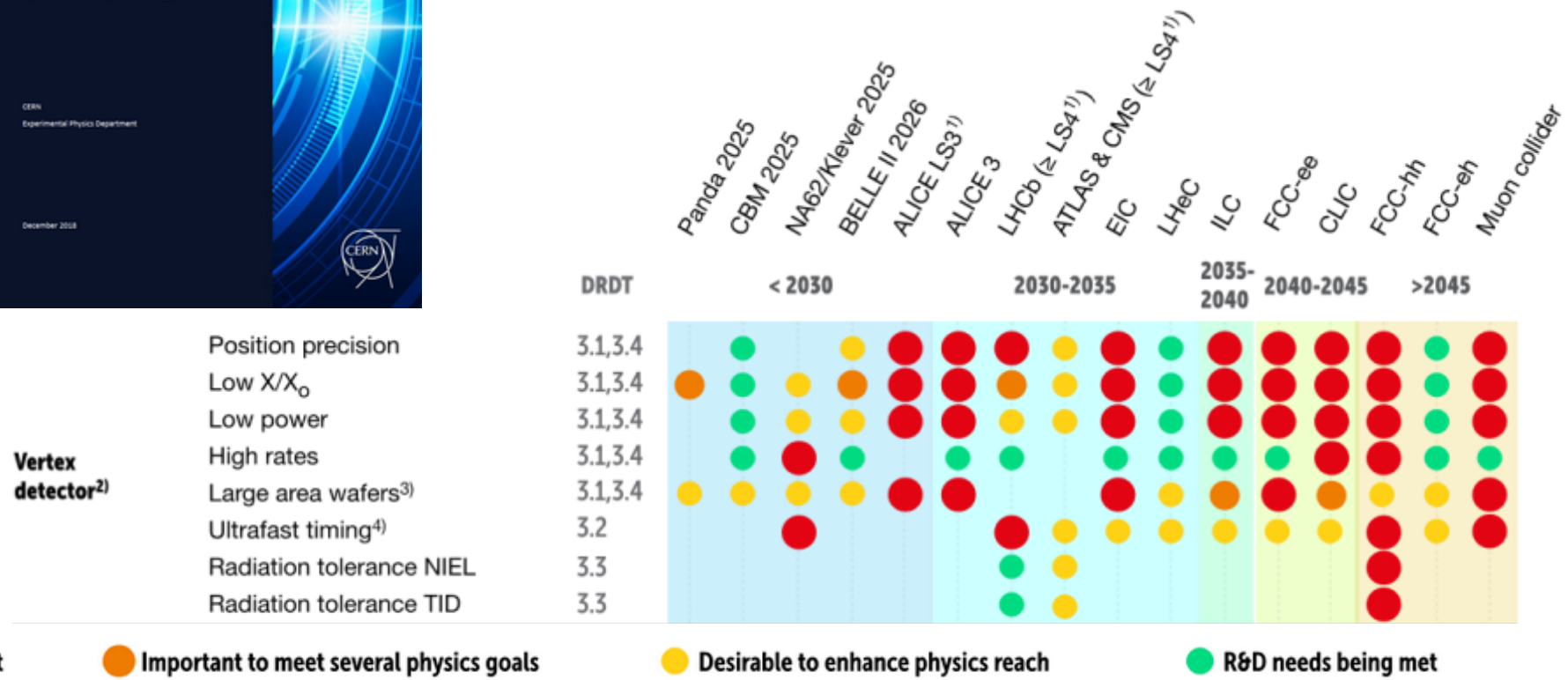
Multiuse Ladder Box Concepts
(Transportation, bonding, tests)

International R&D Landscape

European Strategy and CERN R&D Program

Parallel structure in Eurpean Strategy and CERN R&D Programm

Focus on large area DMAPS sensors with high spatial resolution and low mass, exploring CMOS commercial technologies



Must happen or main physics goals cannot be met

Important to meet several physics goals

Desirable to enhance physics reach

R&D needs being met

Conclusions & Outlook

Conclusions & Outlook

- IFIC involved in detector development at several HEP experiments (ATLAS, LHCb, Belle II).
  - Experience in silicon sensors, FE and BE electronics, mechanics, cooling, integration …
- Strong interest in R&D for vertex detectors and trackers based con CMOS DMAPS
  - Activity in line with different strategies in R&D international landscape (ECFA, DRD …)
- Future Vertex Detector Demonstrator under development in synergy with other projects.
  - TJ-Monopix2 performance, including irradiated devices, matches expectations
    → Solid steppingstone towards OBELIX, to be submitted in Q3 2025
  - All silicon CMOS ladder demonstrator produced and under test

- ASFAE program allowed us to maintain our strong leadership in current experiments and develop cutting-edge instrumentation for future colliders

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THANK YOU