Towards HL-LHC: Spanish contributions to the ATLAS, CMS & LHC-b upgrades

Manuel Lozano (On behalf of all Spanish Groups)

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Plan de Recuperación, Transformación y Resiliencia

Funded by the European Union NextGenerationEU

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Agencia Estatal de Investigación

Centro Nacional de Microelectrónica IMB

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Micro nano Fabs Red Española de Salas Blancas de Micro y Nano Fabricación

ICTS Infraestructuras Científicas y Técnicas Singulares

www.imb-cnm.csic.es

Aknowledgement

- This is a presentation made of many contributions. Warm thanks to:
  - Cristina Fernández Bedoya, Ignacio Redondo
  - Sebastian Grinstein, Stefano Terzo
  - Carlos Lacasta, Fernando Martínez, Arantxa Ruíz
  - Gervasio Gómez
  - Santiago Folgueras
  - Miguel Ullán, Salvador Hidalgo, Giulio Pellegrini
  - Abraham Gallas
  - Eugeni Graugés
  - Diego Martínez Santos
  - Xavier Vilasís

Disclaimer:

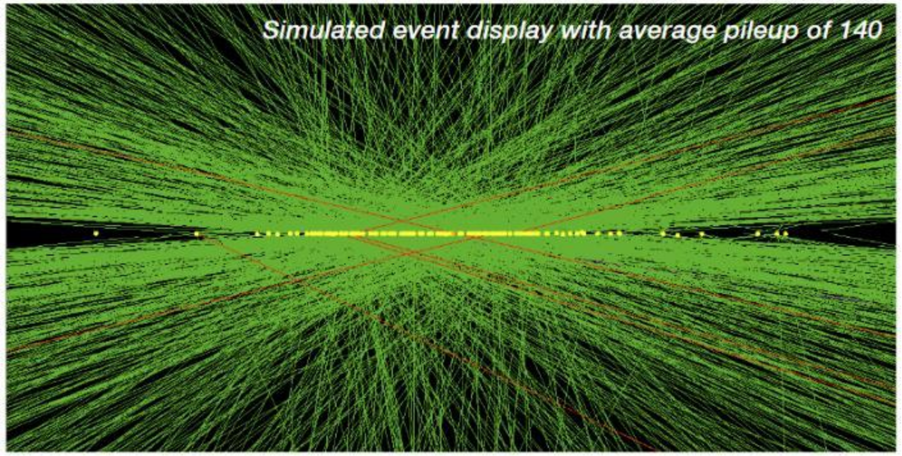
- Only detectors, no magnets, nor accelerator
- Almost no Real Time Analysis
- No personal names

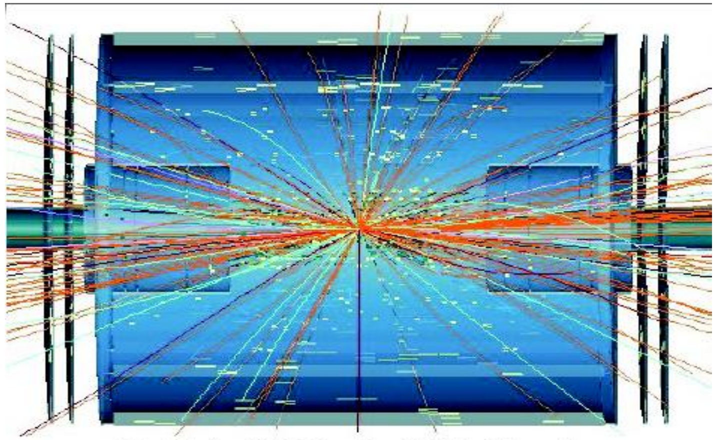
Apologies:

- It is almost impossible to present every contribution
- Apologies for the missing parts

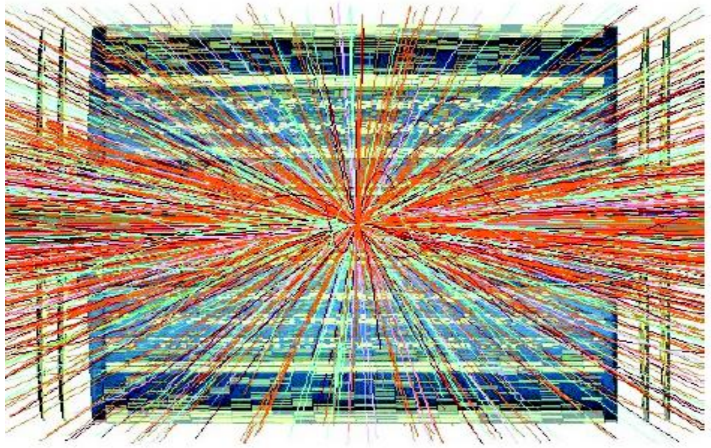
HL-LHC Upgrade

- High Luminosity upgrade of the LHC accelerator
  - Provide ~ x10 increase in luminosity w.r.t LHC design value
  - Larger datasets → increase potential for discoveries after 2029
  - Physics motivation covered in other talks
- Challenging operational environment requires major detector upgrades
  - From 20 to 200 collisions per beam crossing; track multiplicity from ~700 to 10.000
  - Radiation tolerant detectors and electronics to cope with unprecedented fluences
  - Increased granularity to cope with large occupancy and track multiplicity (large pileup)
- Spain contributes to the upgrades of ATLAS, CMS and LHCb



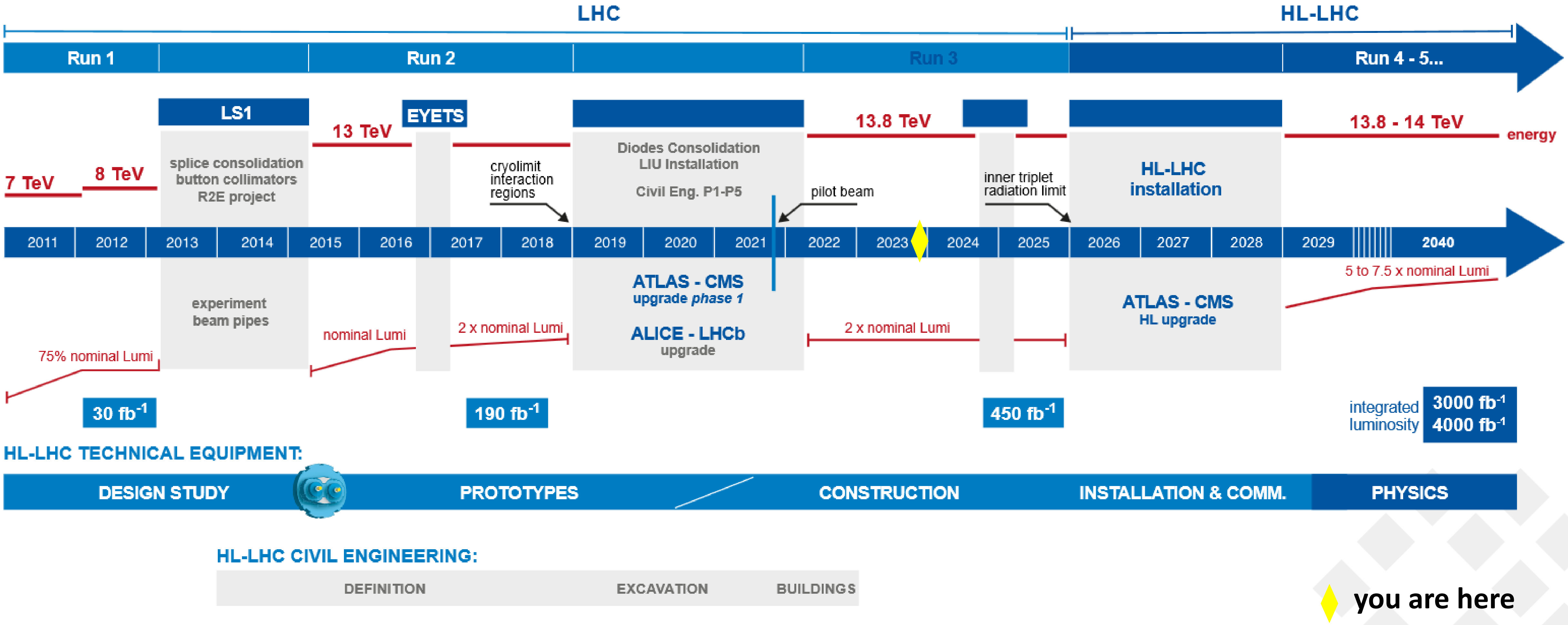


LHC in 2011: $1x10^{33}$ 1/cm^{2}s



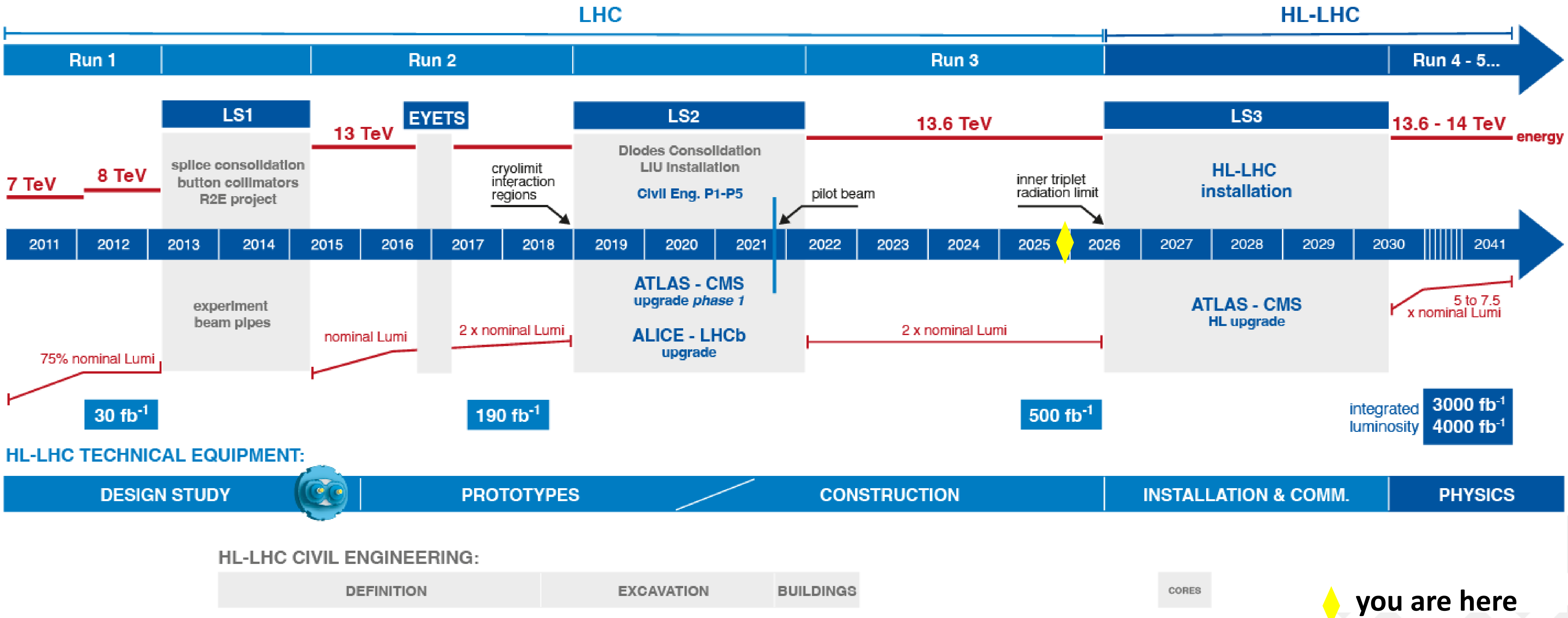
HL-LHC: $5x10^{34}$ 1/cm^{2}s

LHC / HL-LHC Plan



Situation at CPAN Days Nov. 2023 (Santander)

LHC / HL-LHC Plan



Update September 2024: ***"The decision to shift the start of the HL-LHC by approximately one year and increase the length of the shutdown reflects a consensus supported by our scientific committees."***

January 2025 figure

The Spanish Team

ATLAS EXPERIMENT

- TileCal
- ITk-strips
- ITk-pixels
- HGTD

Institut de Física d'Altes Energies (IFAE) · Institut de Física Corpuscular (IFIC) · Centro Nacional de Microelectrónica (CNM) IMB

CMS

- Muon DT
- L1 trigger
- HGCAL
- IT pixels
- MTD-ETL

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LHCb

- ECAL
- VELO
- SciFi/Tk

IGFAE · USC Universidade de Santiago de Compostela · laSalle Universidad Ramon Llull · Institut de Física Corpuscular (IFIC) · ICCUB · Universidade da Coruña

The Spanish Team

- **Muon DT**
- **L1 trigger**
- **HGCAL**
- **IT pixels**
- **MTD-ETL**

CMS Compact Muon Solenoid

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Universidad de Oviedo

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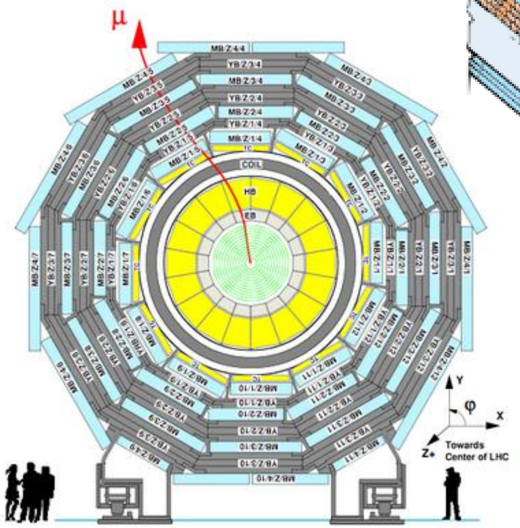

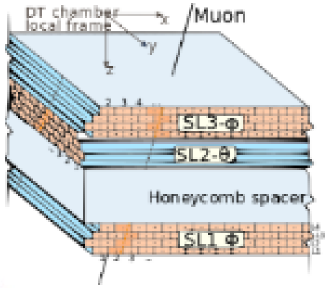

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μ DTs + L1 Trigger

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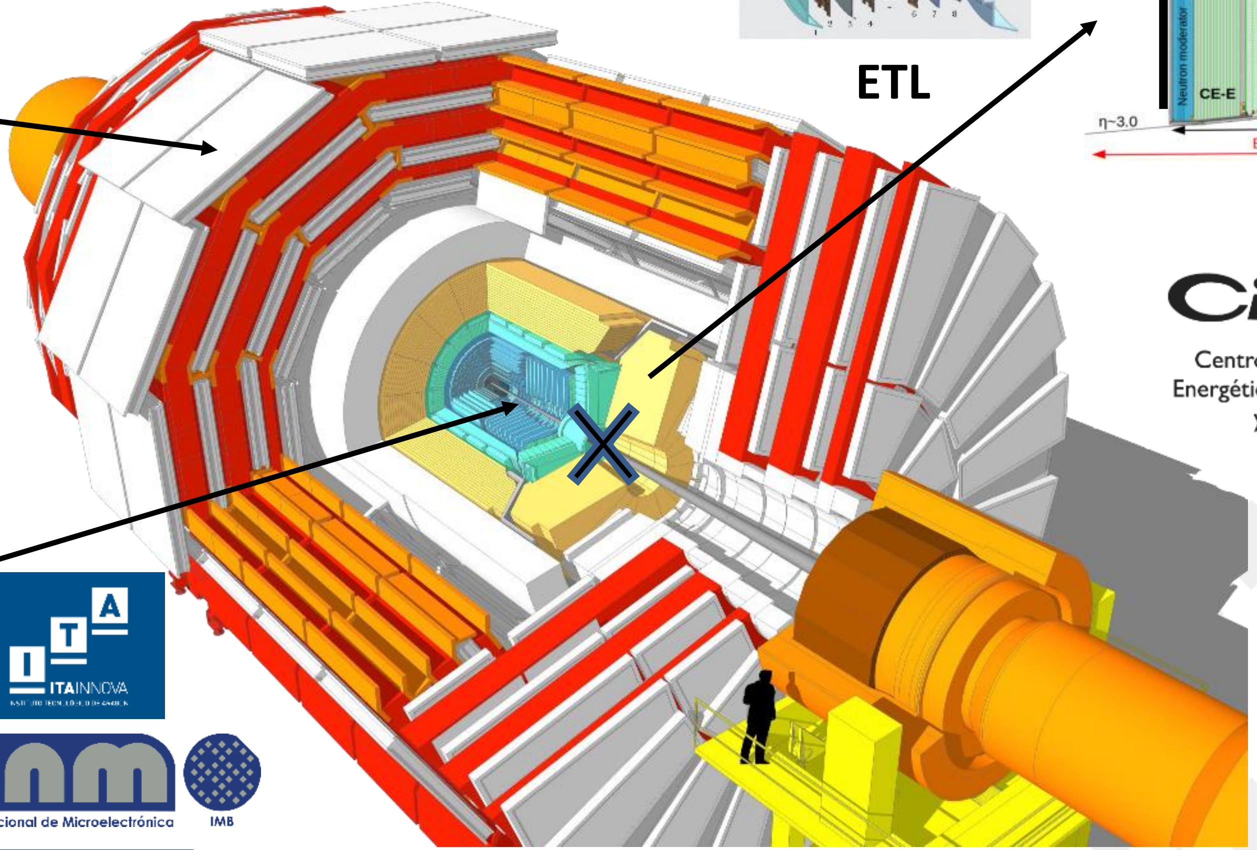
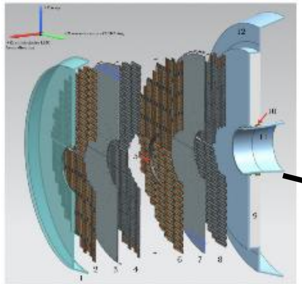
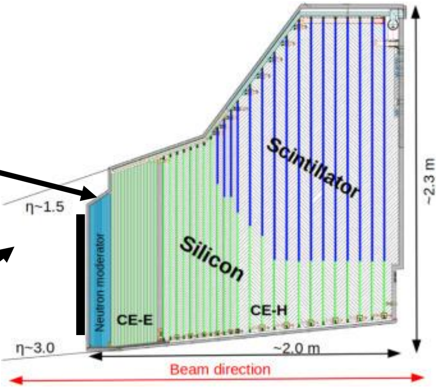
Instituto de Física de Cantabria





ETL



HGCal

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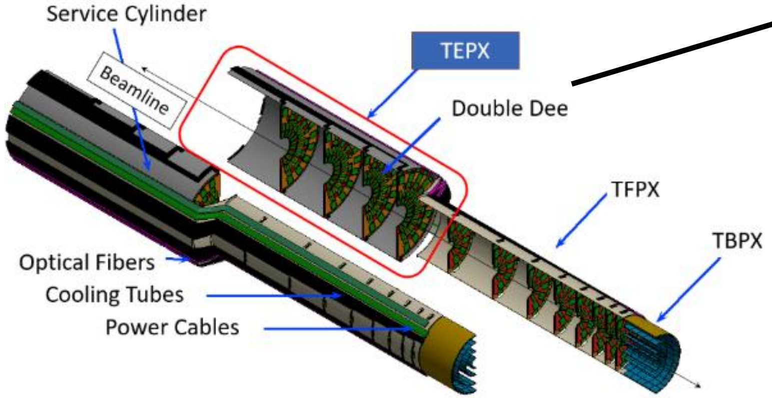
Inner Tracker



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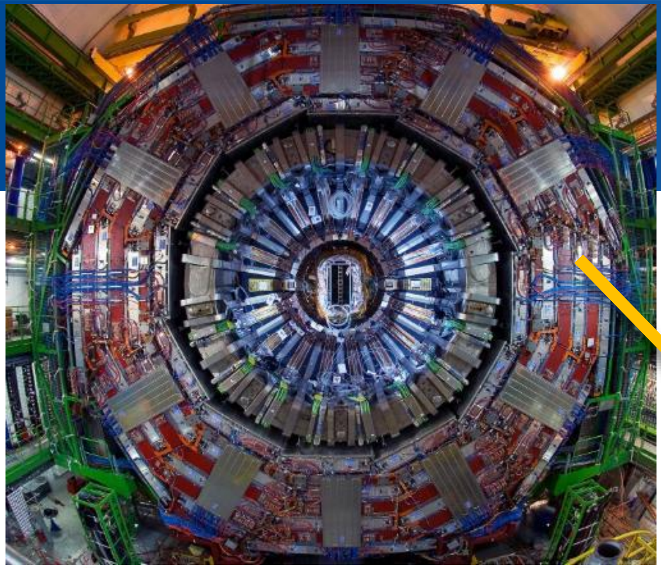
CMS Muon Drift Tube Upgrade



- 250 chambers to be refurbished with new electronics:
  - Time digitization of the 172200 channels
  - Chamber interfaces, pressure ADCs, alignment forks, RPC interfaces, etc
- 830 boards embedded in the 250 Minicrates structures
- Full refurbishment of backend electronics allows reaching ultimate detector performance in the trigger

- **Drift tube chambers** will not be replaced. **Longevity**: several years of radiation campaigns at GIF++ (Gamma Irradiation Facility) to validate its performance under HL-LHC. Efficiency loss should be acceptable
- **Full electronics** needs to be replaced to stand: L1A rate, occupancy, radiation
- Architectural change → to **a full streaming of detector information**

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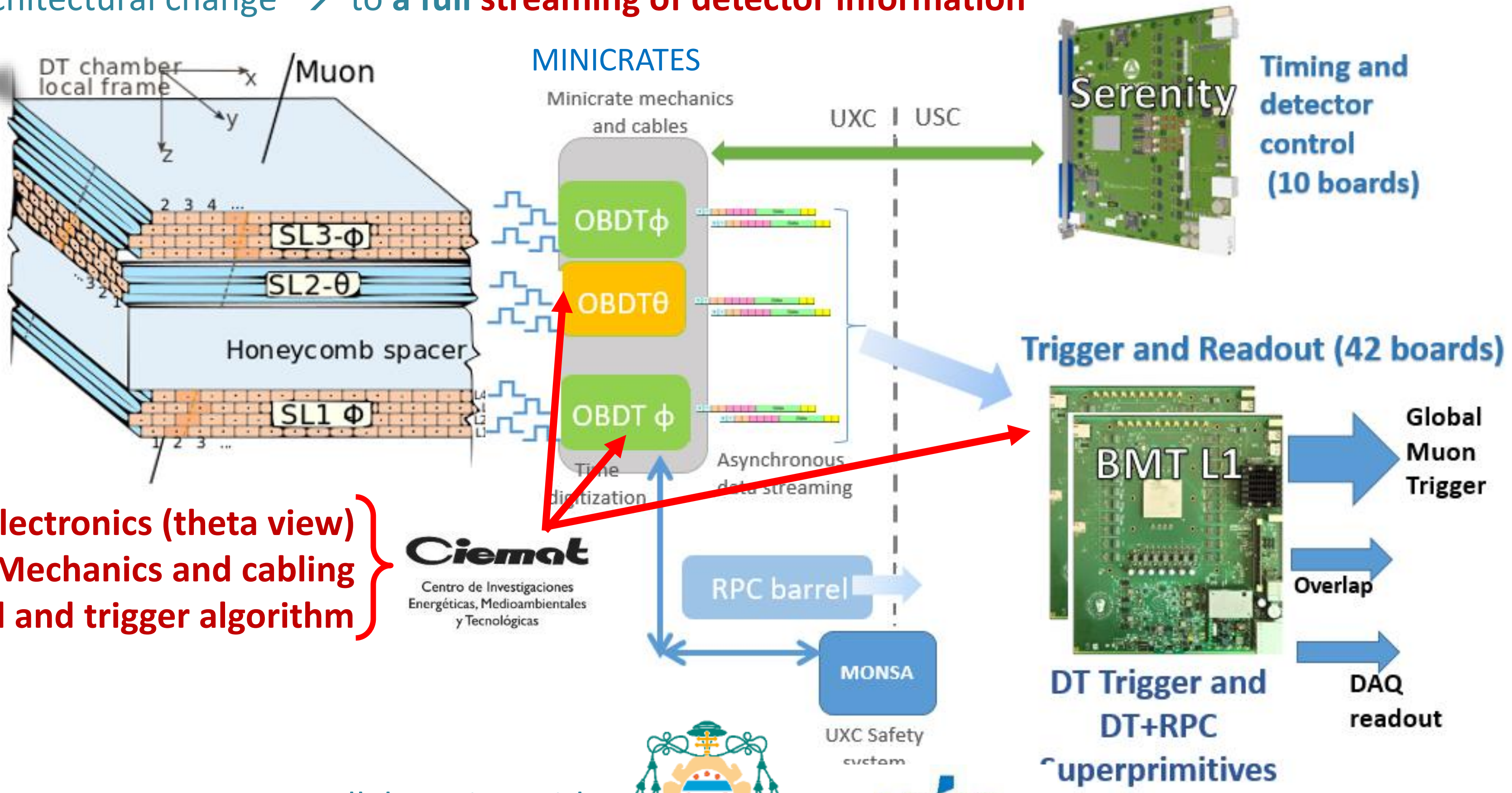

-Electronics (theta view)
-Mechanics and cabling
-Backend and trigger algorithm

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Collaboration with Universidad de Oviedo, UAM Universidad Autónoma de Madrid

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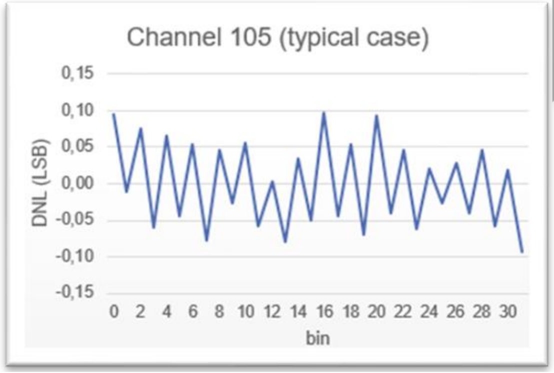
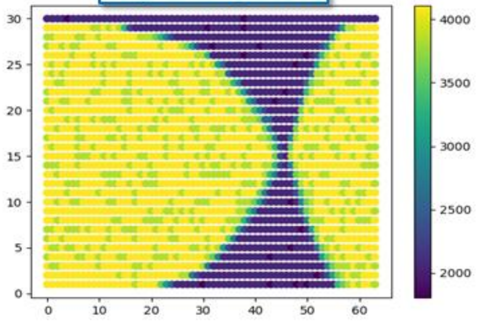
CMS Muon Phase 2: DT on detector electronics

- **Advanced and flexible readout board**
- **OBDT-theta board: designed and produced at CIEMAT**
- Time digitization on the FPGA (228 channels/board) at 0.7 ns. **Radiation tolerant FPGA Microsemi Polarfire**
- **High speed optical communication (10 Gbps/link),** total throughput available **~50 Gbps/board**
- Makes use of CERN ASICs: lpGBT (v1), SCA, VTRX
- Halogen free, radiation tested
- Automatic safety mechanisms embedded (temperature, current, voltage protections)

Excellent performance of the board

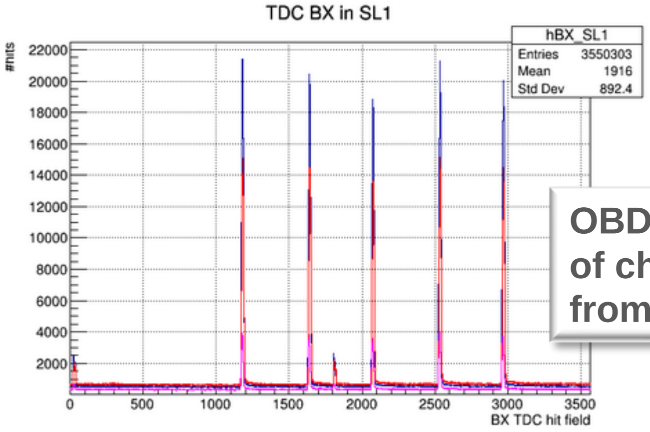


Eye Diagram



Radiation tests performed at CHARM (100Gy)

Board validated with collisions in CMS (Slice Test)



OBDT time measurements of chamber hits coming from LHC collisions in CMS

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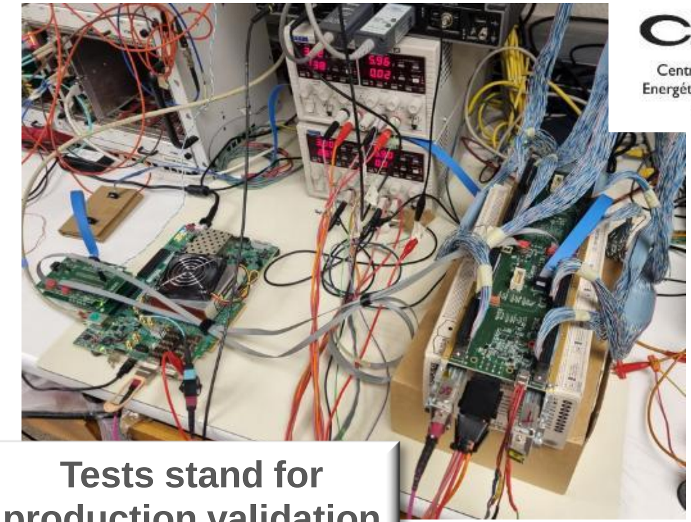
CMS Muon Phase 2: DT on detector electronics

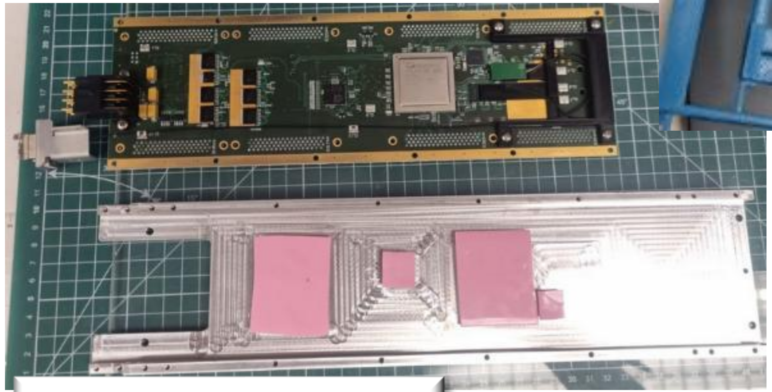
Boards passed burn-in tests (2 weeks@50ºC) to discard infant mortality on components

Production on-going 88% completed



Tests stand for production validation

3D printing for fiber routing. Validation of plastics under radiation



Mechanical pieces for the OBDT frame assembly

Small mechanical pieces and cables production completed (~10 kunits)

SND experiment

OBDT-theta being used also in other experiments (SND@LHC)

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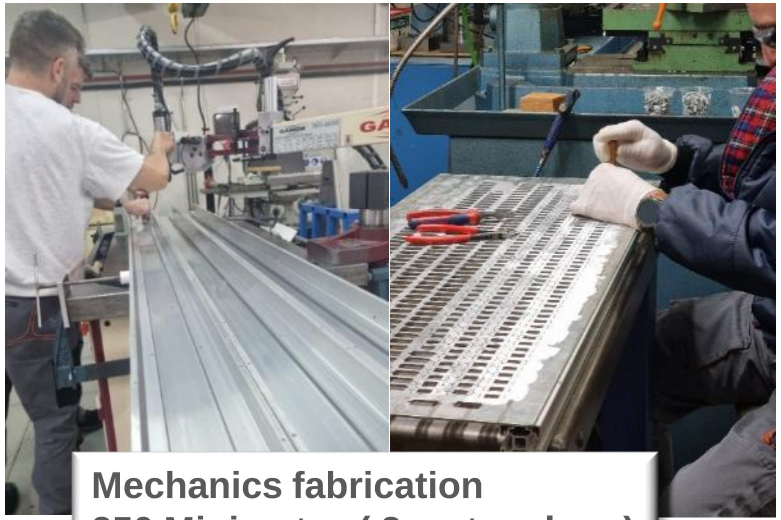
CMS Muon Phase 2: DT Minicrate mechanics, cables and assembly



Mechanics fabrication
250 Minicrates (2 meters long)
+ 800 different pieces

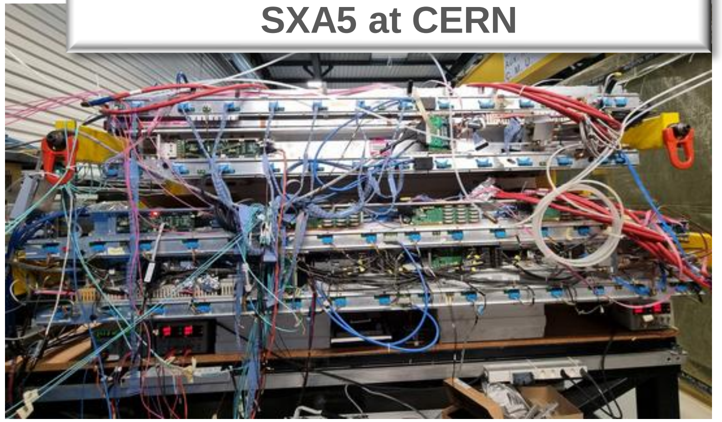
Cooling validation

Minicrate assembly hall at CIEMAT

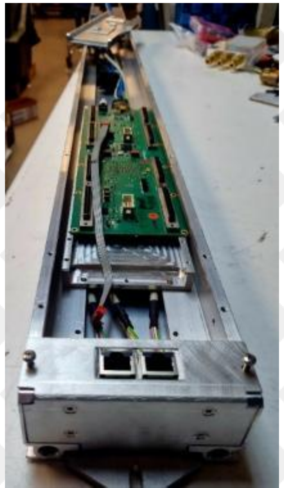
Installation exercises at CERN

Slice Test: two CMS sectors working in parallel with upgrade electronics

Cabling and integration tests at SXA5 at CERN



Launching Minicrate assembly and testing at CIEMAT site



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CMS Level 1 Trigger Phase 2 upgrade

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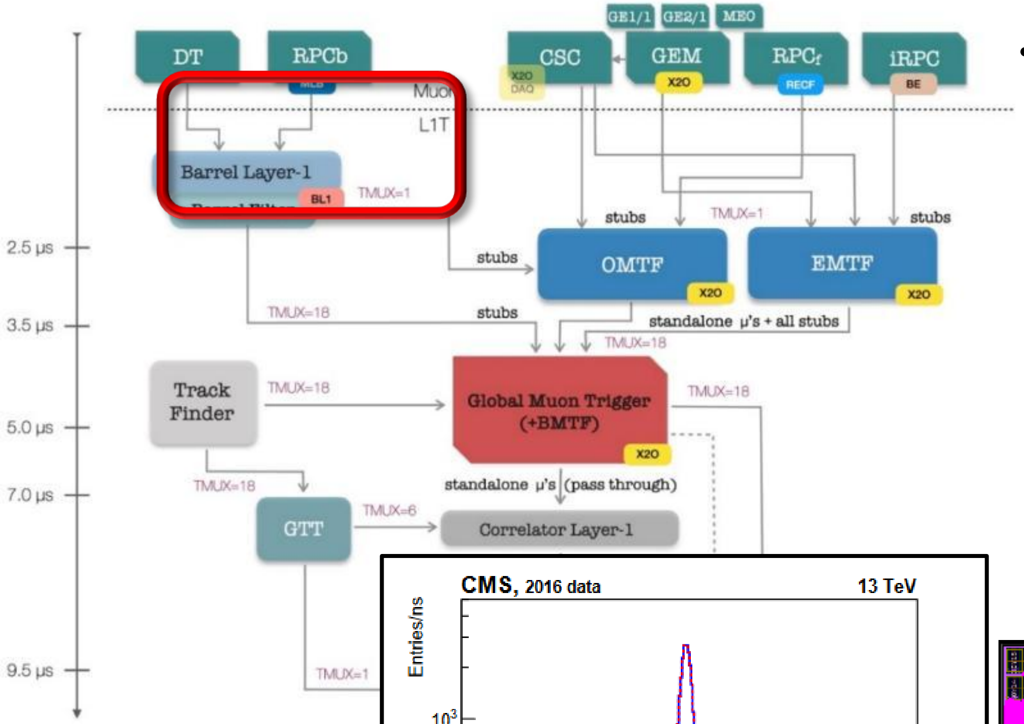

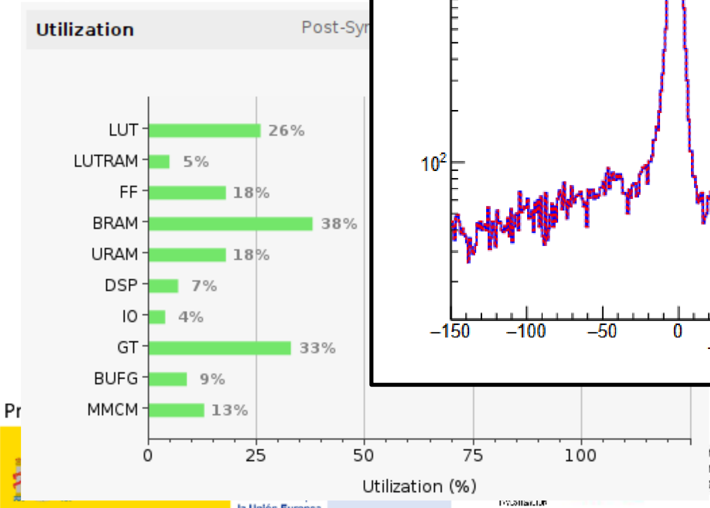

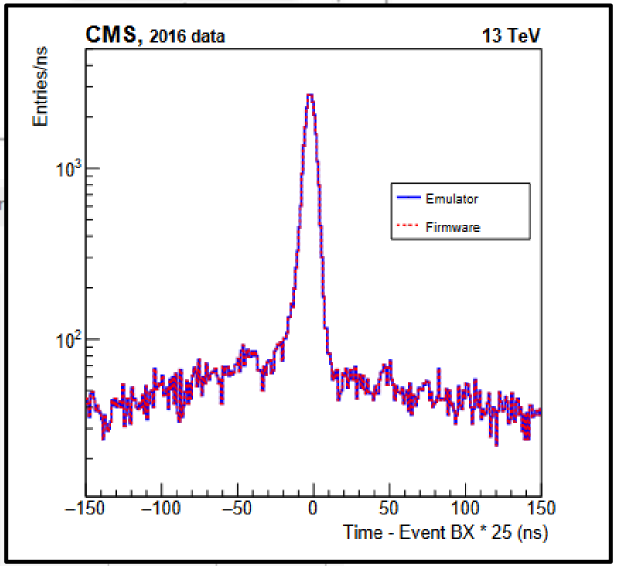

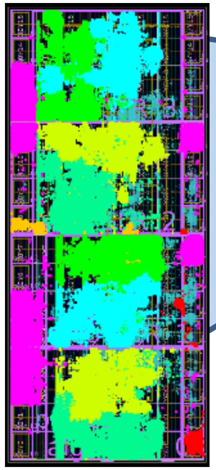

- **CIEMAT is responsible of the CMS Muon Barrel Trigger** primitive system for HL-LHC:
  - **Algorithm development** (complex muon track, combinatorial explosion, DT+RPC)
  - **Firmware implementation for trigger and DAQ**
  - **Construction of the hardware** system ATCA based in Spanish companies (installation and commissioning in 2027-2030)

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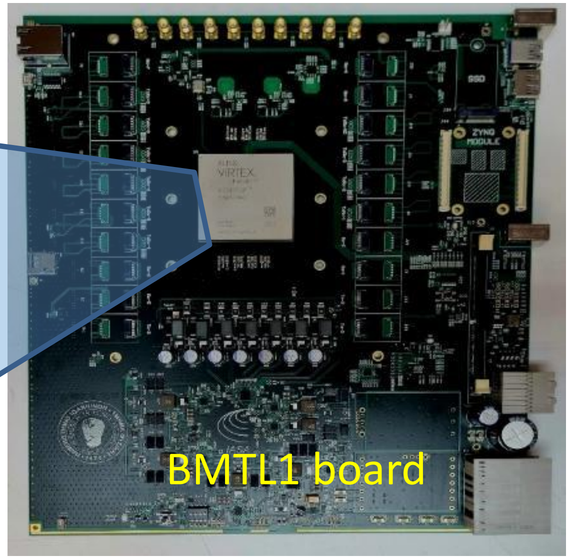
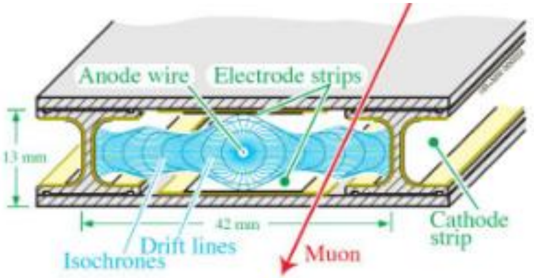
Hardware backend

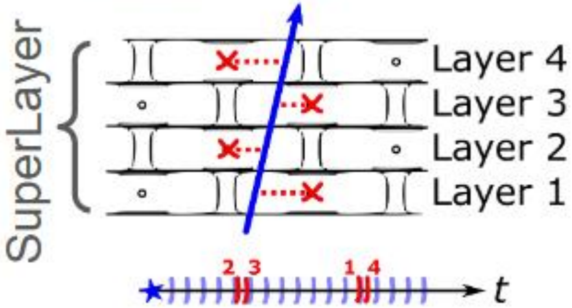


- 42 ATCA boards so called BMTL1
- Ultra high performance FPGAS: AMD VU13P
- Very high data throughput (3.8 Tpbs)
- Collaboration with Univ. Ioannina (PCB), CIEMAT (design of the firmware)
- Half of the production in Spanish industries

Funded by the European Union NextGenerationEU

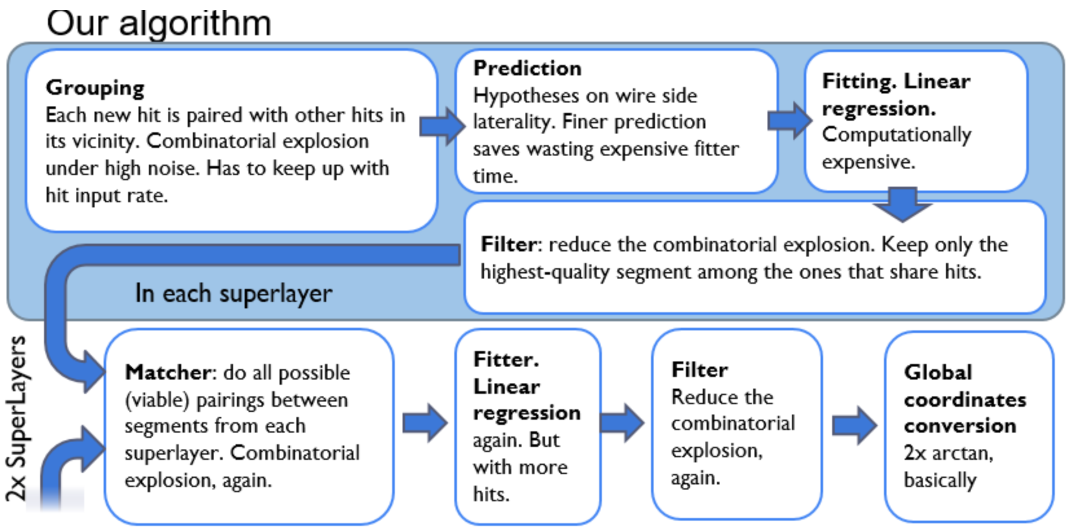
CMS Level 1 Trigger Phase 2 upgrade

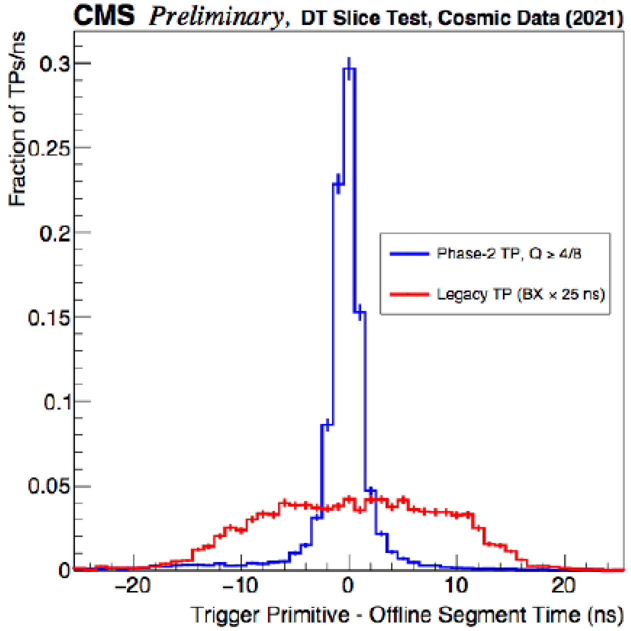


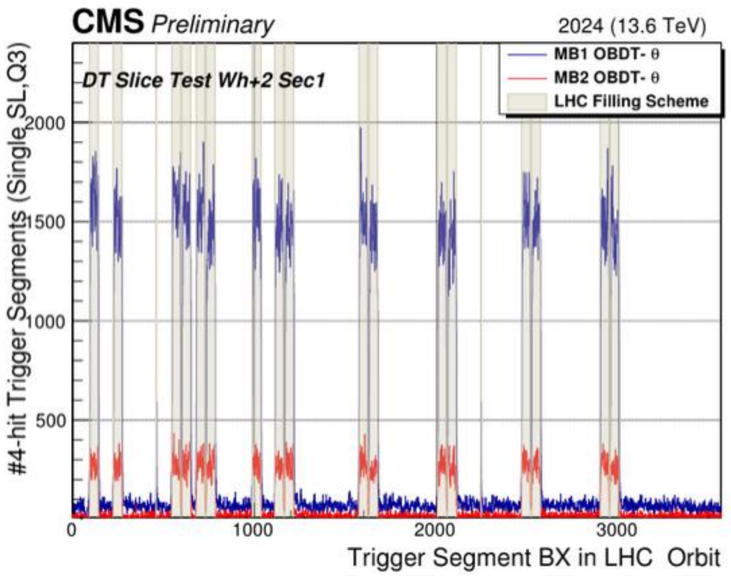


Muon trigger algorithm development

- **Analytical Method** has been developed to implement reconstruction of the barrel (DT+RPC) trigger primitives in HL-LHC
- Accepts all generated DT data at maximum resolution and builds segments. Deals with combinatorial explosion and complicated Drift Tube logic (unknown time tag with 400 ns uncertainty (time drift). It can only be obtained from the fit.
- **Exploits maximum achievable resolution**, bringing the hw system close to **offline performance capabilities**. [10.1016/j.nima.2023.168103]
- ➔ Enables HW **trigger on exotic signatures**: displaced muon triggers and showers
- Validated with proton-proton collisions at the CMS slice test







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Level-1 Muon Trigger Upgrades

Universidad de Oviedo

- Operations and maintenance of the Level-1 Overlap Muon Track Finder (OMTF):
  - Software, firmware, and shifts (online and offline).
- Collaborating with CIEMAT for Phase-2 Upgrade of the Barrel Muon Trigger (Layer-1 and Filter)
  - Software (theta view, integrating with CMSSW, Muon Shower tagging)
  - Firmware (Muon shower tagging).
  - Strong participation of Spanish community.
- Contributing to the firmware and software development for the Phase-2 OMTF upgrade (collaboration with U. Warsaw); and to the manufacturing of the X2O boards (collaboration with UFL and UCLA).
- Exploring alternative algorithms (i.e. GNN-based) for reconstructing LLPs using L1 muon trigger (using OMTF as a proof-of-concept).
- Responsibilities:
  - Offline software coordinator
  - Phase-2 Muon DPG contact
  - Trigger Resources Manager
  - Trigger Editorial Board

CIEMAT Contributions to CMS HGCAL (High Granularity Calorimeter)

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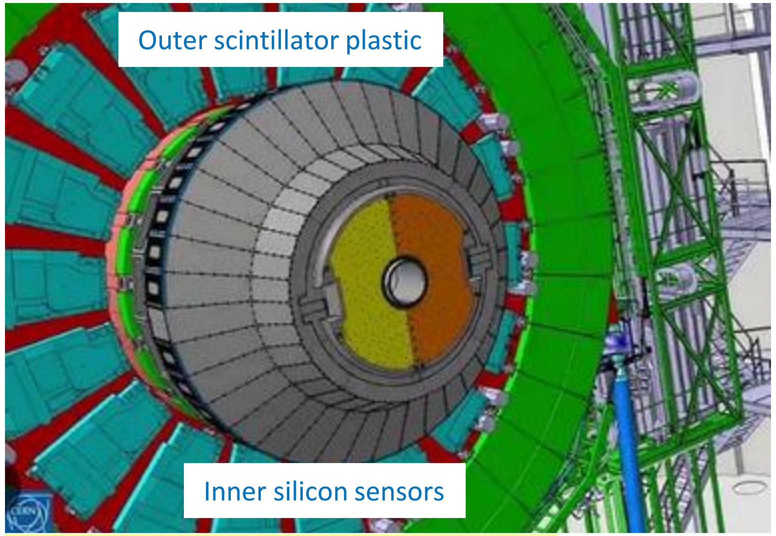

- HGCAL - An innovative project deploying many silicon tracker technologies in a calorimetry environment
- After Ukraine invasion, Russian institution collaboration with CERN and CMS in particular at risk: → Large participation from Russia on HGCAL.
- CIEMAT joined efforts to ensure building this detector timely.
- Therefore, several contributions taking place that involve Spanish industries

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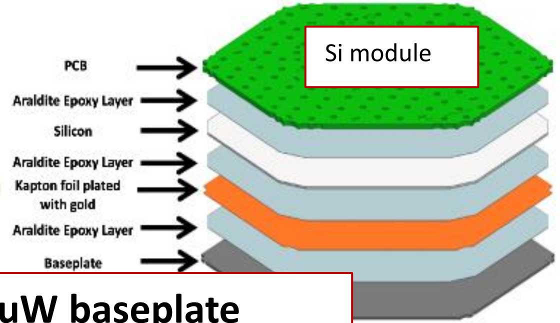
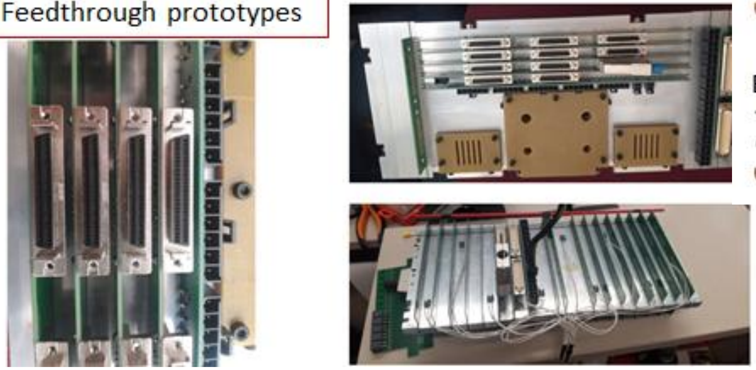


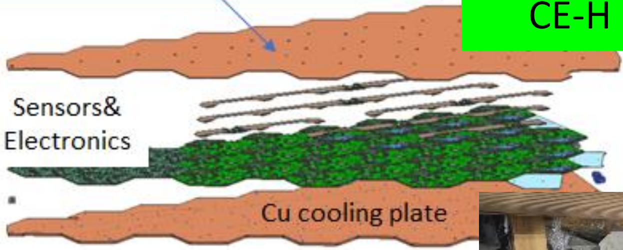
CuW baseplate

Machine ~1000 CuW thermal interface baseplates for HGCAL Si modules

Production of ~1200 PCBs allowing services cross the HGCAL thermal screen

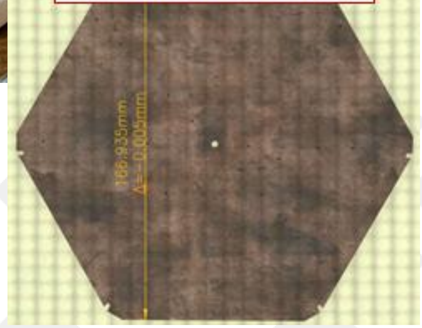
Feedthrough prototypes





Produce a fraction of steel protection covers of the CE-H HGCAL cassettes

CIEMAT CuW prototype



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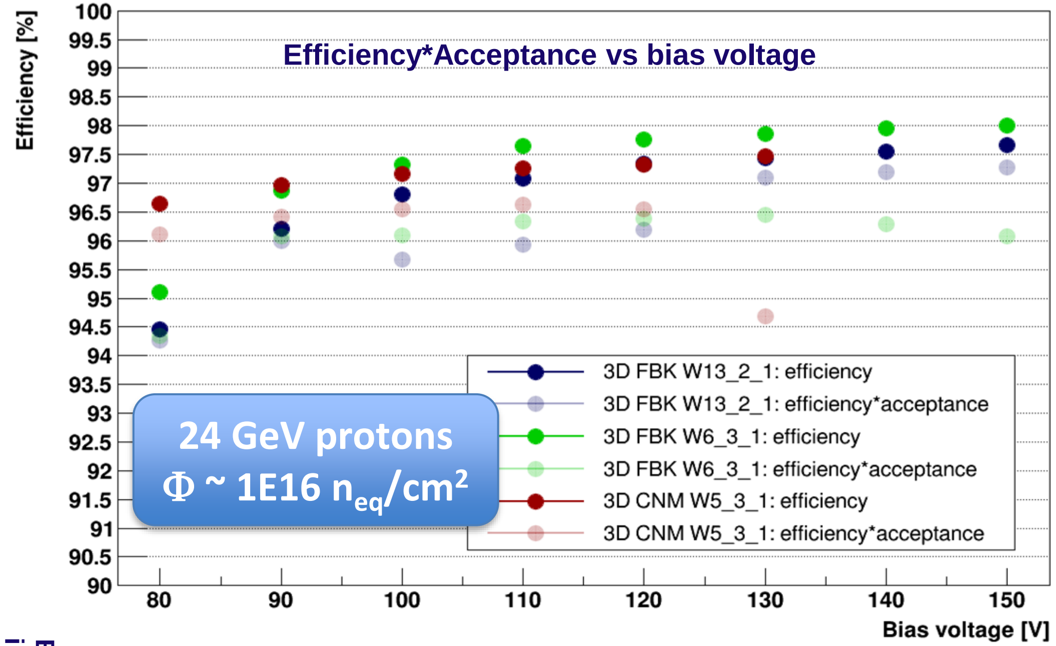
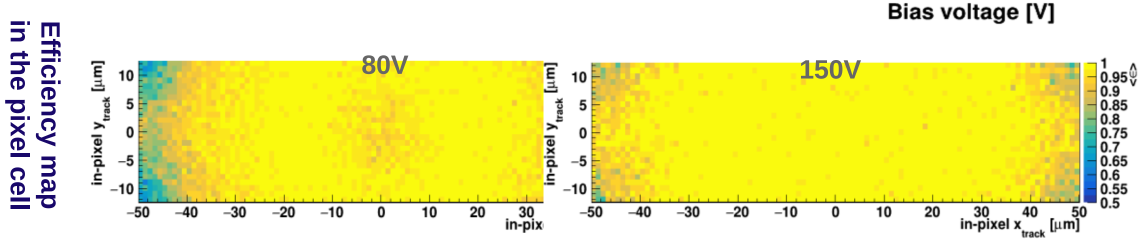
CMS Inner Tracker Upgrade: 3D pixel activities

- Characterization of 3D sensor radiation tolerance in TB campaigns
- **IT TBPX L1 to be implemented with 3D 25x100 μm pixel sensors**

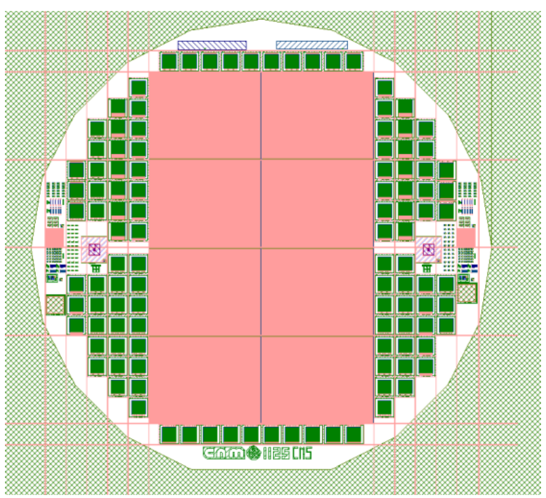
Efficiency at normal incidence: higher than 97% for all the modules after full depletion.

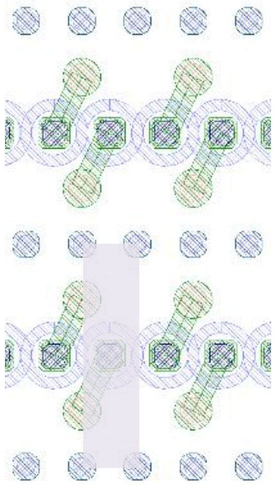
- Modules tuned to average thresholds of 1000e- at T≃-30º
- The **efficiency plateau starts at around 90V**
  → operation range: around 40V for CNM and 50V for FBK modules.

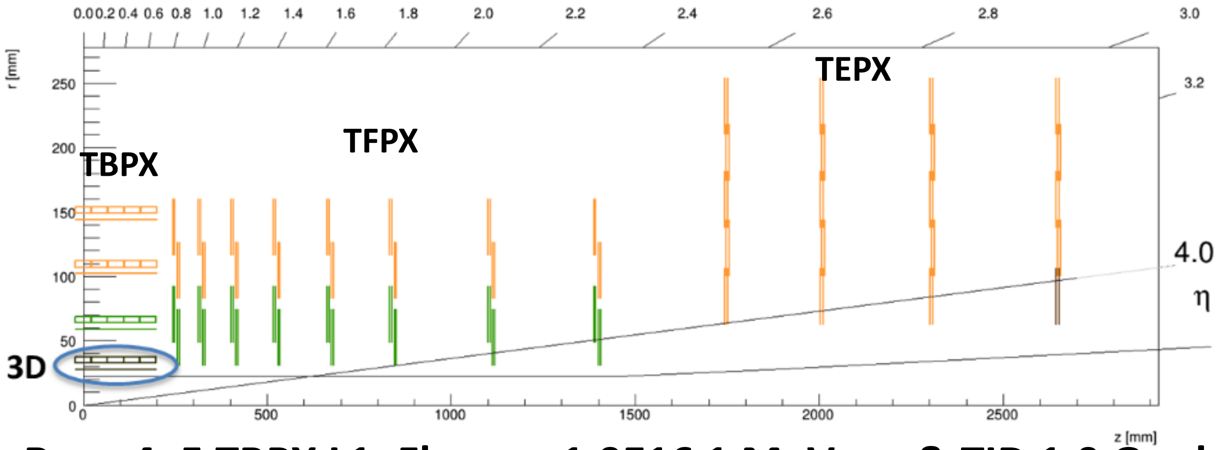




CNM: 100 mm SiSi wafers (150+200 μm)
8 CROC singles 25x100 (p-stop)







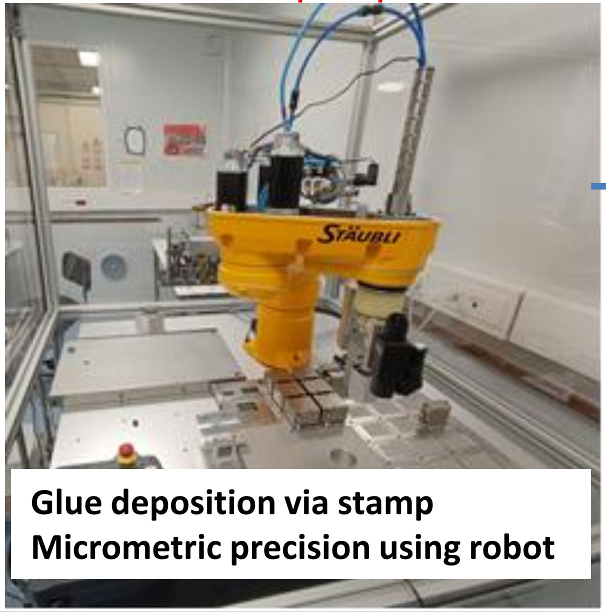
Runs 4+5 TBPX L1: Fluence 1.9E16 1 MeV n_{eq} & TID 1.0 Grad

IFCA coordinates CMS IT sensor group since 2018

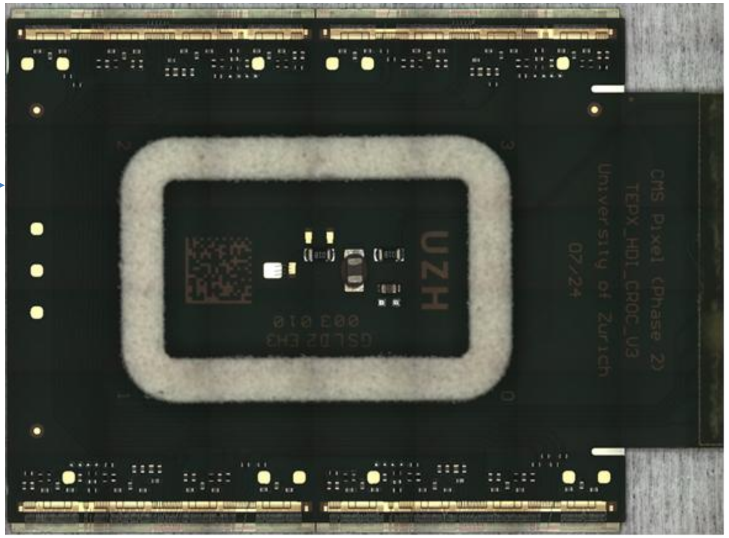
CMS IT modules

IFCA will assemble:

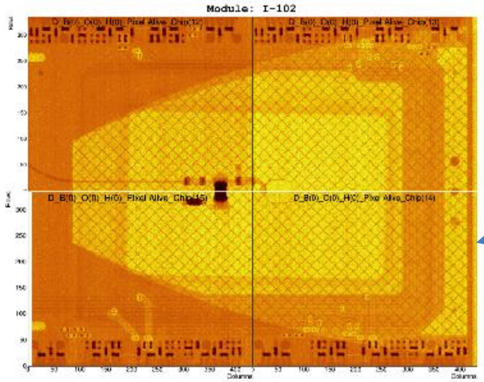
- **~ 400 TEPX 2x2 modules** (planar sensors)
- So far: 26 pre-production modules assembled and tested



Glue deposition via stamp
Micrometric precision using robot



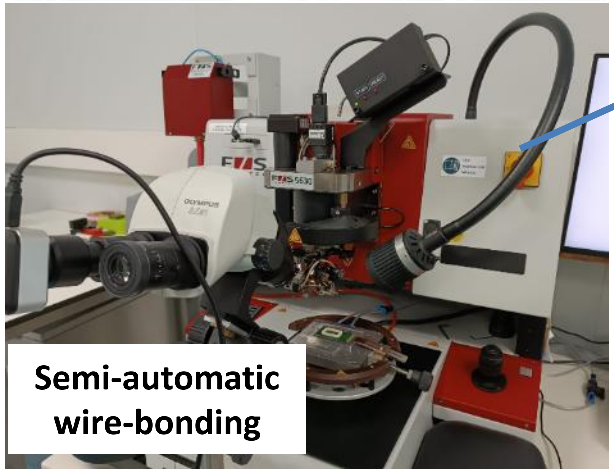
Wire bonding: ~200 wire bonds / ASIC (~800 / module)



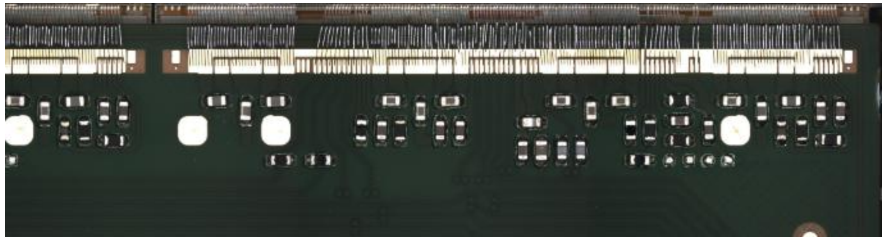
X-ray

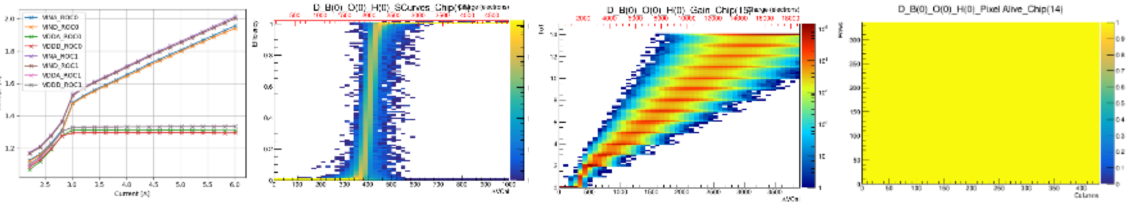
Module QC

- Pull tests on dedicated wire bond pads
- Thermal cycles in cold box
- CMS DAQ readout for system tests
- X-ray tests for pixel hit map

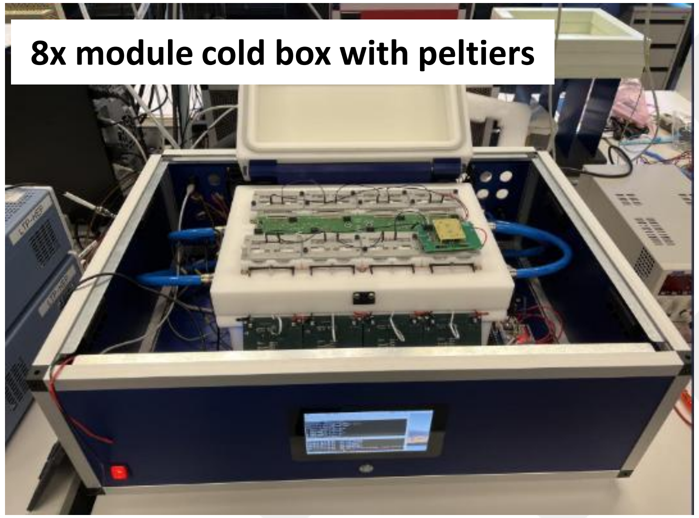


Semi-automatic wire-bonding





8x module cold box with peltiers



FE, HDI, EMC, Serial Power

- CROC simulation models & ETROC testing (ASICs)
- CMS Pixel & ETL System prototyping & EMC

Parasitic layout inductance effects.

Output transient response – CROC simulation

DEFAULT SIMS CONFIGURATION:

RD53C / CROCv2

I_power = 1.0 A (each SLDO)

Voffset = 1V

Vin = 1.5V

C_in = 6 uF in total

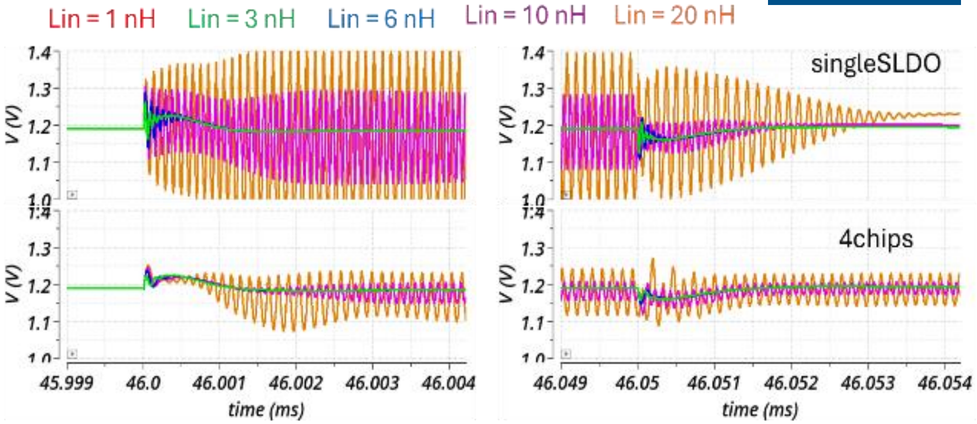
(1.5uF per chip in 4chips in parallel).

C_out = 2.2 uF

L_in = L_out = 1 nH (parasitic inductances)

R_load = 1.5 ohm (I load = 0.8A with 1.2V)

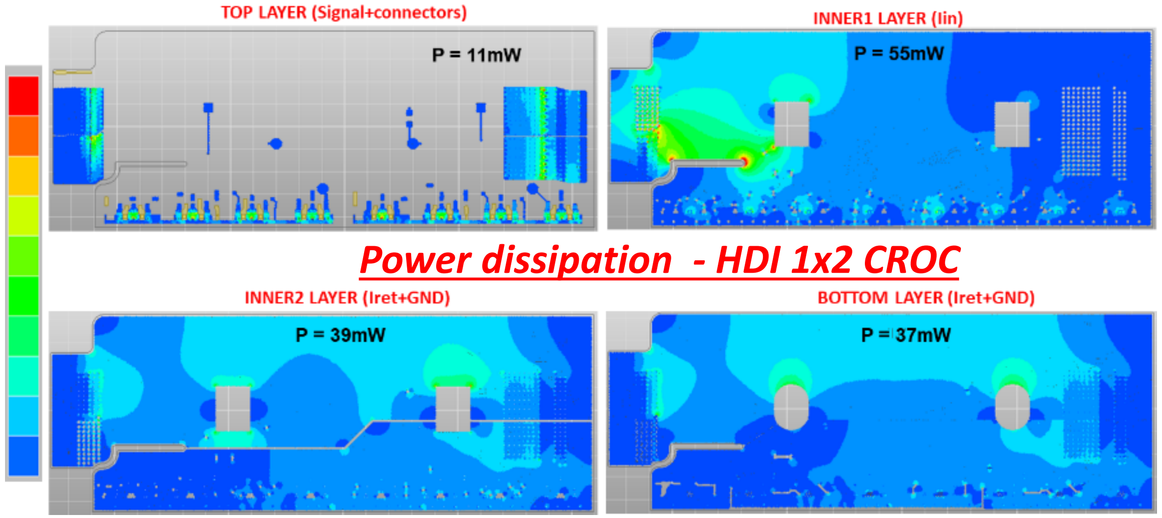
Temp = 25C



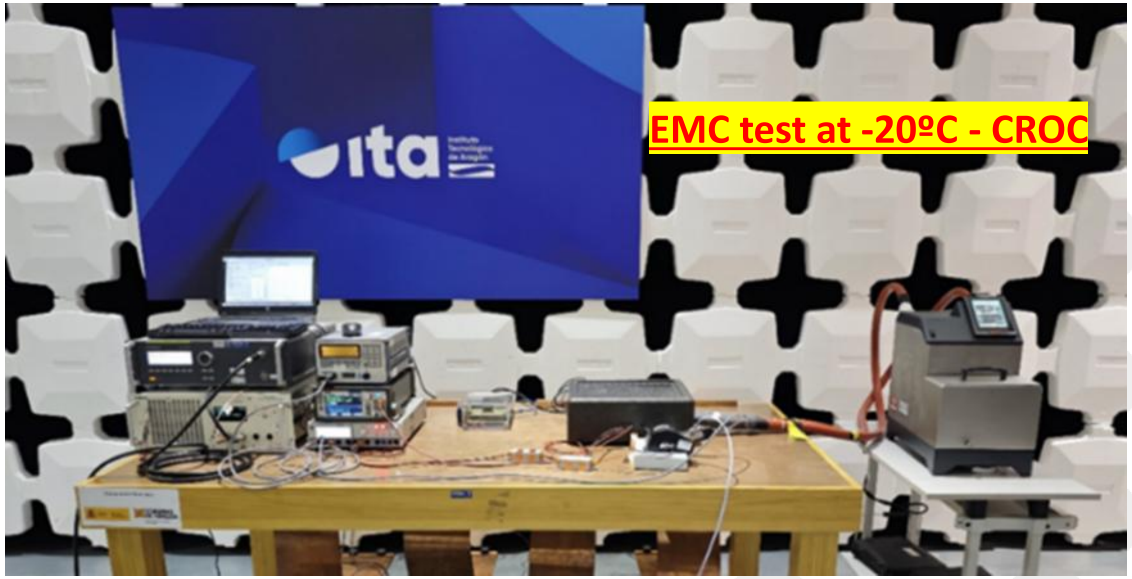
LOAD TRANSIENT = 0.8 A → 0.2 A → 0.8 A

- -40C is worst case. SLDO gets unstable with **>5nH** in 4chips configuration
- Connecting SLDO in parallel makes the system less stable

1x2 HDI final version simulation:



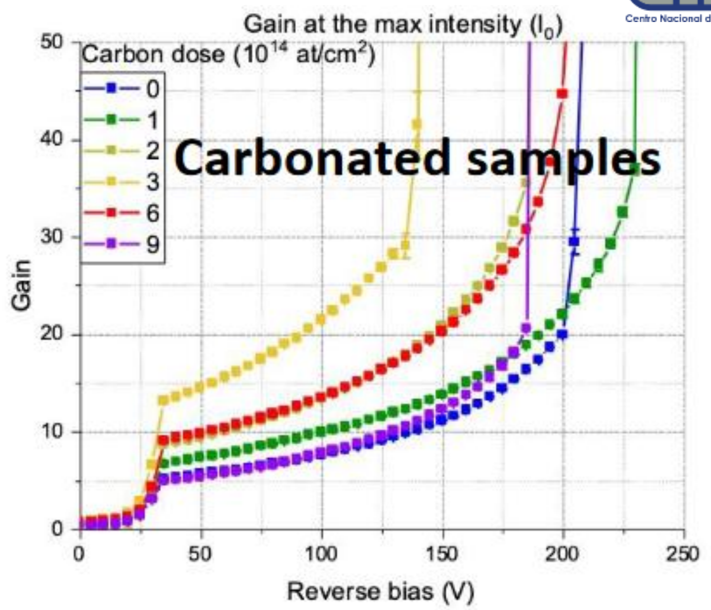
Power dissipation - HDI 1x2 CROC

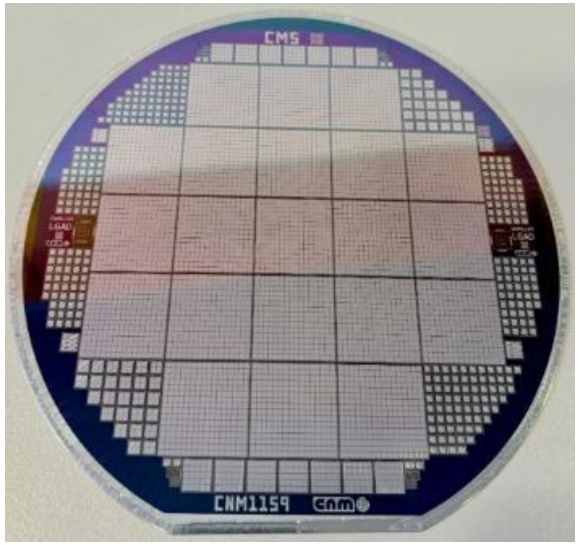


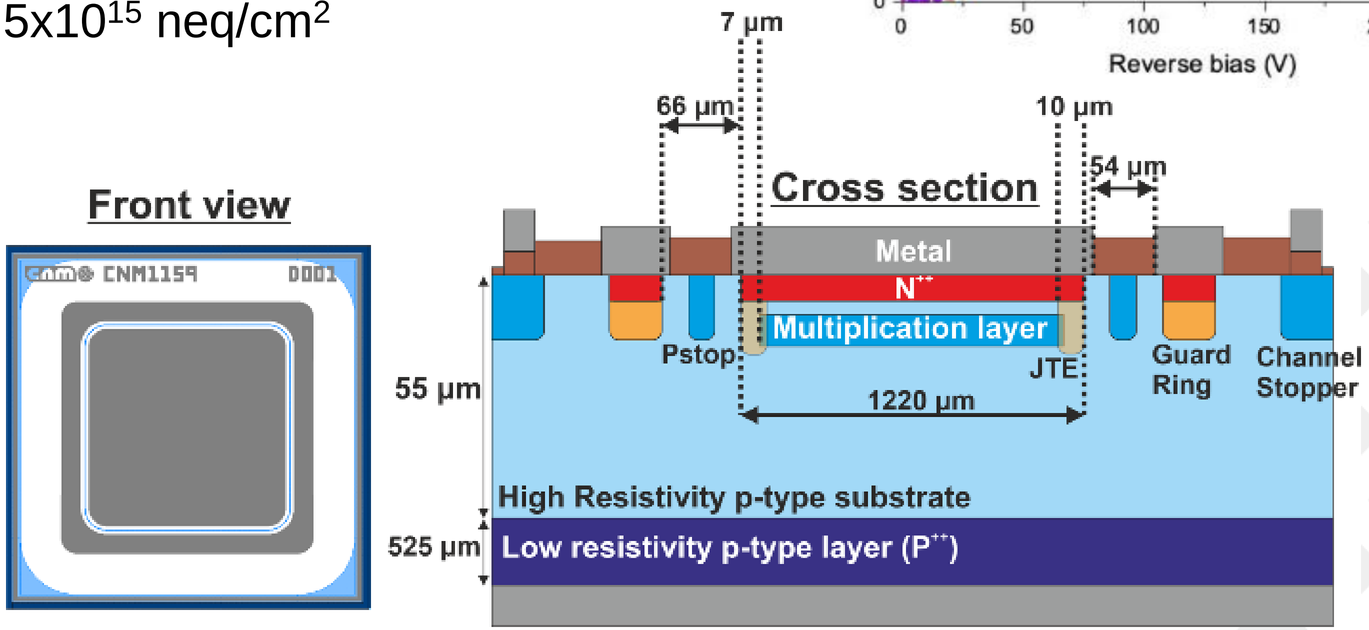
EMC test at -20ºC - CROC

CMS ETL: LGAD sensor R&D

- Optimization of the Carbon dose to improve the radiation tolerance
- Carbonated LGAD matching final sensor specifications for ETL manufactured at IMB-CNM
- Full characterization carried out with Radioactive source and SPS test beam at CERN
- Compliant with performance and ration tolerance requirements for the ETL
  - Q>8fC and σ_t<50 ps @ f = 1.5×10^{15} neq/cm^2







ETL-ETROC2

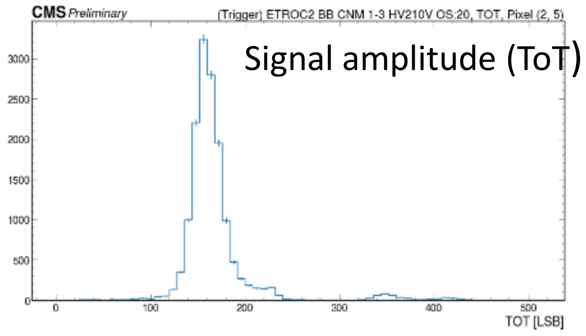
- **Major project milestone** : First version of a full fledged readout ASIC (ETROC2) arrived in March.
- Bump bonding (IMB-CNM and Baretek) of first batch ETROC2 batch to 16x16 LGAD prototype sensors completed in August
- Very low noise levels present, overcoming previous ETROC version major issue.
- Test beam at the CERN North Area and laser testing at CERN SSD laser facility carried out in the second half of September

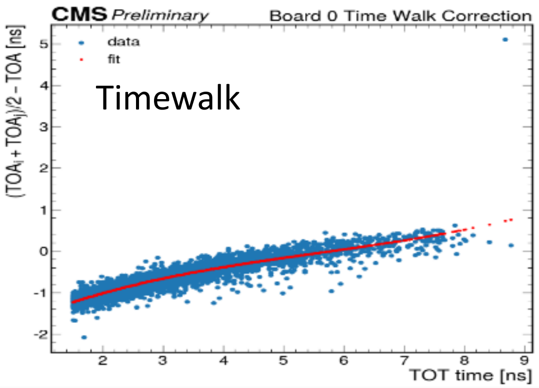
Fully self contained, self referential sensor+ETROC2 stack system at SPS TB. Three sensor layers with accompanying master clock board and FPGA DAQ.

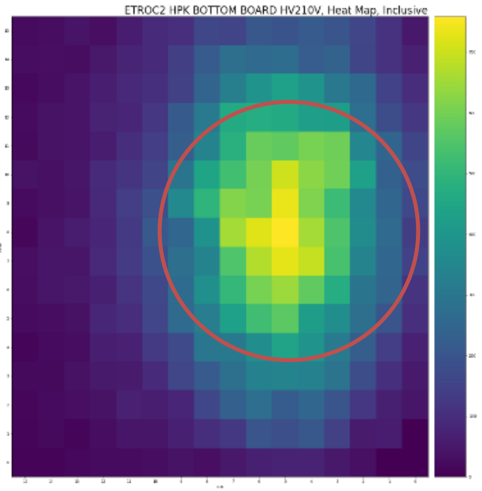
Fully functional ETROC2+sensor assembly (SSD laser facility) for dedicated jitter studies and ETROC2 performance

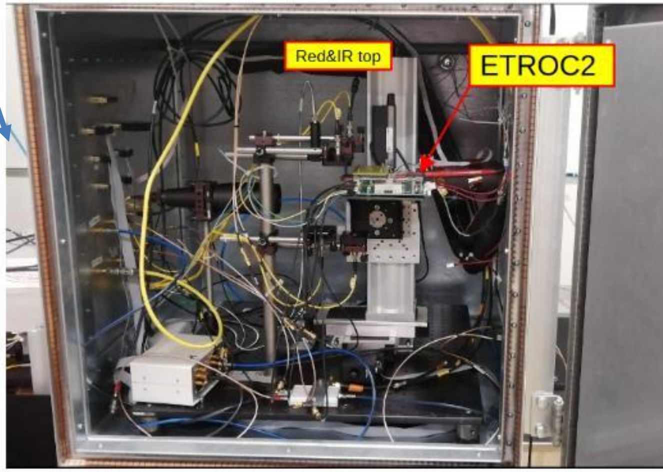
- Very promising out-the-box performance: SPS beam profiling and track correlation observed.
- Preliminary determination of the ETROC2 assembly jitter using the laser: < 30 ps.

beamspot



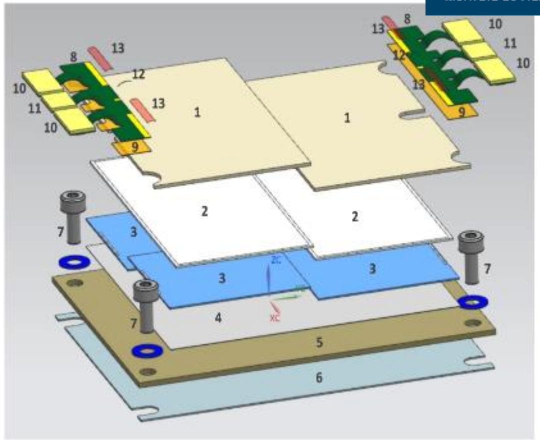


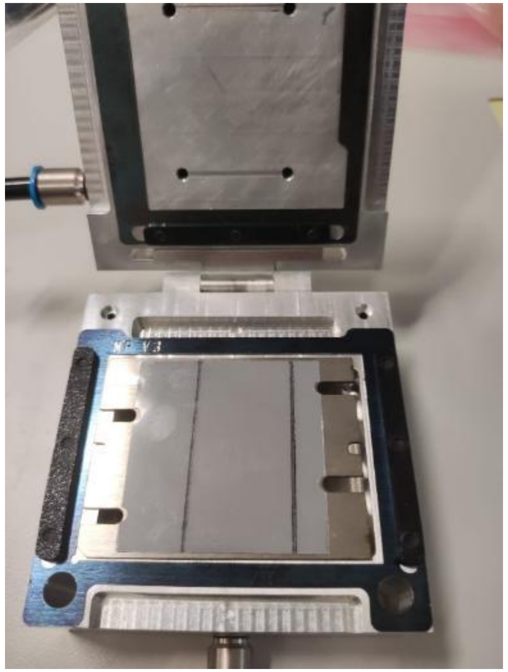


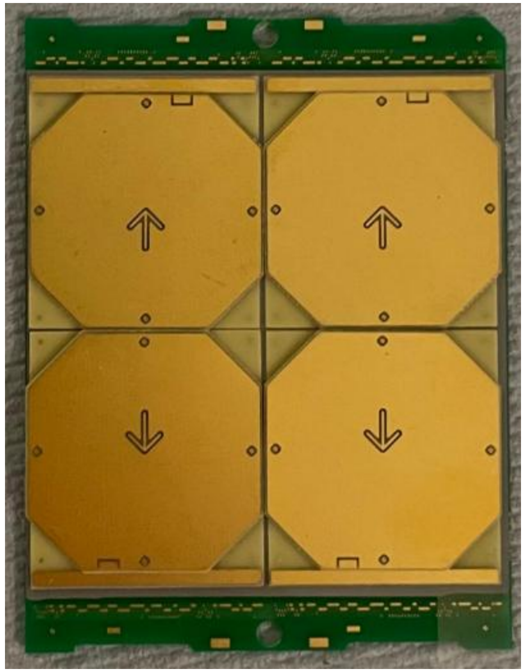


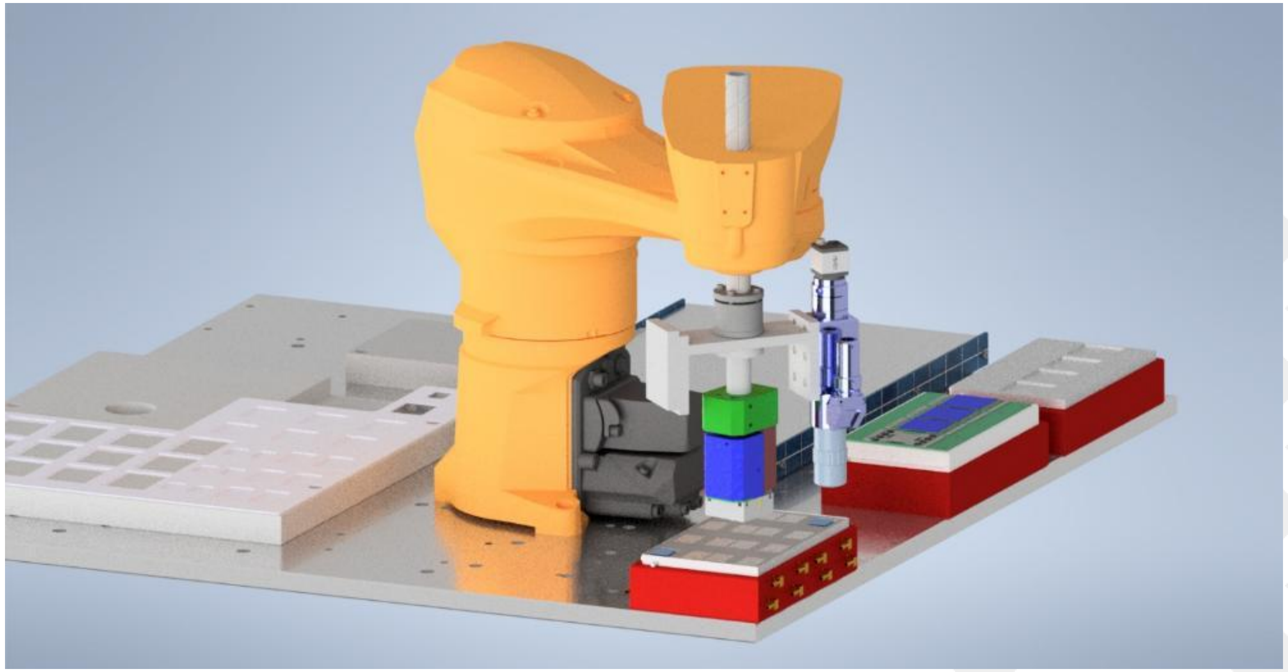
ETL Module Assembly

- IFCA will assemble ~900 (~10%) Endcap Timing Layer modules
- Workflow established in collaboration with other sites (Nebraska, Fermilab and Torino)
- Automated procedure based on a SCARA ROBOT to ensure precision
- Integrate digital camera and AI recognition of fiducial mark positions
- First mockup assemblies during first manual step using precision jigs
- Waiting for LGAD+ETROC bare modules to start pre-production
- Wire bonding and testing of modules performed on-site





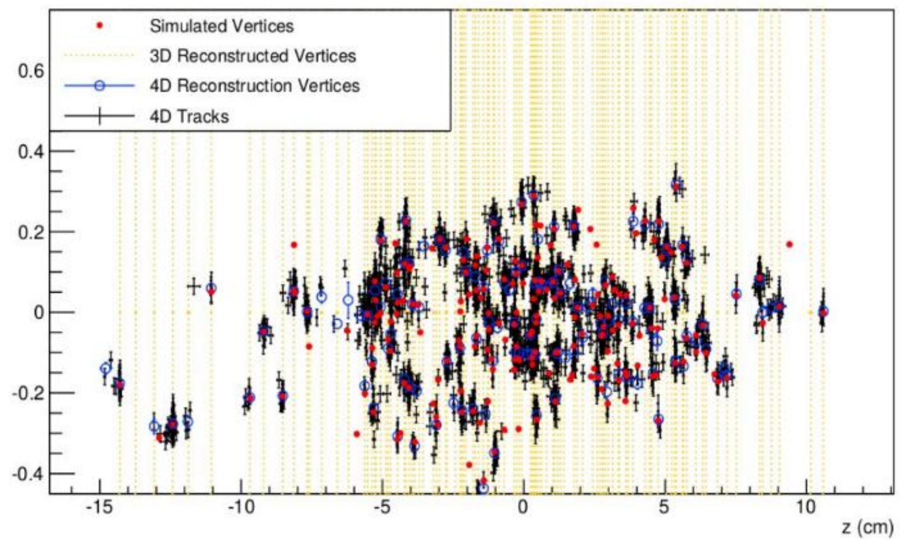


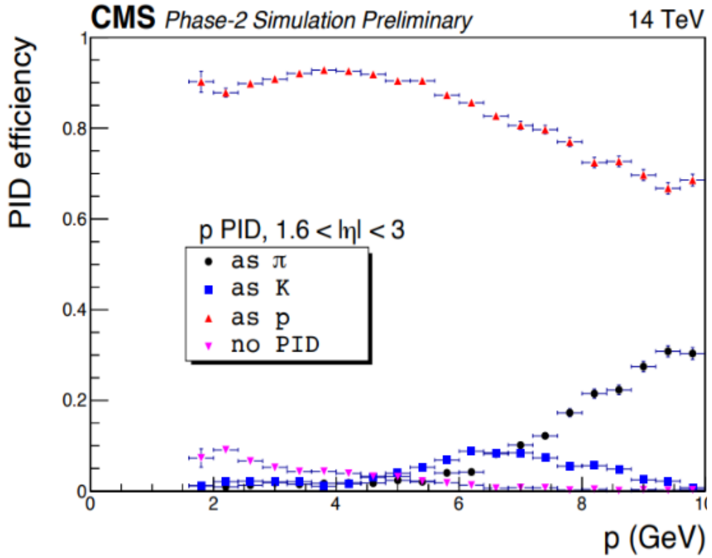


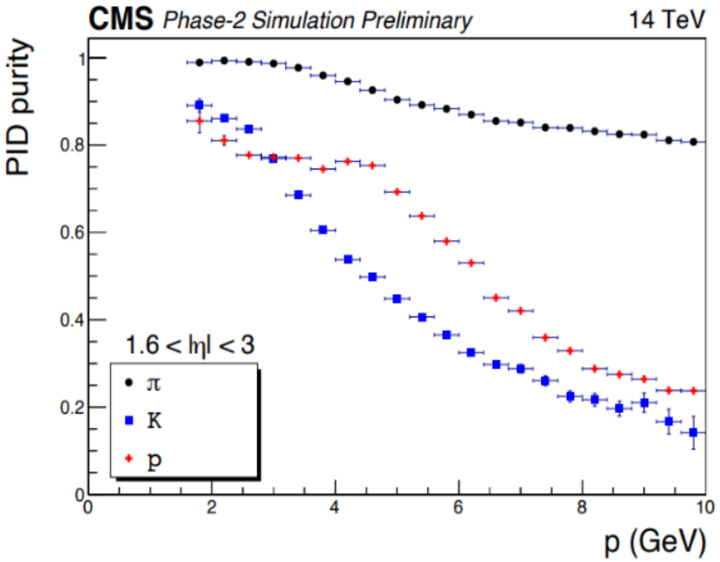
MTD Geometry, Reconstruction and Physics Case

- In charge of the Data Performance Group of the MTD (2019 – 2023)
- Implementation and optimization of the detector geometry in CMSSW
- Digitization and detector response (new ETL response model in progress)
- Local reconstruction, 4D global reconstruction and 4D vertex building
- Calibration procedures and alignment

- New physics cases studied
- Extension of searches for long-lived particles decaying into displaced jets
- Use of timing information to estimate Particle ID (Time-Of-Flight-based Particle ID)
- Strong impact on B physics analysis as it improves the particle tagging performances

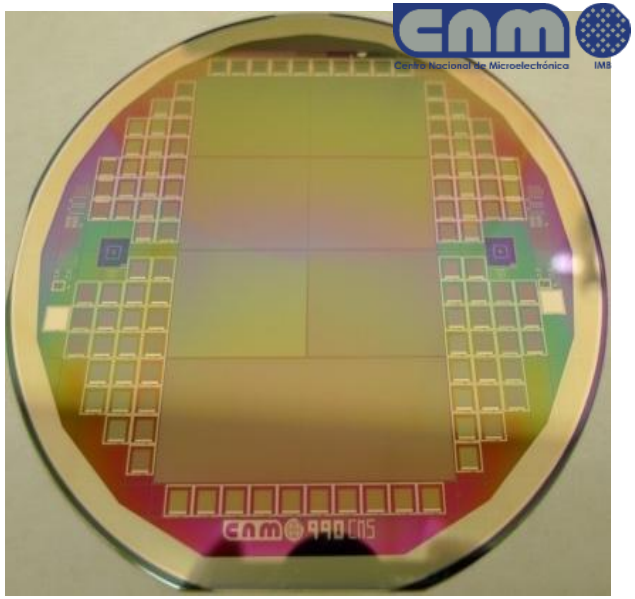


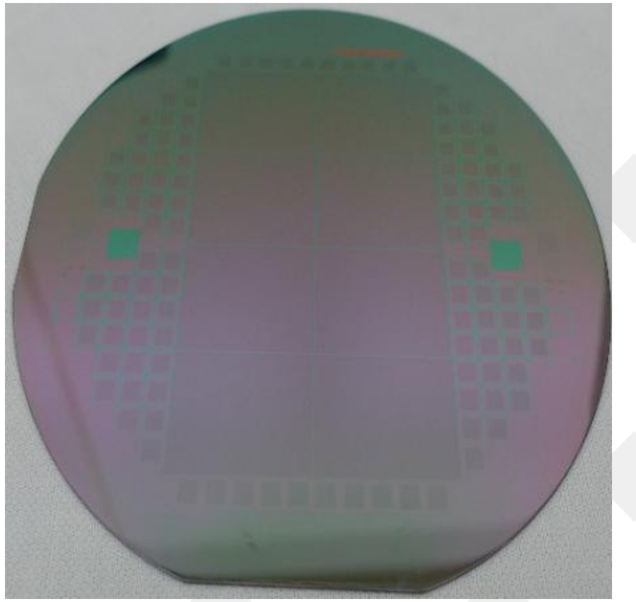




IMB-CNM. CMS Activities

- Fabrication of 3D sensors
  - Improve the fabrication yield of 3D pixel detectors to produce sensors for the CMS Inner Tracker upgrade
  - Production of 3D detectors based on the new 3D single side technology developed at IMB-CNM
    - 3D Technology stabilization
    - 3D-CROC First prototypes
      - Cell pitch: 50x50 µm2, 25x100 µm2
      - 1 Electrode configuration (1E)
  - CMS selected the 3D sensors to instrument part of the Inner Tracker



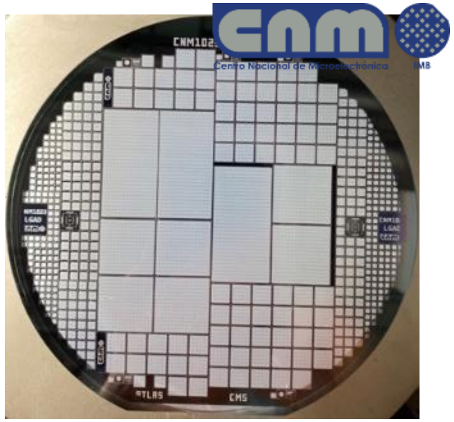


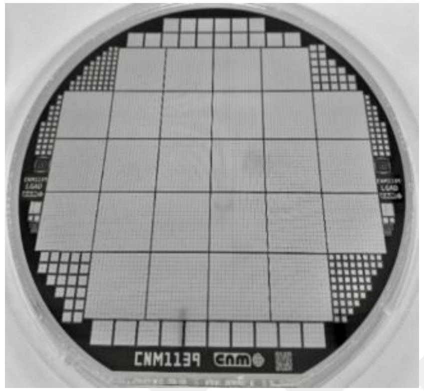
CMS Market Survey and Tendering

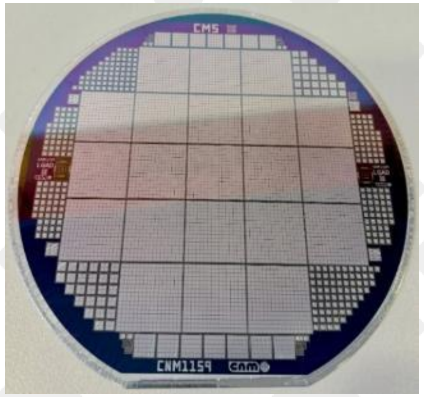
- IMB-CNM was qualified as a supplier of 3D detectors for CMS in the Market Survey
- However, in the tendering process, FBK detectors were selected due to their lower price
- Similar for ATLAS-ITk

IMB-CNM. CMS Activities

- Fabrication of LGADs sensors
  - Detectors produced in 150 mm epitaxial wafers (50 µm active thickness)
  - 16x16 matrix design (1.3x1.3 mm2 pad area)
  - Fabricated according to the CMS Market Survey specifications
    - LGADs on epitaxial substrates (6LG3, 15x15, 16x16, 15x30, 16x32 pixels)
    - LGADs with Carbon (6LG2, standard doping profile (15x15, 16x16), deep doping profile (16x16))
      - More resistant to radiation, more stable breakdown voltage and gain values
      - Temporal resolutions in the order of 35 ps
      - Prototypes irradiated with @ $1.5\text{x}10^{15}$ n_{eq}/cm^2 CC > 8 fC and a time resolution < 50 ps @ 12 V/µm (CMS technical requirements)
      - Large area prototypes (15x15 and 16x16 pixels, 2.5x2.5 cm2) show increasing yields (50%, 94%, and 99%) as manufacturing is repeated and stabilized
  - CMS selected the LGAD sensors to instrument the future End Cap Timing Layer





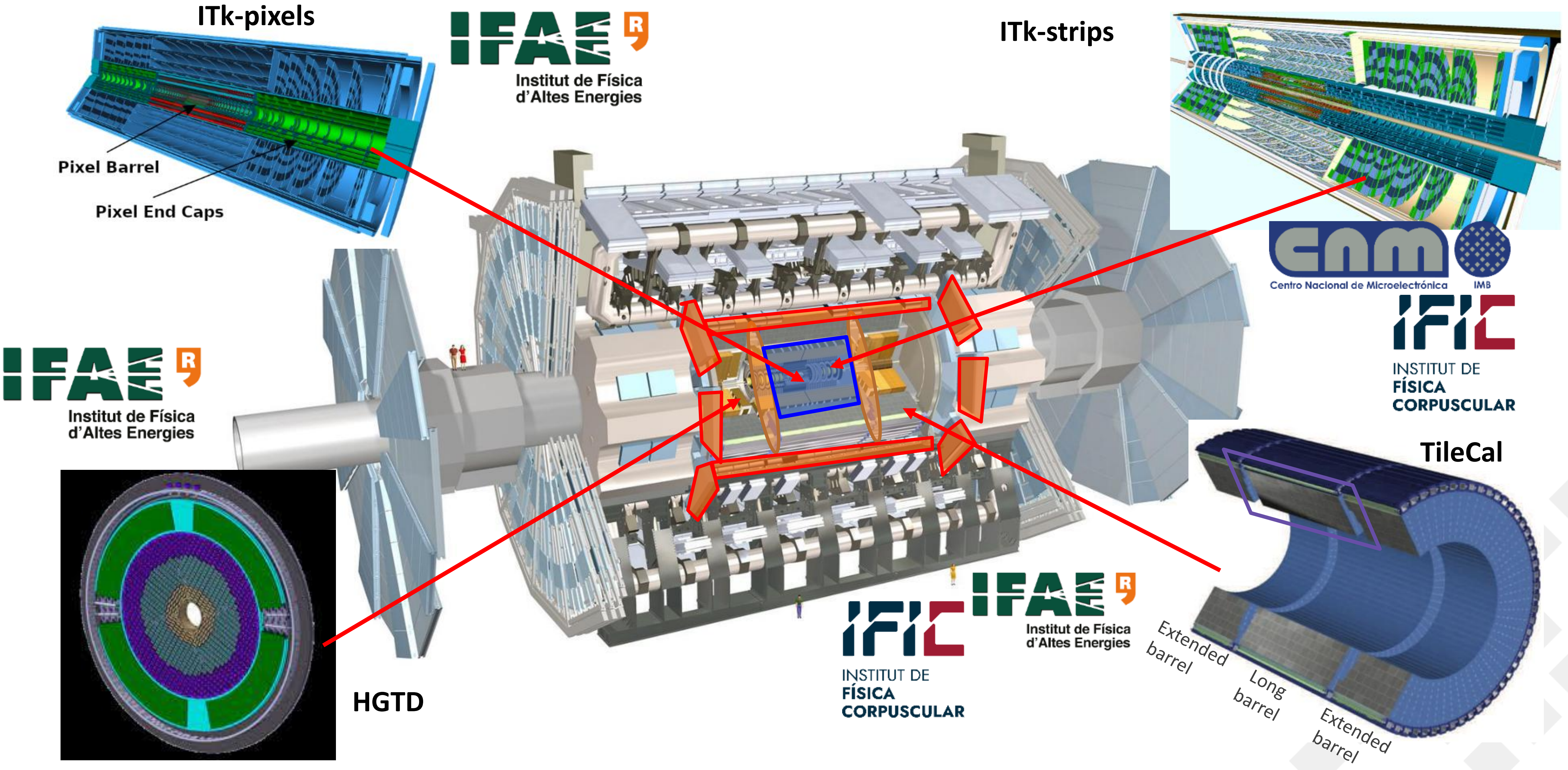


CMS Market Survey and Tendering

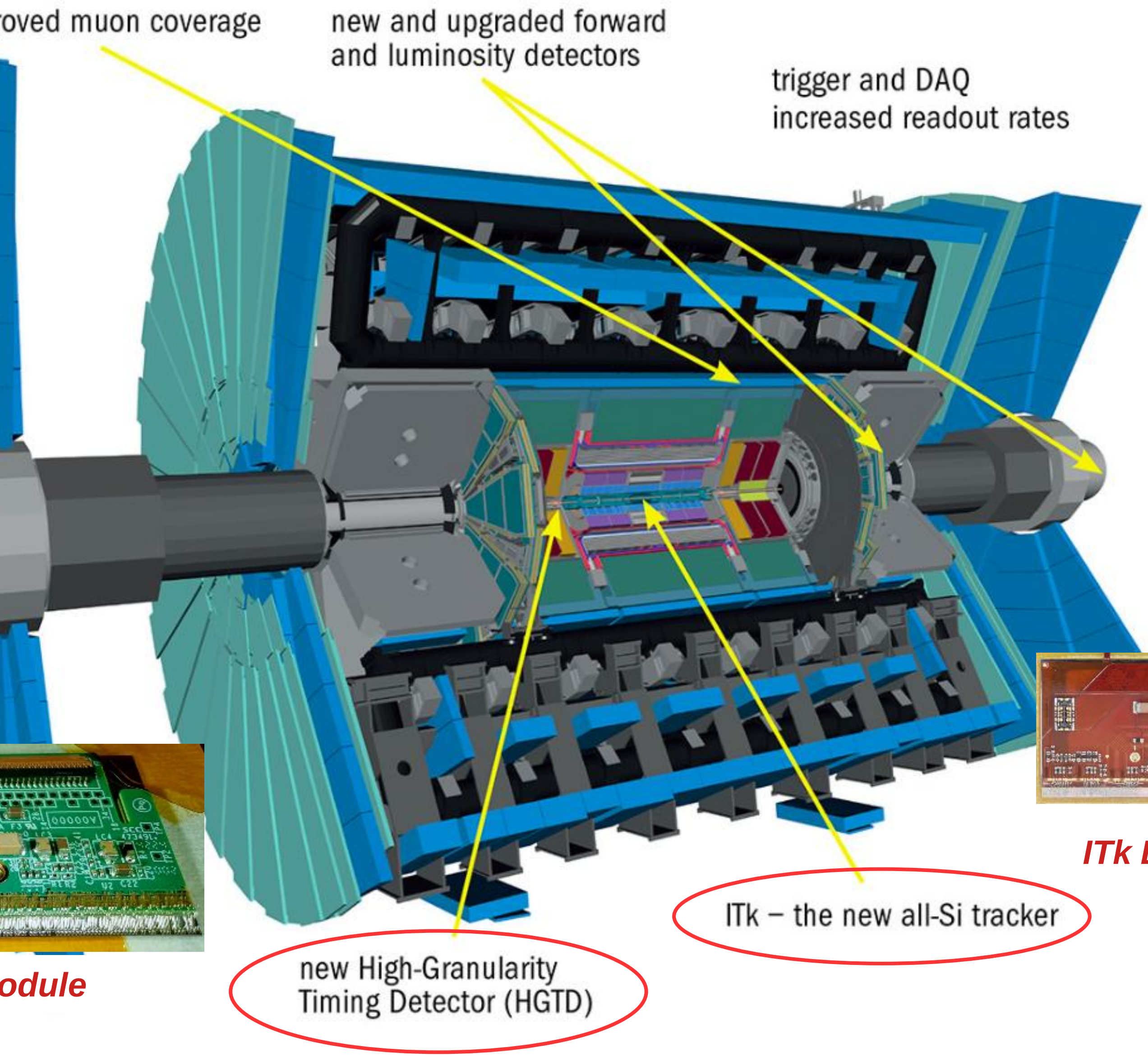
- IMB-CNM fulfilled ETL specification but was not selected as supplier
- HPK was selected for the outer layer of the ETL, with the inner layer awaiting accreditation from Lfoundry (Tendering)
- For ATLAS IMB-CNM did not accomplished specifications

- TileCal
- ITk-strips
- ITk-pixels
- HGTD

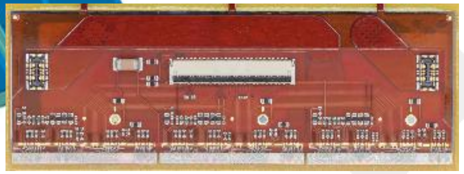
ATLAS Upgrade



Overview: Goals and Status



HGTD Module

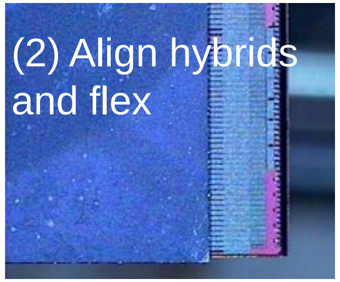


ITk Linear Pixel Triplet module

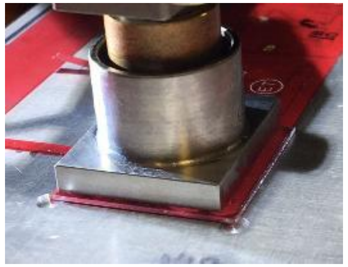
ATLAS ITk Pixel Triplet Module Assembly

- In the past we worked on pixel **sensor R&D**, **prototyping** & **qualification**
- Finished **qualification** and **pre-production**

- ITk 3D hybrid
- 25x100 um2 for linear triplet
- Triplet flexible PCB



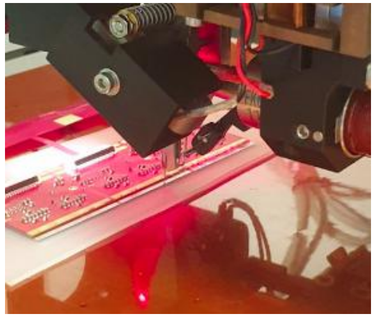
(3) Place hybrid on flex



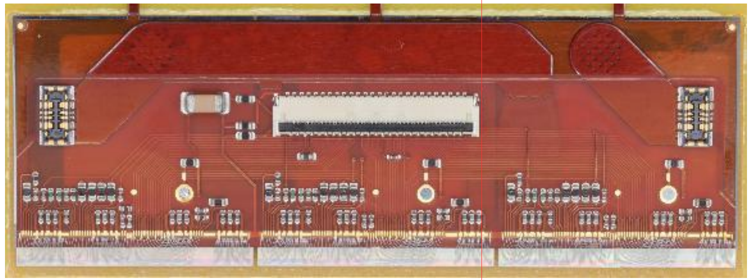
Several metrology steps

- Length, rotation, Flatness, Glue coverage

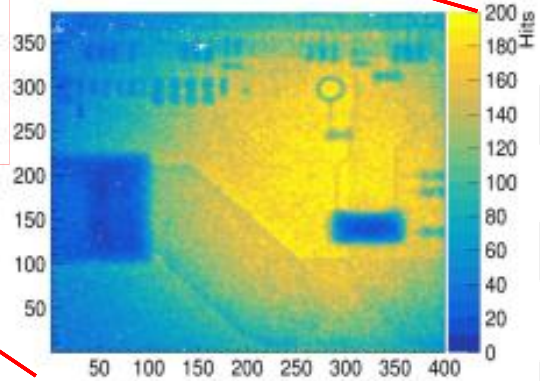
(5) Wire-bond



(6) Metrology



(7) Testing: Threshold tuning, Detection with Sr90, Thermal cycling, etc

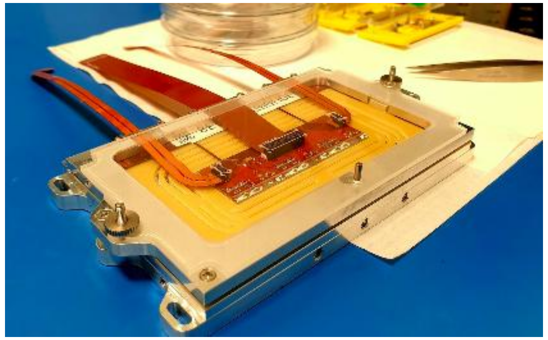


N. Kakoty, https://doi.org/10.1088/1748-0221/20/06/C06028

ATLAS ITk Pixel Triplet Module Pre-production

- Linear triplet pre-production finished **IFAE** (11 shipped to CERN/SLAC) ✓
- Out of **11** pre-production triplets only **1** had critical failure (ASIC readout)
- Production to start early 2026

Short Name	Metrology of Parts	Assembly	Metrology	Wire Bonding	Pull-test	Visual Inspection	Initial Tests	Warm Tests	Cold Tests	Thermal Cycling	Stability	Test after Stability	Final Warm	Final Cold	Final	Shipped	Location	Hybrids
IFAE-Pre-0	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	SLAC	SINTEF-IZM
IFAE-Pre-1	Yes	Yes	Yes	Yes	Yes	Yes	FAIL	NO	NO	NO	NO	NO	NO	NO	NO	Yes	Berkeley/SLAC	FBK-LND
IFAE-Pre-2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	SLAC	FBK-LND
IFAE-Pre-3	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	SLAC	FBK-LND
IFAE-Pre-4	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	SLAC	FBK-LND
IFAE-Pre-5	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	NO	NO	NO	NO	NO	Yes	Yes	SLAC	FBK-LND
IFAE-Pre-6	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	NO	NO	NO	NO	NO	Yes	Yes	SLAC	FBK-LND
IFAE-Pre-7	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	NO	NO	NO	NO	Yes	Yes	SLAC	FBK-IZM
IFAE-Pre-8	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	SLAC	FBK-IZM
IFAE-Pre-9	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	SLAC	FBK-IZM
IFAE-Pre-10	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	Yes	Yes	Partial	Yes	Yes	SLAC	FBK-IZM
IFAE-Pre-11	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	NO	NO	NO	NO	NO	NO	NO	CERN	FBK-IZM
IFAE-Pre-12	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes			IFAE	SINTEF-IZM
IFAE-Pre-13	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes			IFAE	SINTEF-IZM
IFAE-Pre-14	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes								CERN	FBK-LND
IFAE-Pre-15	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Partial	Yes	Yes	Yes	Next				CERN	FBK-LND
IFAE-Pre-16	Partial	Yes	Yes	Yes	No	Yes	Yes	Yes	No								IFAE	FBK-LND
IFAE-Pre-17	Partial	Yes	Yes	Yes	No	Yes	Yes	Yes	No								IFAE	FBK-LND
IFAE-Pre-18	Partial	Yes	Yes	Yes	No	Yes											IFAE	FBK-IZM V2 50

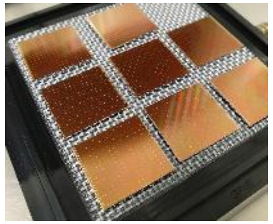


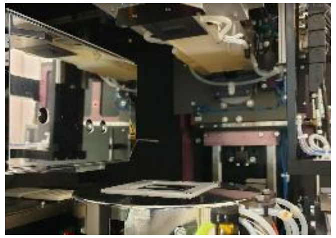
- Triplet production (*final modules*): **133 triplet modules** for the **innermost pixel layer** (committed rate: 2 modules/week)
- Also commitment to 3D **sensor QA** (with CNM)
- We are ready for the production phase
    - Waiting for hybrids...

ATLAS HGTD Module Assembly

- Worked on **sensor R&D**, **ASIC design**, **hybridization**, prototyping & **qualification**
- IFAE completed prototype **hybridization** and **assembly qualification** for HGTD

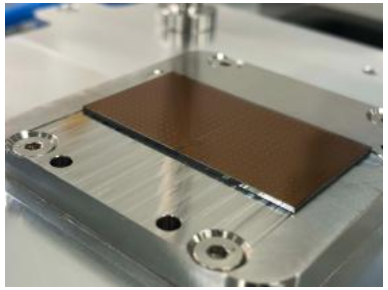
Hybridization **(in house)**

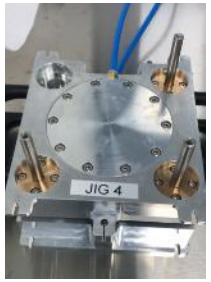




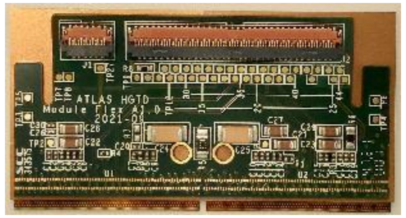
Contribution to ASIC design and LGAD development (CNM)

Flex/hybrid alignment and gluing

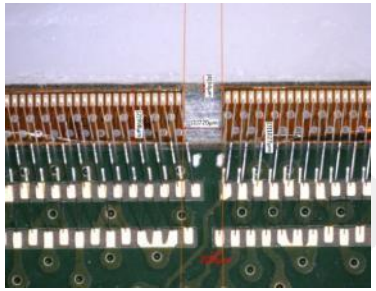




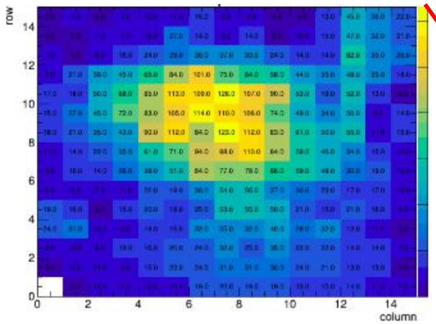
Metrology

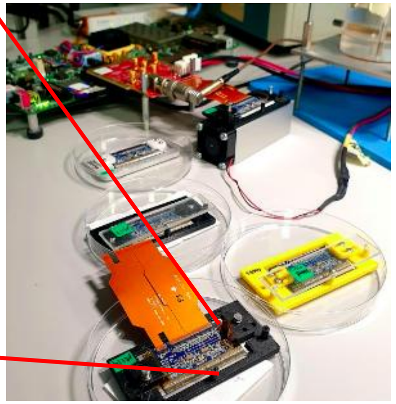


Wire-bonding and pull tests



Final module testing





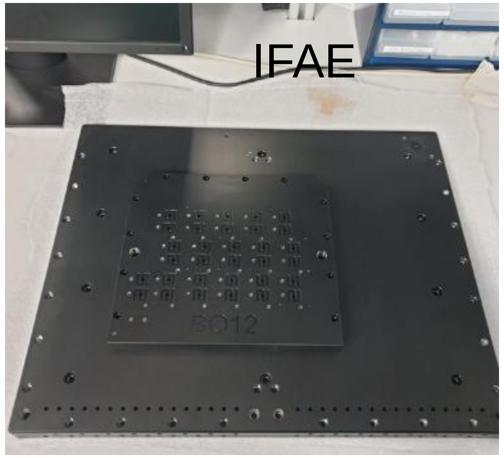
Alvin readout system developed at IFAE (for **lab** & **beam tests**)

V. Gautram, https://doi.org/10.22323/1.463.0009

ATLAS HGTD Module Status

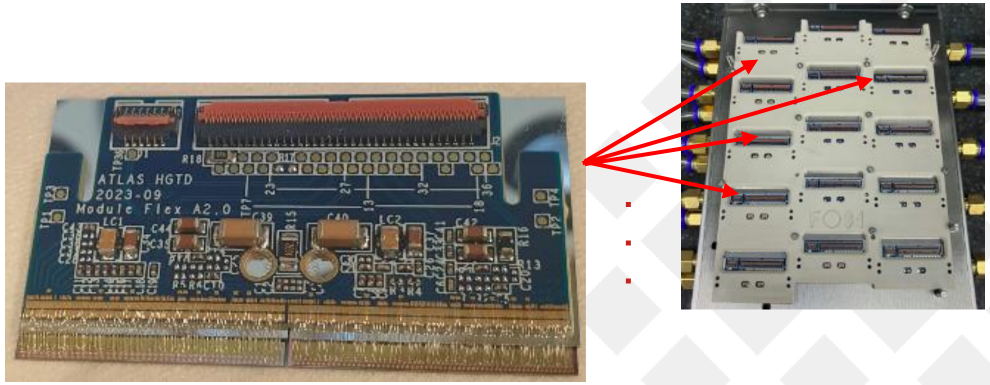
- Almost 200 hybrids produced, more than 50 modules assembled ✓
- Bump bonding at IFAE ongoing
- Pre-production starting, ramping up, expect to do ~100 modules in 2026...

IFAE ID	Sensor 0	Sensor 1	ASIC 0	ASIC 1	Flex	Assembly	Glue [mg]	Full Weight [g]	Total Length [mm]	Sensor Gap [µm]	Initial Bump Conn.	Electrical comm.	WB date	Location	In DB	Comments
A1101	PRE IHEP-IME 42 (thin!)	PRE IHEP-IME 43 (thin!)	AltiA	AltiA	A3.0	feb 2025	Not measured	2.9 g (without WB)	see A1101_Quick_Metrology	Chip gap: 400 um	-	OK	Feb 2025	IFAE	yes	No reflow! Many disconnected bumps! Thin sensors... Also some bad results with this sensor gelpack before...
A1102	USTC pre-prod W16 #3	USTC pre-prod W16 #5	AltiA	AltiA	A3.0	April 2025	17		see A1102_Quick_Metrology	Chip gap: 614 um	-	OK	May 2025	IFAE	yes	OK
A1103	USTC pre-prod W16 #6	USTC pre-prod W16 #7	AltiA	AltiA	A3.0	July 2025	10	3.7958 (WB)		Chip gap: 280 um	-	OK	July 2025	IFAE	yes	OK
A1104	USTC pre-prod W16 #8	USTC pre-prod W16 #9	AltiA	AltiA	A3.0	July 2025	10.7	3.7884 (WB)		Chip gap: 280 um	-	OK	July 2025	IFAE	yes	OK

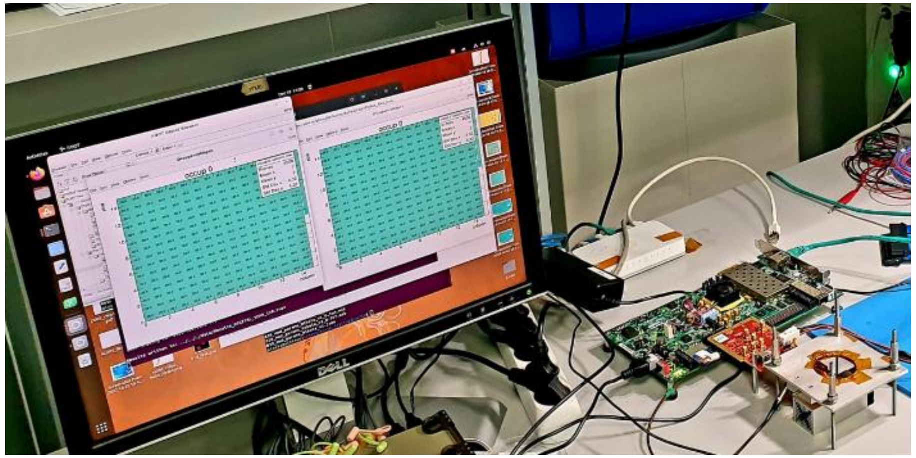


- IFAE commitment: about 1000 modules ie, 2000 **hybrids**
  - ~2 years dedicated to assembly
- Module **assembly**, six module jig operation started… (increase assembly rate)
- Module **loading**: modules have to be loaded into Detector Units...
  - Setup being commissioned

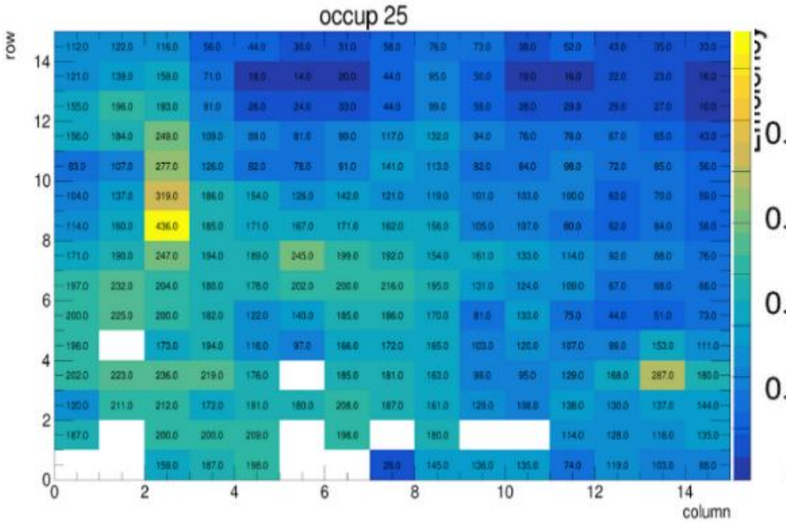
Loading different system than assembly

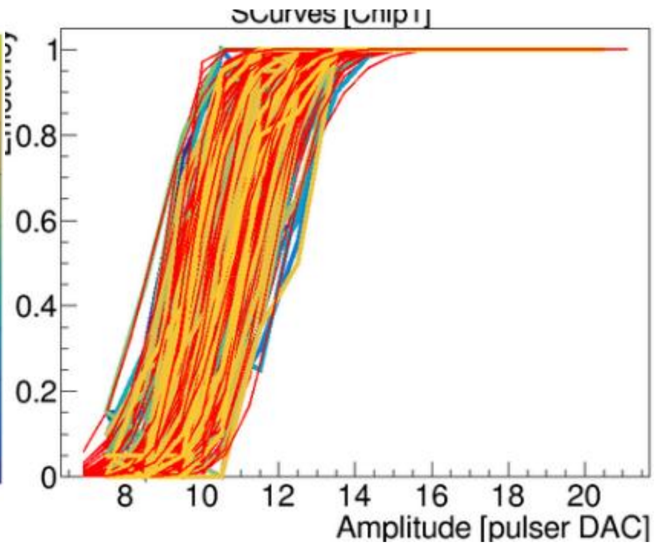


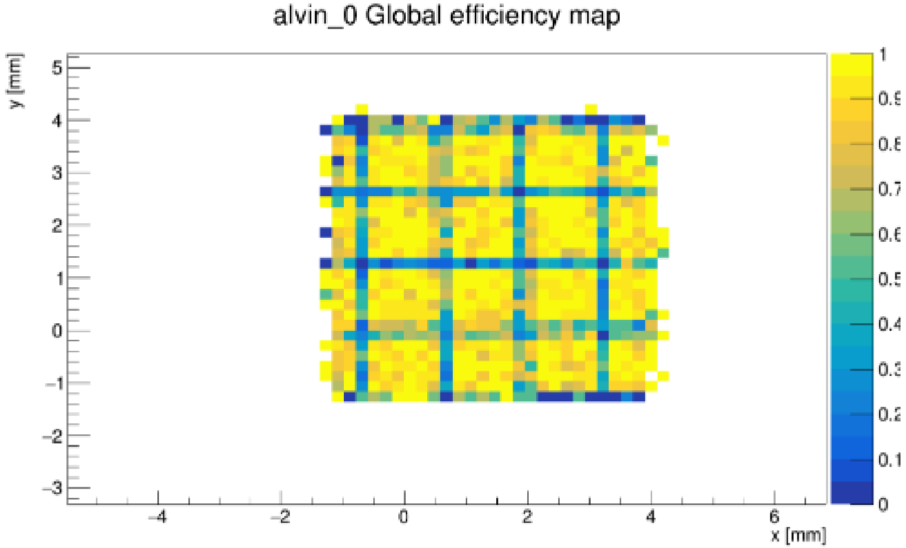
ATLAS HGTD Module Characterization



Alvin DAQ developed by IFAE, used in labs and beam tests







E-L Gkougkousis, https://doi.org/10.1088/1742-6596/2374/1/012175

Conclusions

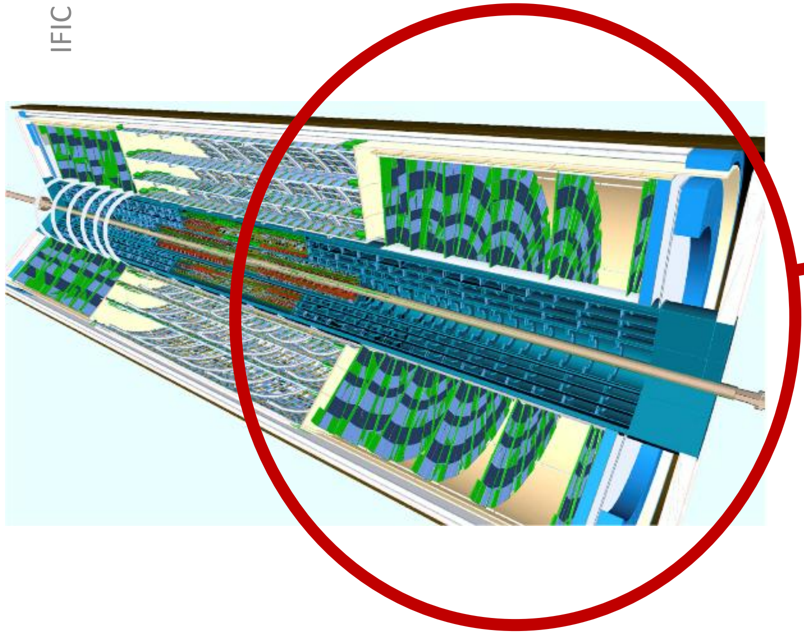
Situation:

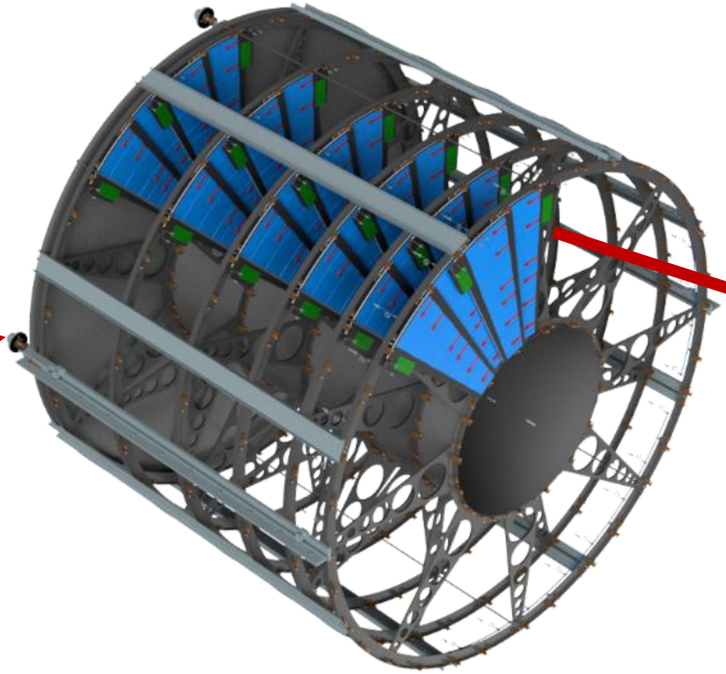
- IFAE's contribution to ITk Pixel and HGTD in the form of modules
- CNM contribution to sensor quality assurance
- ITk Pixel:
  - IFAE responsible for assembly of innermost pixel layer
  - Pre-production completed, about to launch production (waiting for parts)
- HGTD:
  - Prototyping and qualification completed, full detector assembly in-house
  - Pre-production about to be launched

IFIC @ ITk Strips

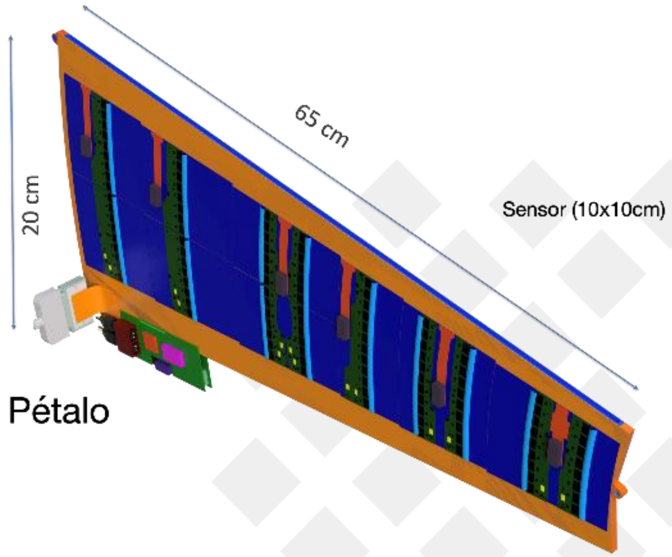
The ITk is the new ATLAS tracker for the HL-LHC.
IFIC-Valencia works in the ITk-Strip endcaps

- Each endcap has 6 disks
- Each disk 32 wedge-shaped carbon fiber supports (petals)
- Each petal houses 18 (9 per side) silicon strip sensors.



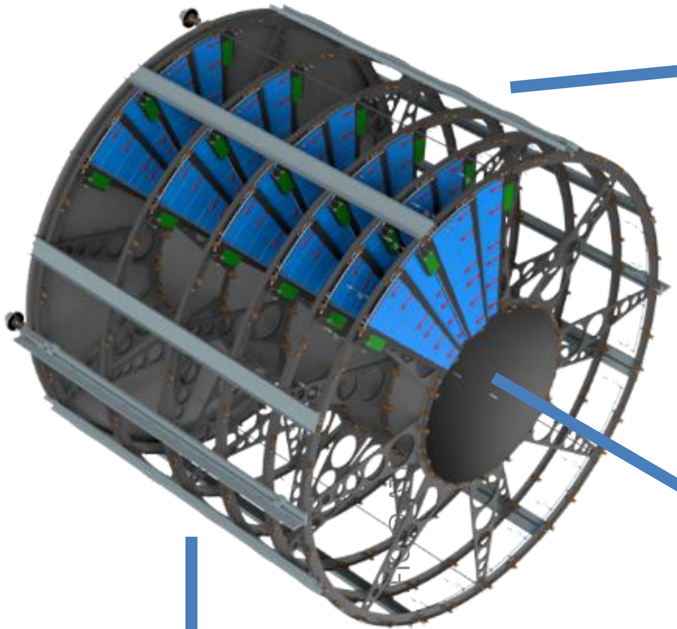


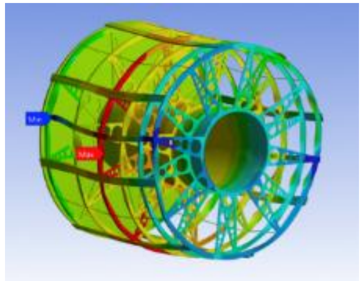
Petal



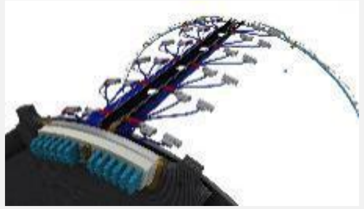
Pétalo

ITk-Strip activities

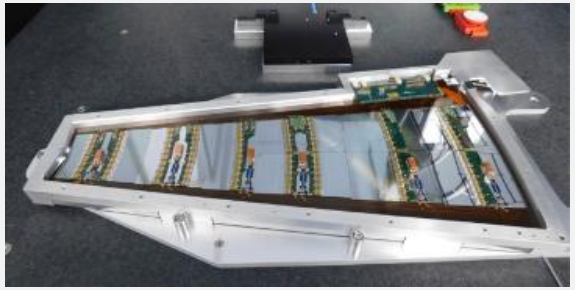




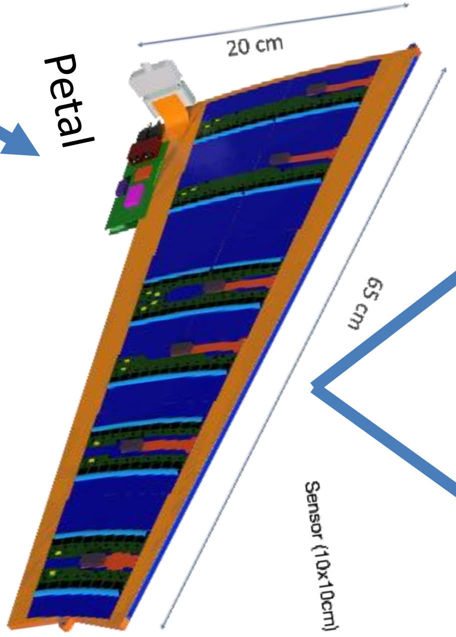
Services



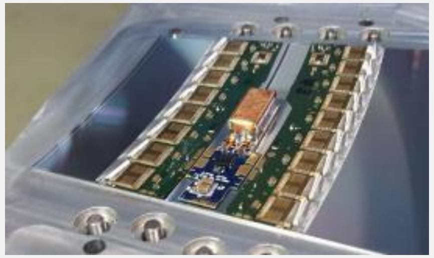
Petal loading



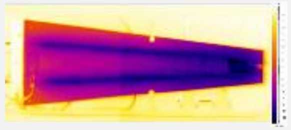
Petal



Modules

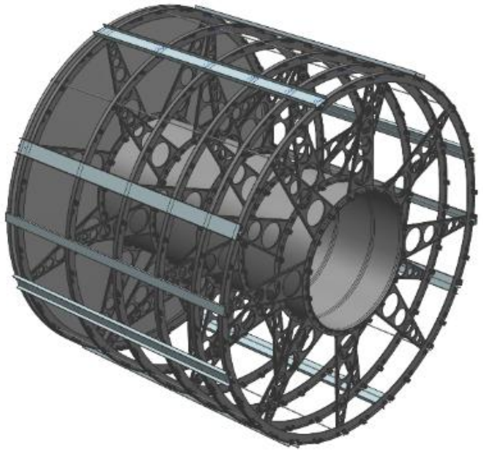


Cores + Bus tapes

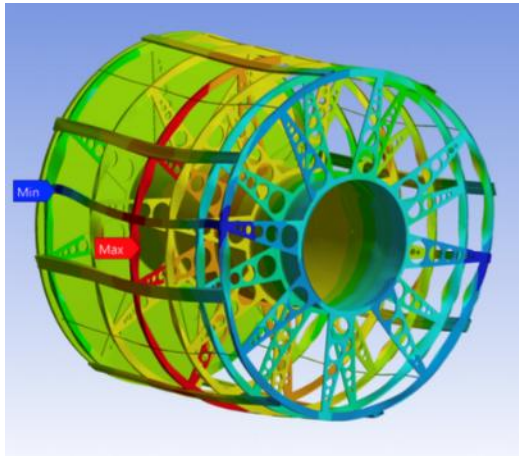


Global Support Structure

Design structure with
NIKHEF & DESY

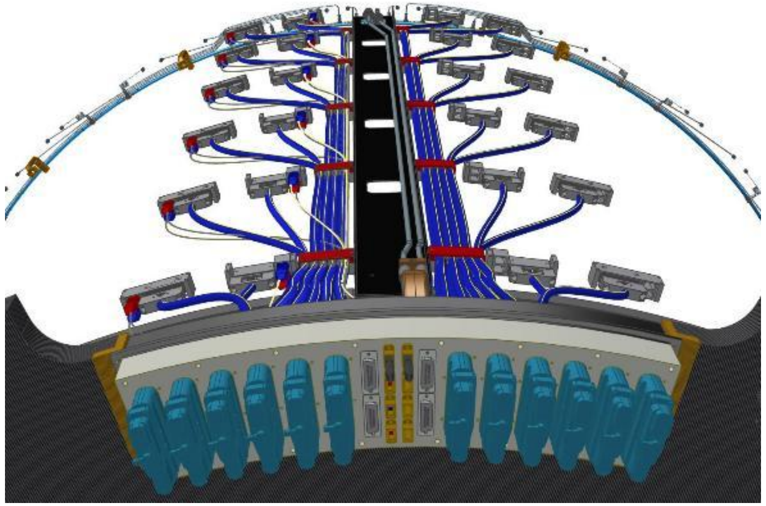


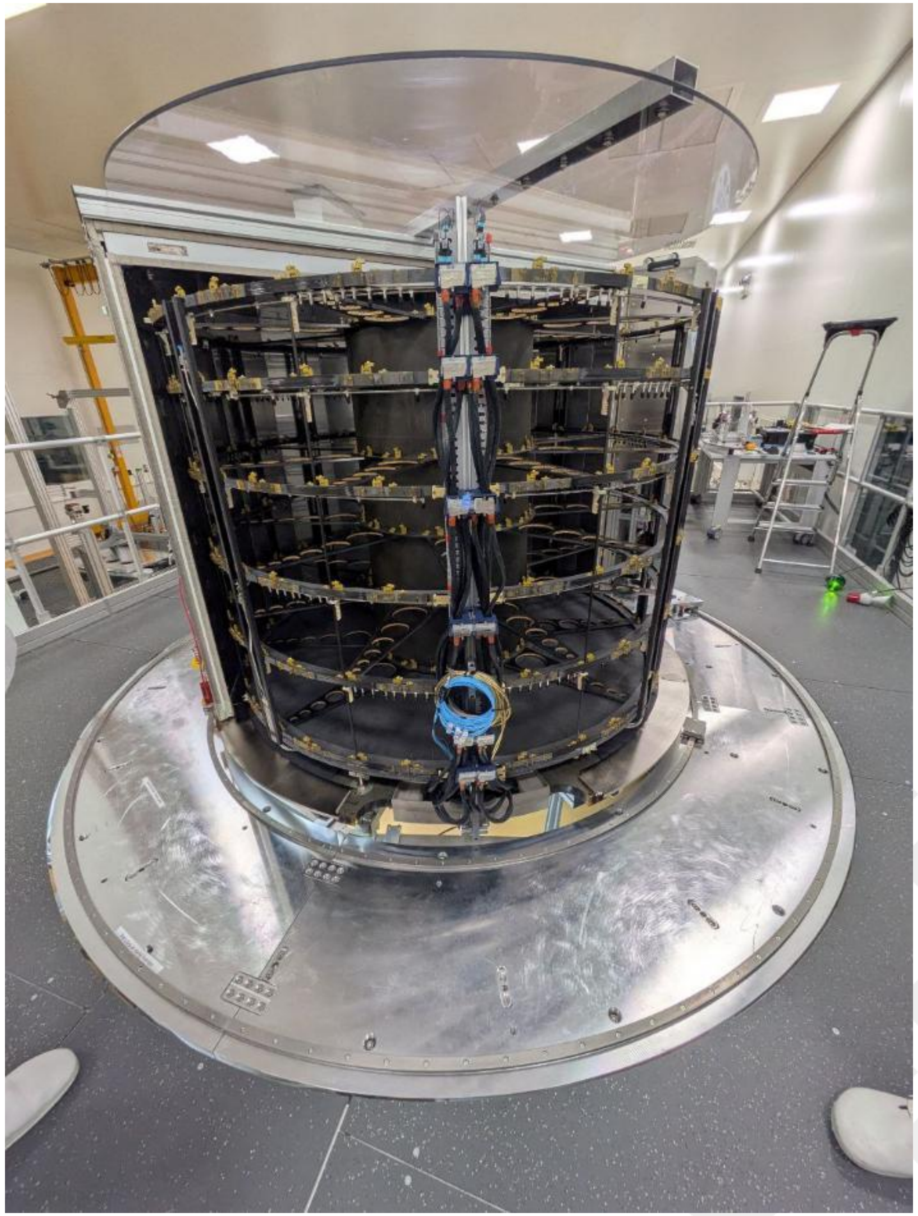
Finite Element Analysis to
optimize the structure

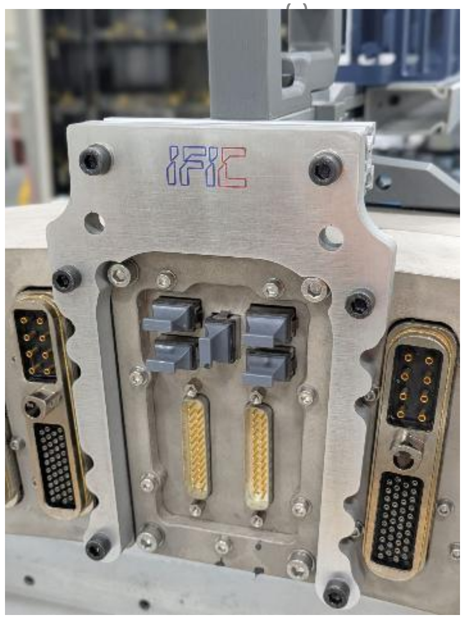


The 2 endcaps already fabricated at at NIKHEF

Services





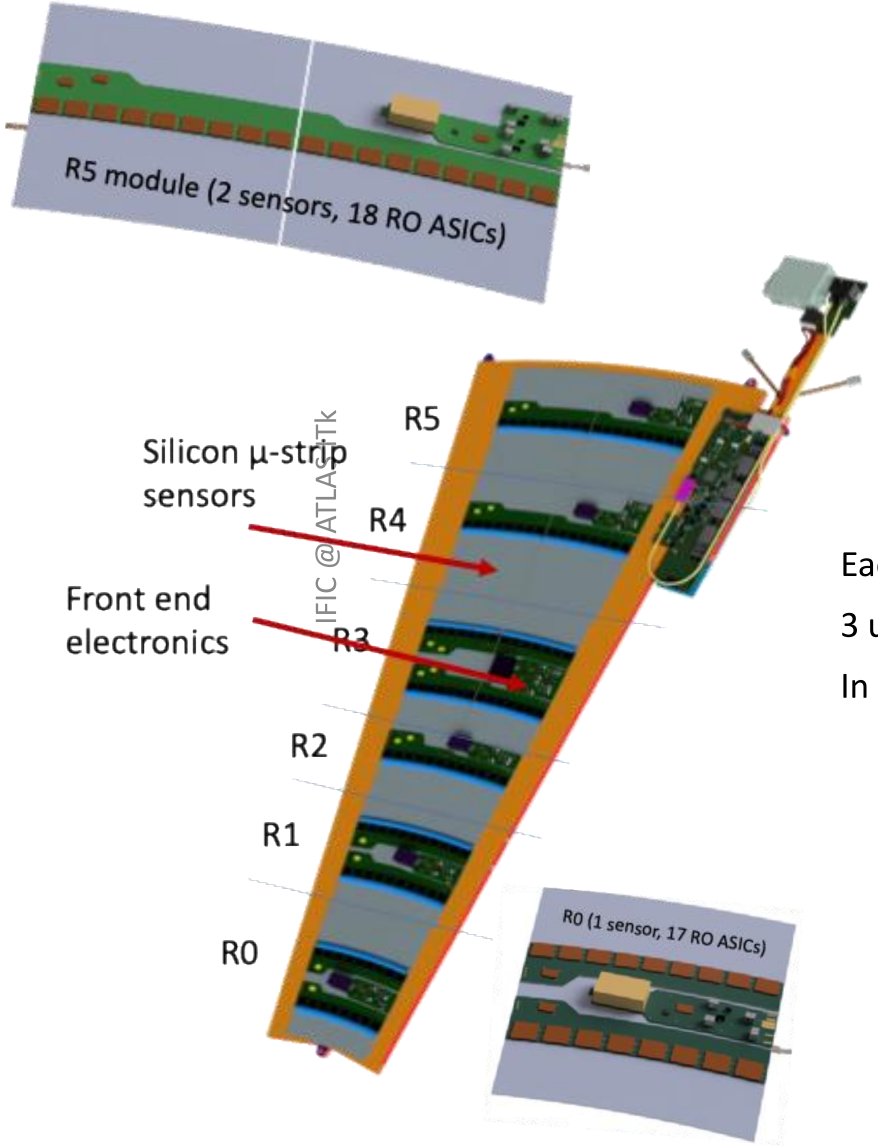


Design of the service module bringing power, control signals and cooling to the petals.

Assemble and install the 16 service modules in the structure

First Service Module already installed in a structure

Petals and Modules



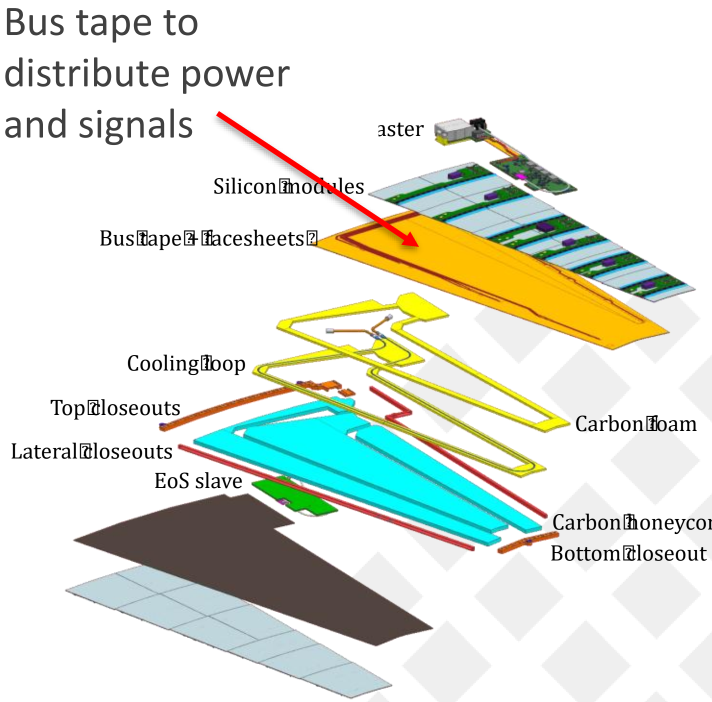
Sensors are glued on local supports (**Petals**). This is the building block of the EC system. It is a carbon fibre sandwich with integrated cooling and electronics.

Double sided object with **18 sensors**, 70cm height, 10-20cm width

Each petal has six rings. One sensor shape per ring.

3 upper radius rings have 2 sensors.

In total, 18 modules, 9 on each side

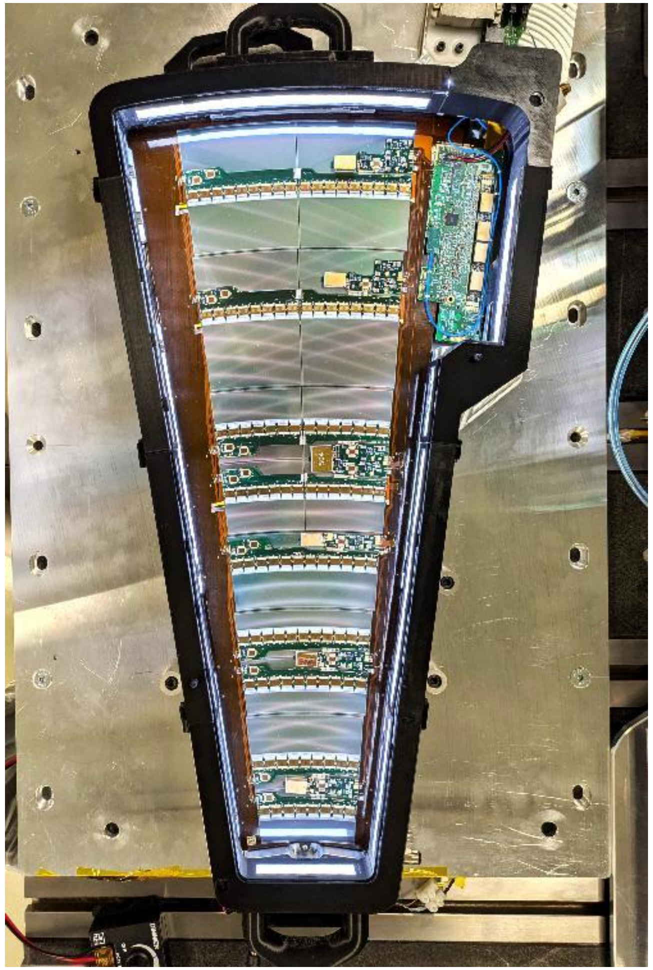


IFIC has to populate 100 of those petals

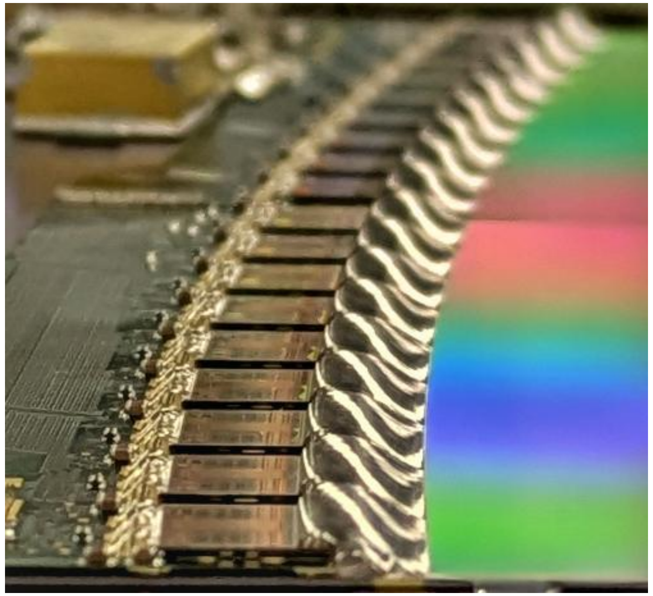
- Will **assemble** all the required R0 (200) and R5 (2x200) modules. In total **600 modules**.
- Will **receive** 200 R1, 200 R2, 2x200 R3 and 2x200 R4. In total **1200 modules.**

Petals and Modules

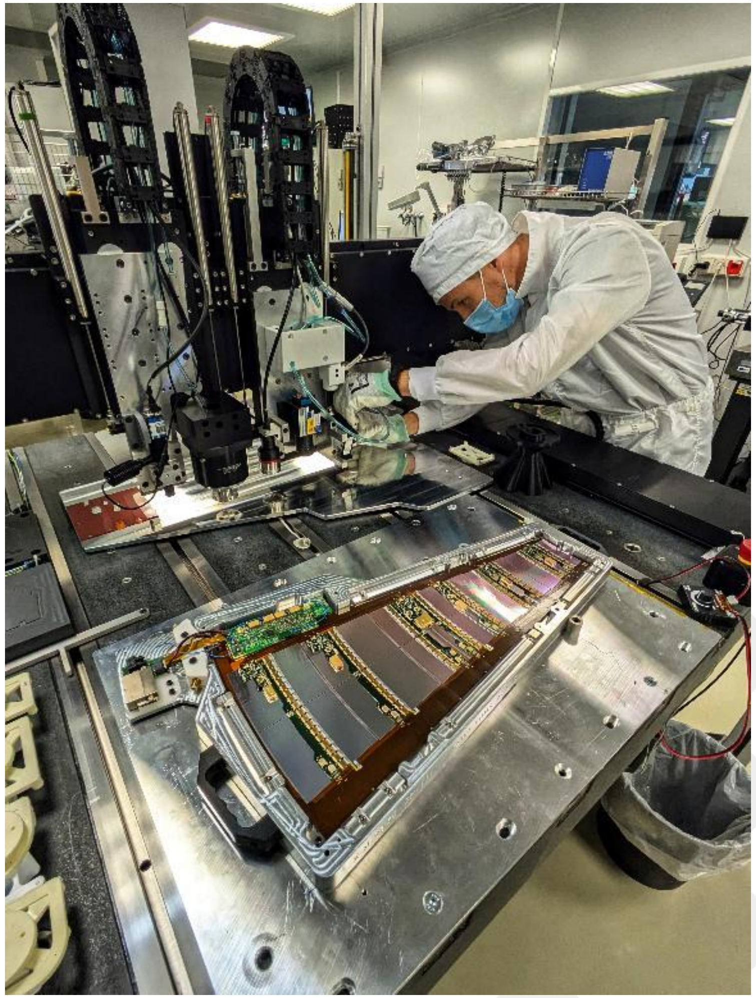
A finished petal



4-row bonding in a module



Loading of a petal in the gantry



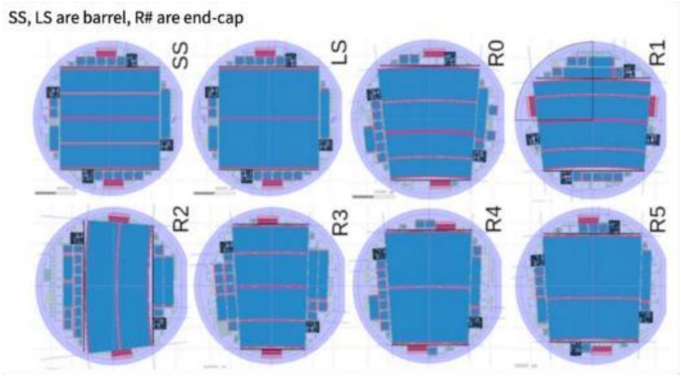
Built so far

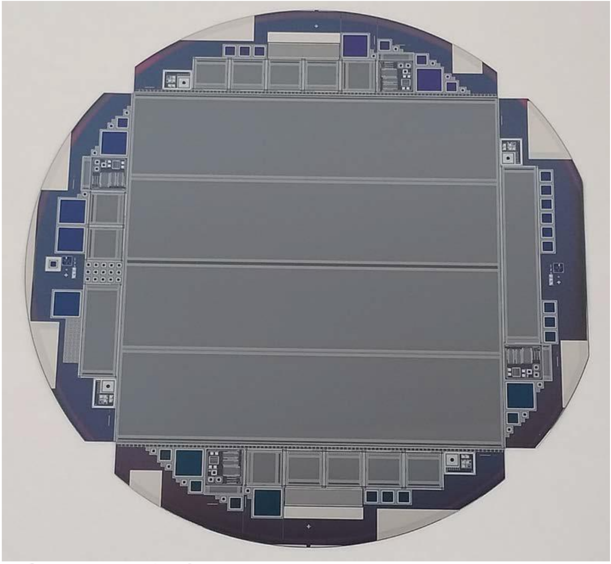
19 R0 modules (97280 bonds)
15 R5 modules (69120 bonds)

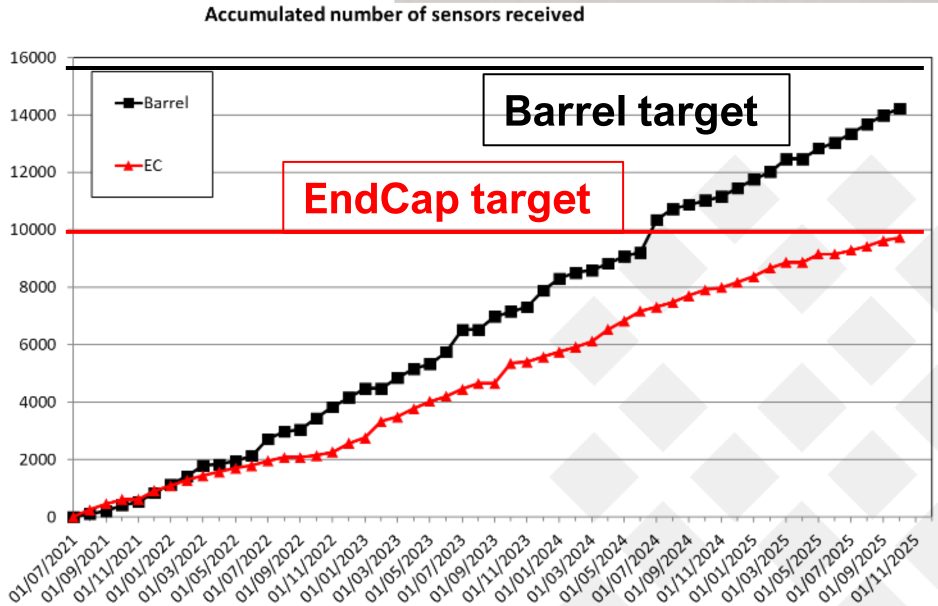
7 petals

Strip sensor R&D and fabrication

- ATLAS-ITK Strip Sensors
  - Strips implanted on p-type silicon bulk (n+-in-p)
  - Single Sided, AC coupled, by Hamamatsu (Japan)
  - Active thickness 300 µm, V_{FD} ~ 280 V
  - 8 sensor geometries, 70 to 80 µm pitch
  - 1 sensor per 6'' wafer + Test Structures
- Coordination of the Sensor Collaboration since 2017
- Quality Control (QC)
  - Checks fulfilment of ATLAS specs with tests on actual main sensors
- Quality Assurance (QA)
  - Monitors the fabrication process to detect deviations and predict tendencies of key parameters. On test structures
  - Tests can be destructive: irradiations
- Status
  - Production is going on at a steady rate (~4.5 years now)
  - About 99% sensors received at this point.
  - 21,553 accepted and ready for modules (89.8%)



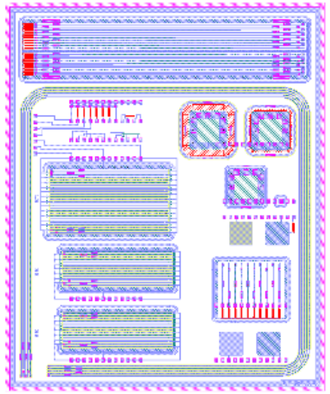




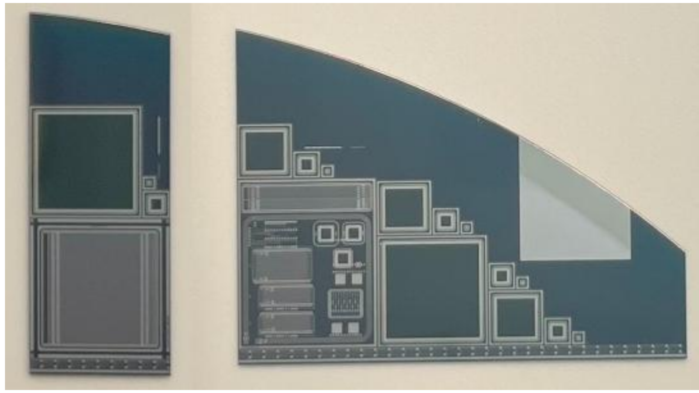
Responsibility in Quality Assurance work for the Collaboration

- Quality Assurance (QA)
  - Preventing defects during production, rather than identifying them after the fact. The QA procedures are applied to both un-irradiated and irradiated test structures
  - Monitor several device and technological parameters throughout production
- 8 test sites around the word
  - Ljubljana, KEK/Tsukuba, Prague, Birmingham, Toronto, Valencia, Barcelona, IHEP
- Test pieces sampled from every production batch
  - Test Chip, Monitor Diodes (MD8), and minis
  - Proton, neutron, and gamma irradiations
  - 2,576 QA pieces distributed for irradiations & tests
    - 596 batches accepted, 6 batches rejected
- Testchip developed at CNM and whole QA plan
  - All pre-irrad tests of QA samples done at CNM
  - Parameter extraction, analysis and DB upload software developed at CNM

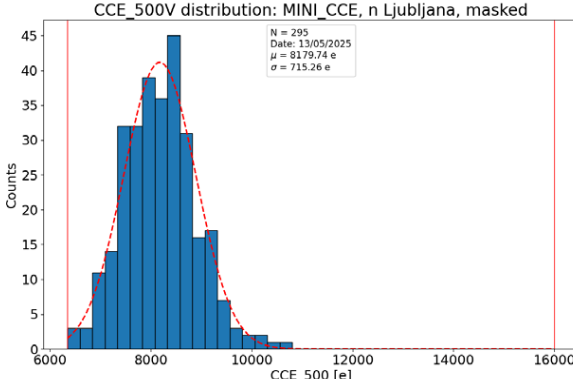
Test chip



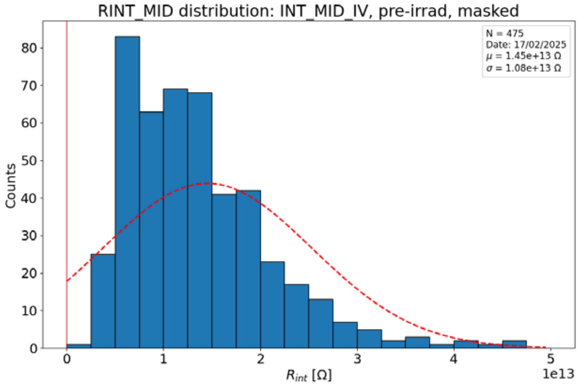
QA Test pieces



Example results



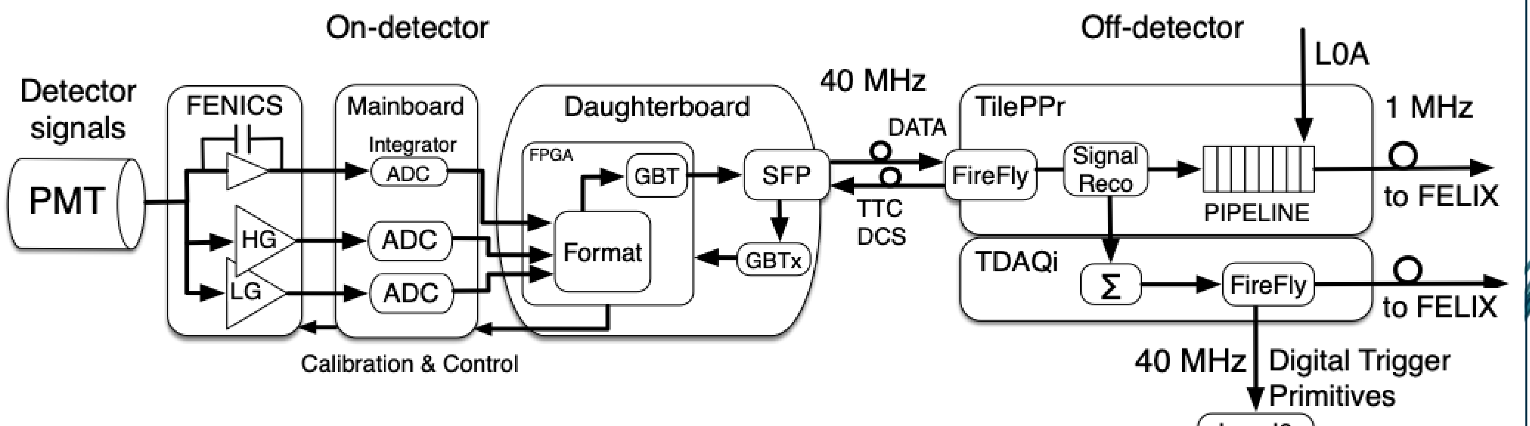
Post-neutron CCE



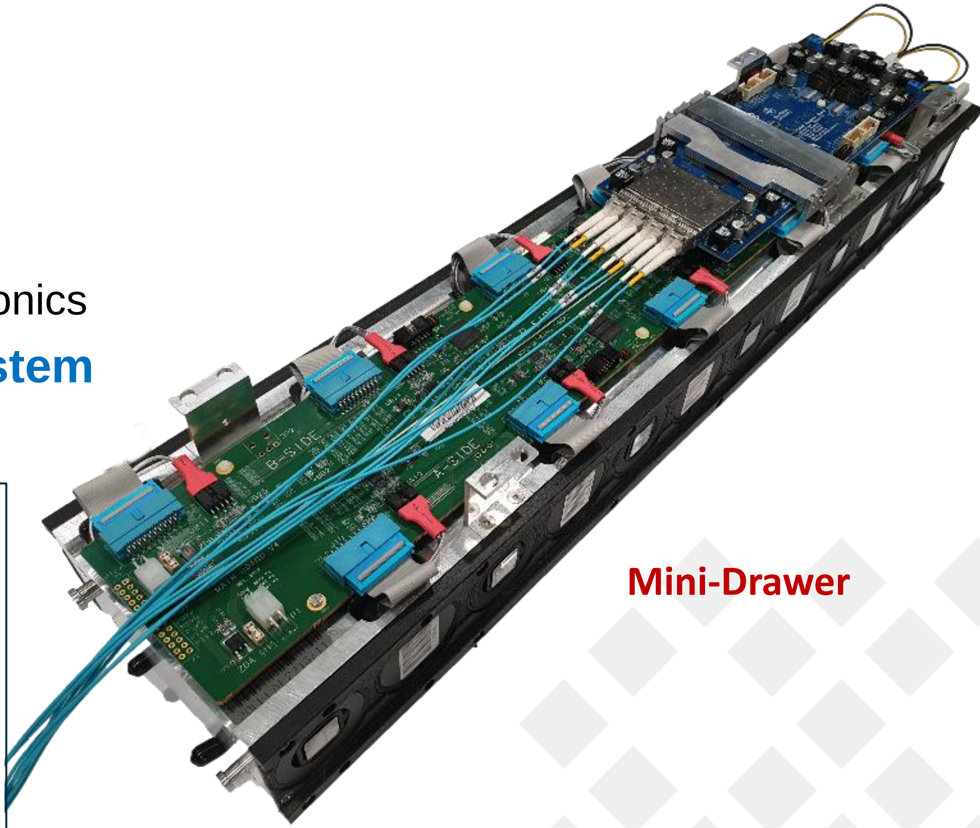
Pre-irrad interstrip resistance

Readout electronics

- On-detector electronics transmits **full digital data** for every bunch crossing (40 MHz)
  - 6,000 optical fibers (aggregated ~ 40 Tbps)
- Off-detector **PreProcessor**
  - Real time **signal reconstruction** to obtain cell energy depositions
  - Provides digital **trigger primitives** to Level 0 Trigger Systems
  - **Readout** events after L0 Acceptance
  - **LHC clock and control commands** transmitted to on-detector electronics
- Redundancy in data links and power distribution for **improved system reliability**



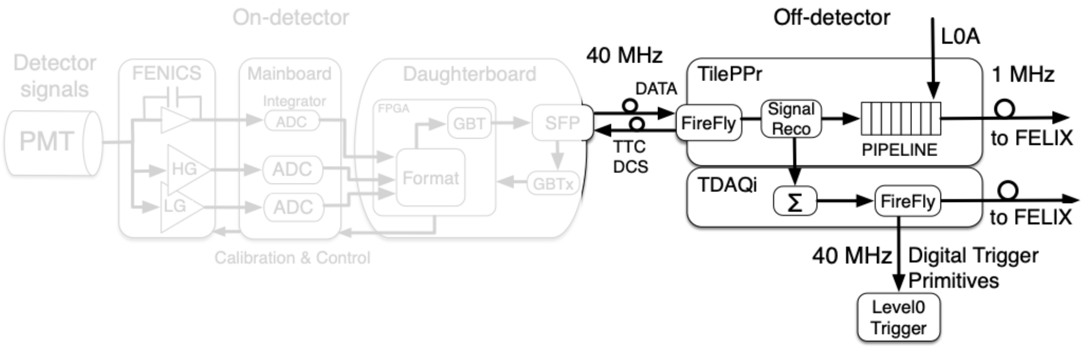
Upgrade of ATLAS Tile Hadronic Calorimeter for HL-LHC -

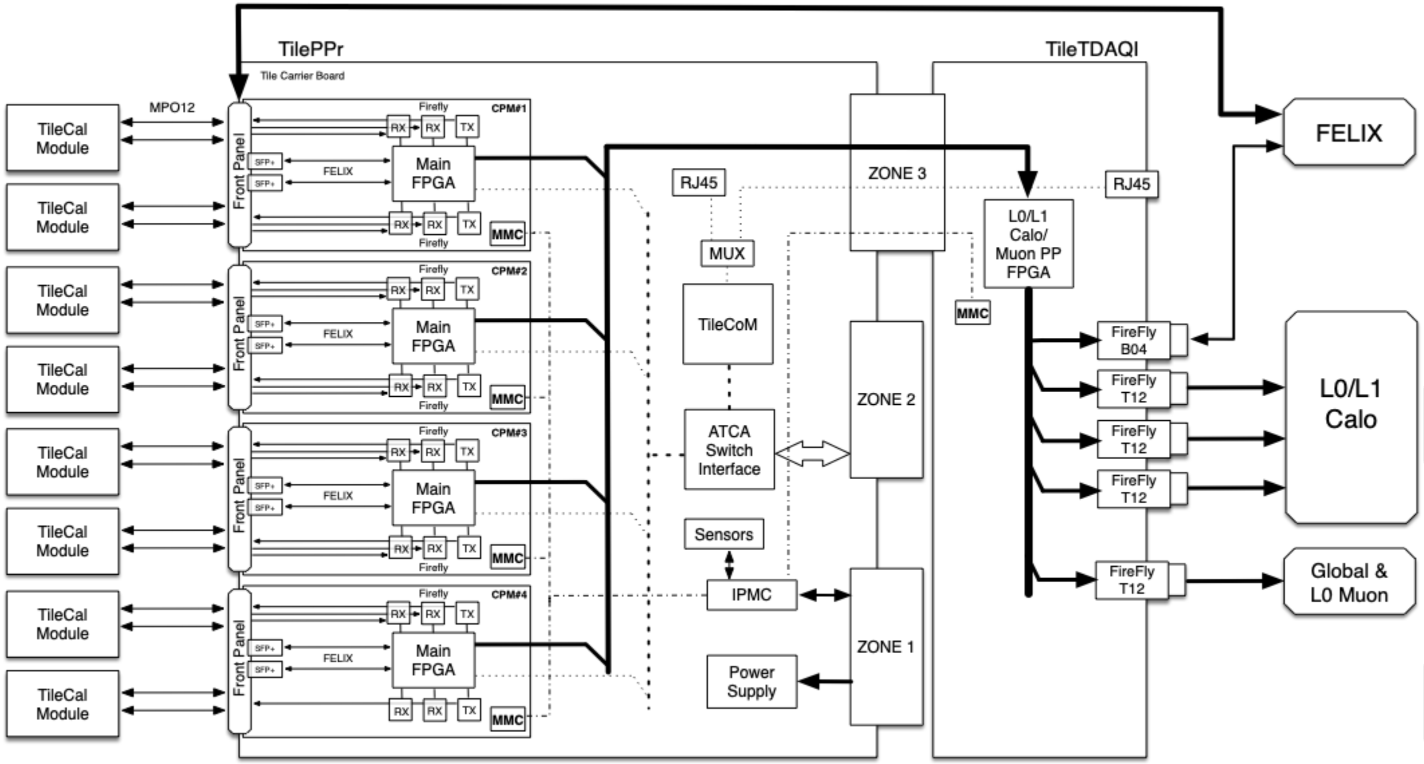


Mini-Drawer

Off-Detector Electronics

- PreProcessor (PPr) : **interface** between the on-detector electronics and the ATLAS Global DCS, DAQ & Trigger systems
- **Signal reconstruction** (trigger and DAQ), **clock distribution**, **DCS interface**, **front-end control**
- Modular design
  - ATCA Carrier
    - TileCoM : System-on-Chip
    - IPMC: Health monitoring
    - GbE Switch : 16x1Gbe ports
  - Compact Processing Module(CPM): data processing
  - Trigger & DAQinterface(TDAQi) : trigger interface
- Final designs approved
  - Now PreProduction





Upgrade of ATLAS Tile Hadronic Calorimeter for HL-LHC

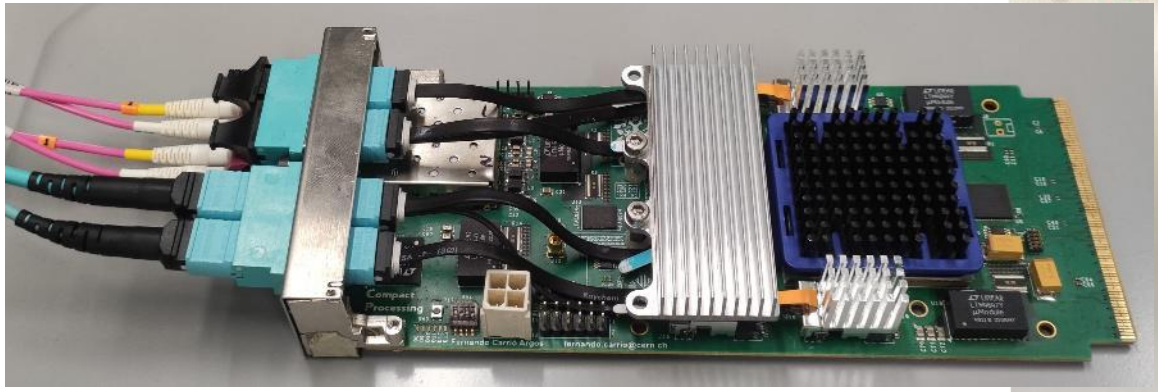
Off-Detector Electronics

Centro Nacional de Microelectrónica IMB

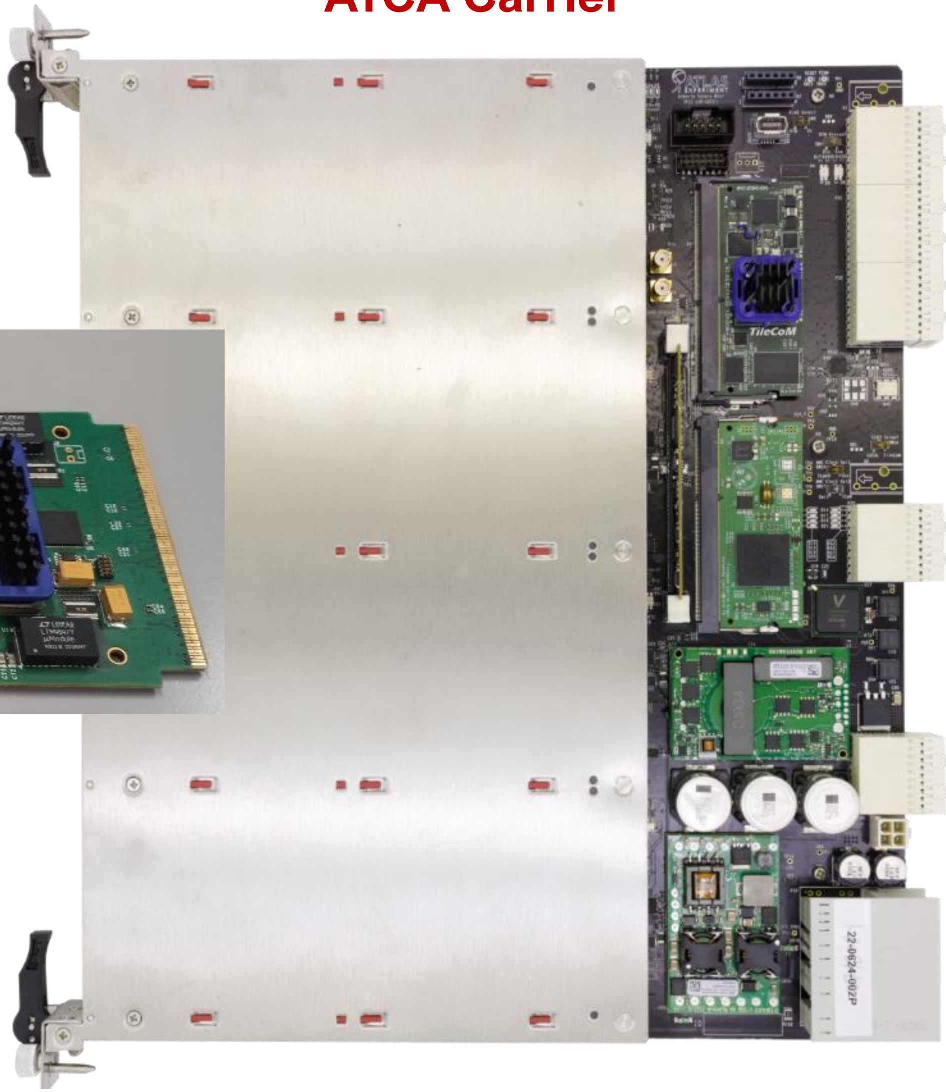
CSIC Consejo Superior de Investigaciones Científicas

INSTITUT DE FÍSICA CORPUSCULAR

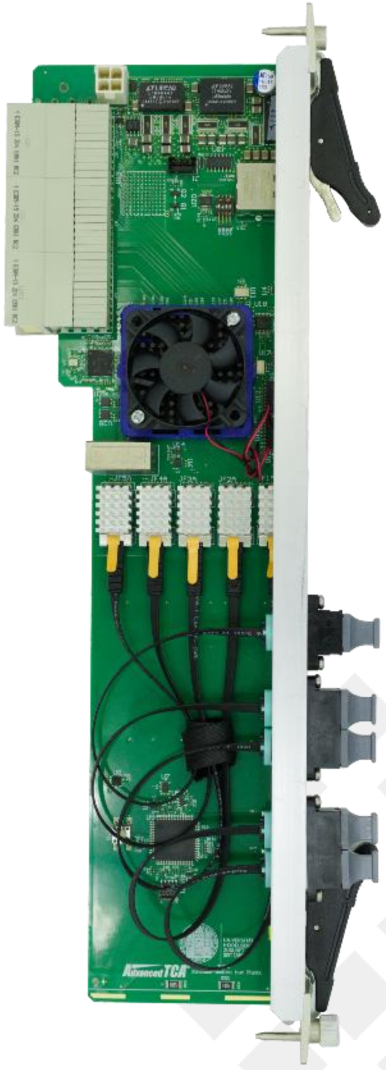
CPM



ATCA Carrier



TDAQi



Upgrade of ATLAS Tile Hadronic Calorimeter for HL-LHC

LHCb

- ECAL
- VELO
- SciFi/Tk

UPC

UNIVERSIDADE DA CORUÑA

IGFAE

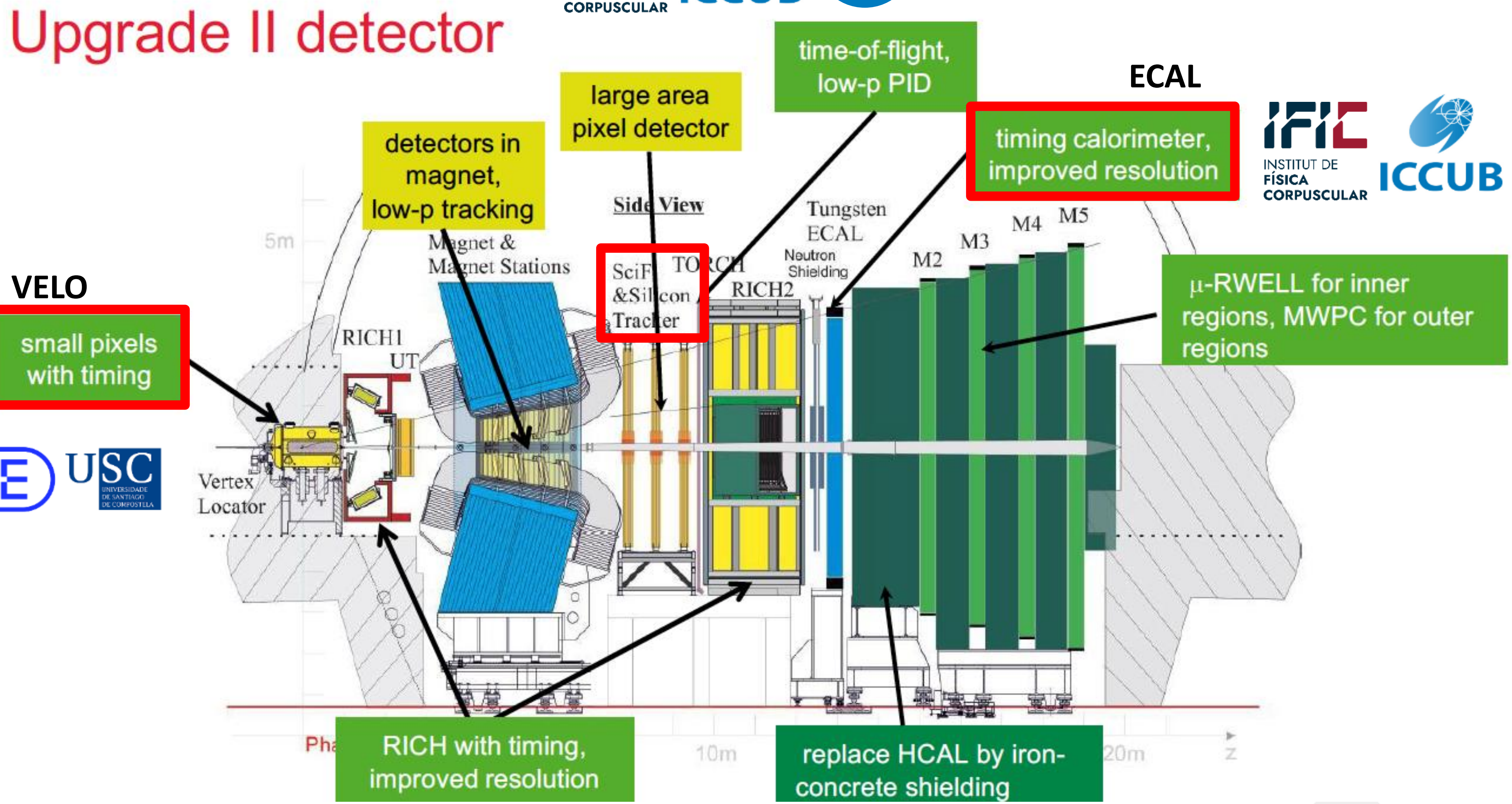
USC UNIVERSIDADE DE SANTIAGO DE COMPOSTELA

ICCUB

IFIC INSTITUT DE FÍSICA CORPUSCULAR

laSalle UNIVERSIDAD RAMON LLULL

LHCb Upgrade II

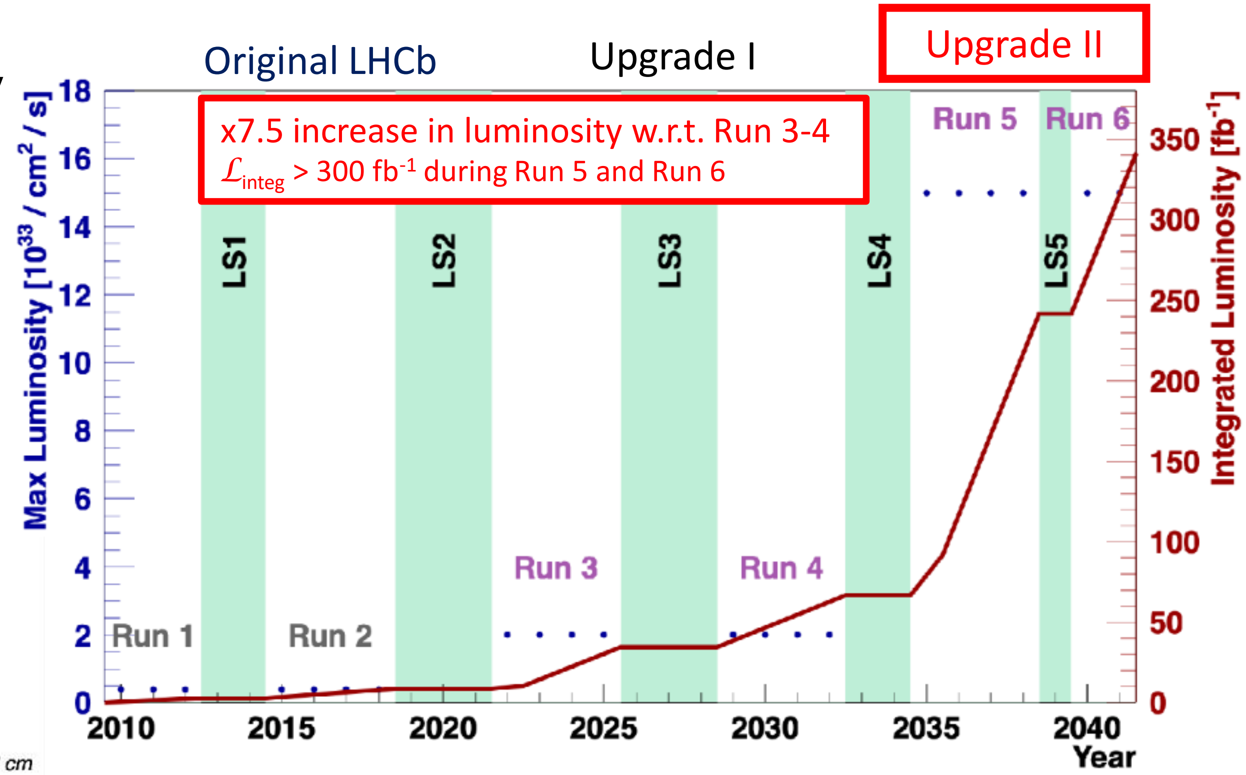


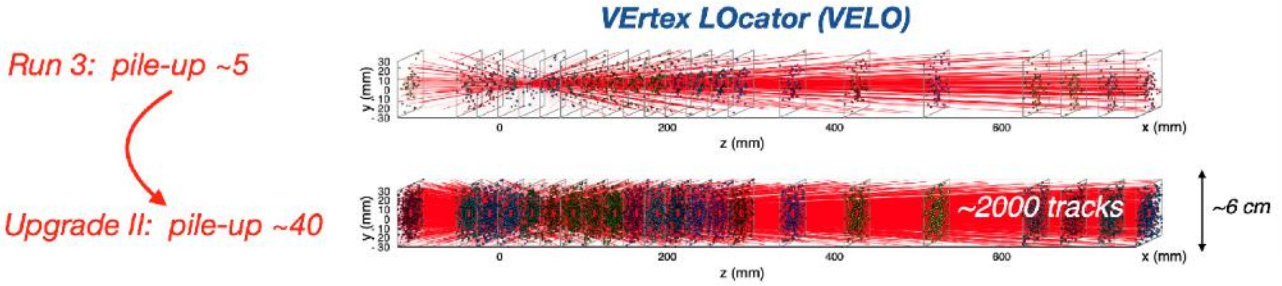
Motivation

Upgrade I will not saturate precision in many key observables: a further upgrade is necessary to fully realise the flavour-physics potential of the HL-LHC.

The performance of **Upgrade II** must equal or surpass that of **Upgrade I**, with:

- Pile-up reaching values of 40
- 200 Tb/s of data
- Charged particle densities up to 1×10^{12} / cm^2

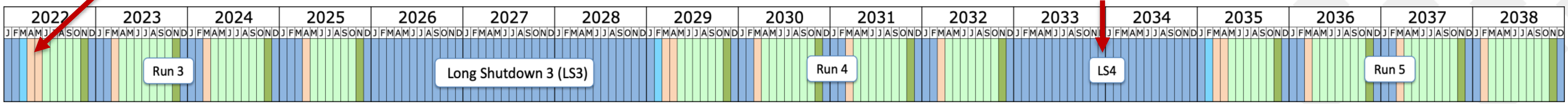




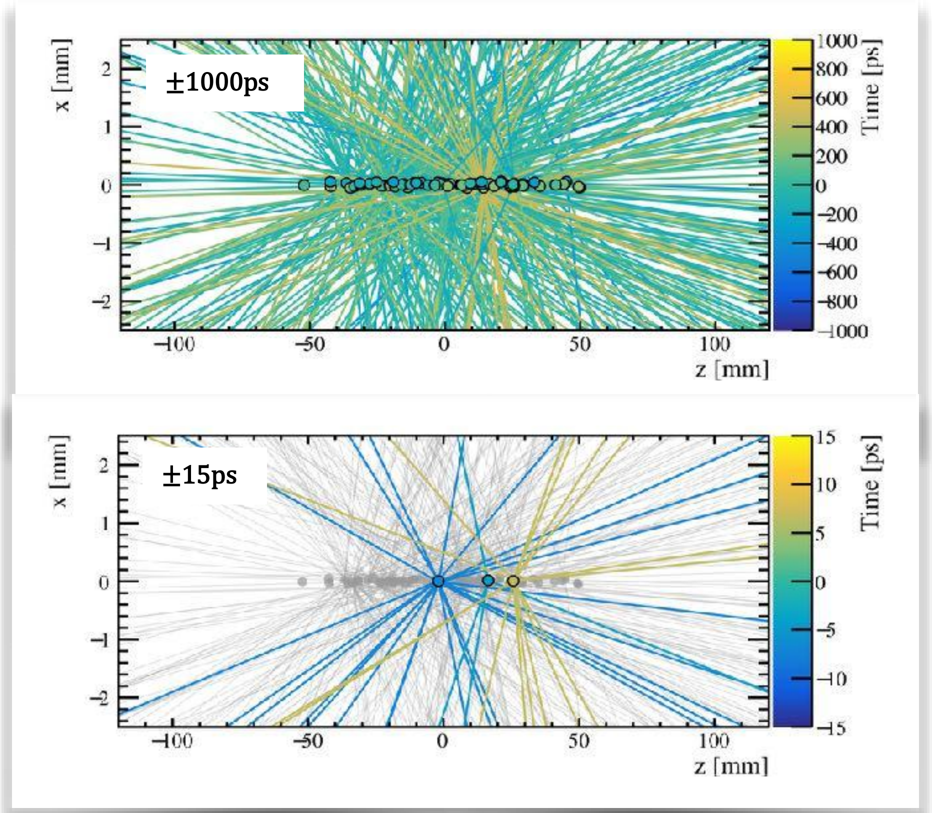
This is the **intensity frontier!** New, lightweight technologies with **high granularity**, **fast-timing**, **radiation hardness** and innovative data processing all necessary to go to $\mathcal{L}_{peak} \sim 1 \times 10^{34}\ cm^{-2}s^{-1}$

Upgrade I installation finished

Ramping up developments for Upgrade II to be installed in **LS4** (~2033)

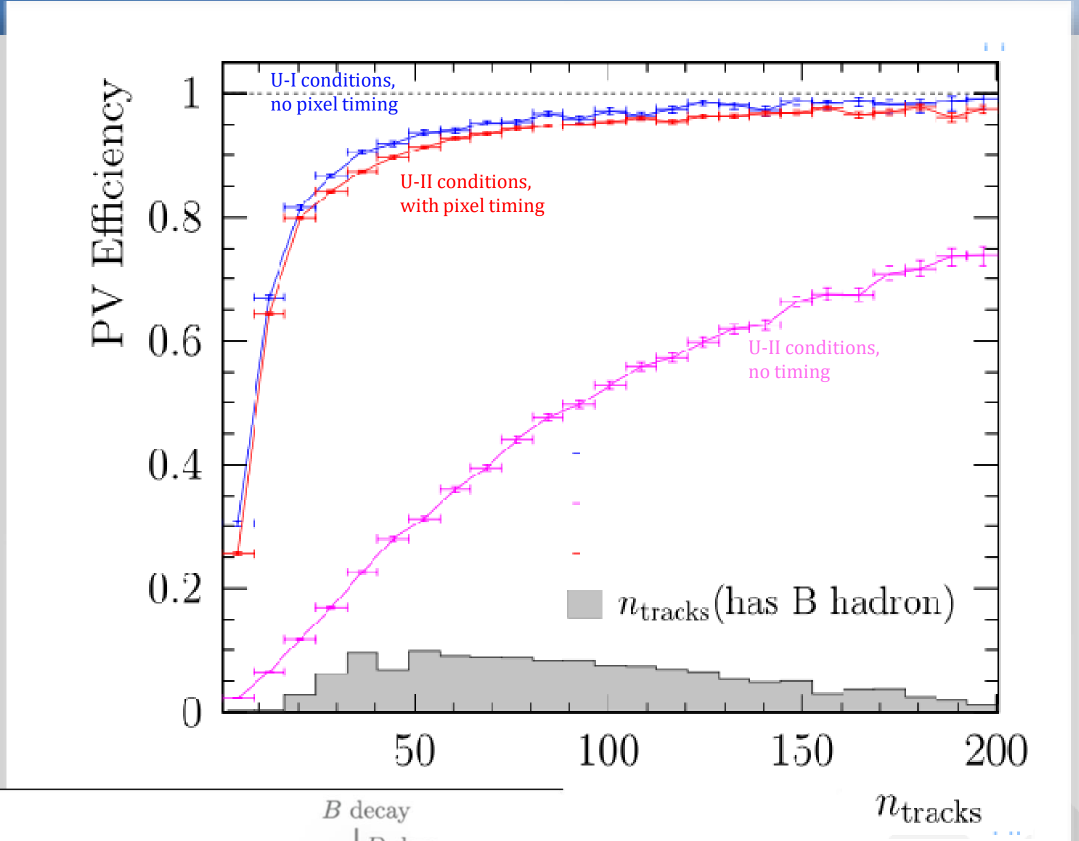


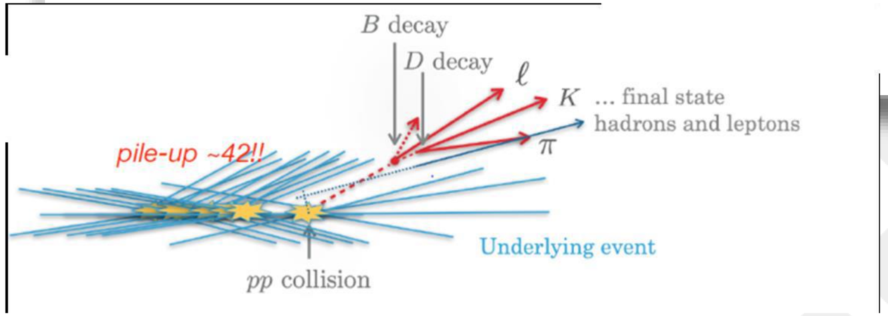
VELO II: the importance of timing



Higher pile-up → PV separation from Upgrade I (4.2 mm) reduced to **1.5 mm** in **Upgrade II** along the beam line.

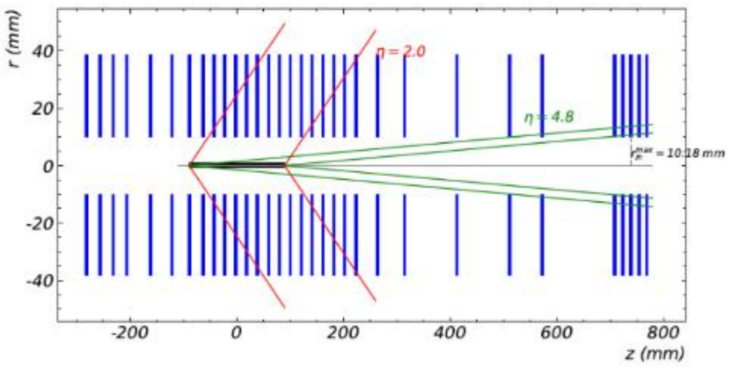
- Proton bunches overlap for a finite time (RMS ~ **180 ps**): in 1 ns window many overlapping collisions
- Increasing the resolution to **20 ps** only a few collisions and corresponding tracks remain

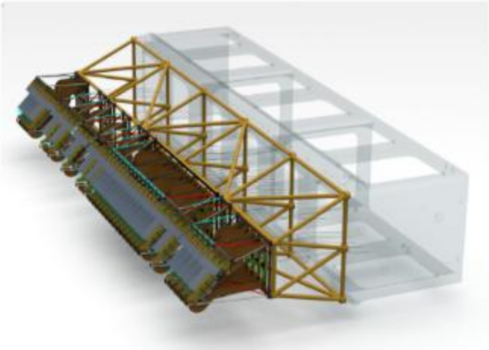




PV efficiency and IP resolutions will yield ~same signal selection performance IF timing resolution of 20 ps/track is achieved.

Upgrade II VELO layout scenarios



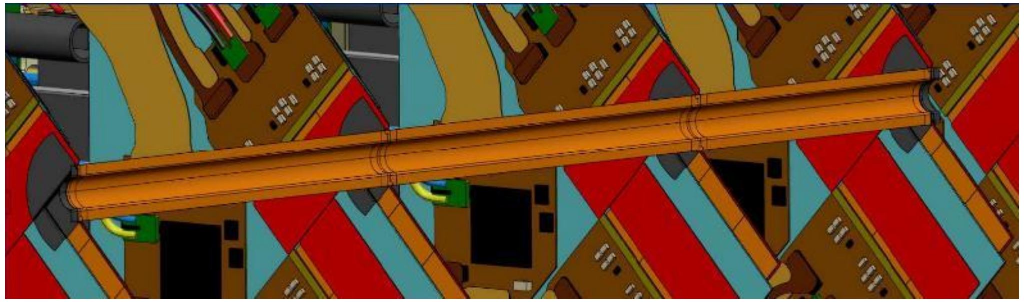


(Left) VELO detector layout in the Baseline scenario. (Right) Illustration of the VELO stations in one half of the detector, in the Baseline scenario

Baseline	Middle	Low
$1.5 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$	$1.0 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$	$1.0 \times 10^{34}\,\mathrm{cm^{-2}\,s^{-1}}$
	VELO	
32 stations, $\eta < 4.8$	32 stations, $\eta < 4.8$	28 stations, $\eta < 4.7$
module 0.8% X_0	module 0.8% X_0	module 1.6% X_0
RF foil 75 µm	RF foil 75 µm	RF foil 150 µm

Baseline:

- **Tracking Efficiency:** >99% within LHCb Upgrade II acceptance (hits in at least 5 detector planes).
- **Sensor Technology**: 3D silicon (150 µm thickness, 50 µm pitch) high spatial and temporal precision for the detector lifetime (> 300 fb^{-1})
- **Spatial Resolution:** < 10 µm single-hit
- **Timing**: 50 ps per hit
- **Sensor Inner radius:** 7,2 mm from the beamline to the closest detector element.



Conceptual design for a lightweight cylindrical RF-shield between the LHC beamline and the Upgrade II VELO modules

Scenarios @ reduced cost: **Middle and Low**

- Reduction in Peak Luminosity 1.5 → 1.0 → reduction of data rates
- Further reduction (Low): Thicker RF foil (a la UI) and 3D-printed metal alloy cooling interfaces instead of silicon microchannels → higher material budget and degradation of IP resolution → reduction in performance**.**

Upgrade II VELO ASICs

Sensor R&D is closely matched to the ASIC development

Upgrade I based on **VeloPix** ASIC (130nm, from Medipix family). A new generation chip - Timepix4 has timing capability

Upgrade II requirements much more demanding still but could draw on similar concepts: **LA-PicoPix**, **IGNITE** demonstrator chips optimised for 3Ds sensors

	VeloPix 1	LA-PicoPix	IGNITE
Technology	130 nm	28nm	28nm
Pixel size	55 x 55 um	50 x 50 um	45 x 45 um
Pixel arrangement	256 x 256	386 x 256 (not decided yet)	320 x 256 (not decided yet)
Time resolution	25 ns	~30ps	~16ps
Readout bandwidth	20 Gbps	100 Gbps	100 Gbps
Ratiation hardness	400MRad	1 GRad	1 GRad

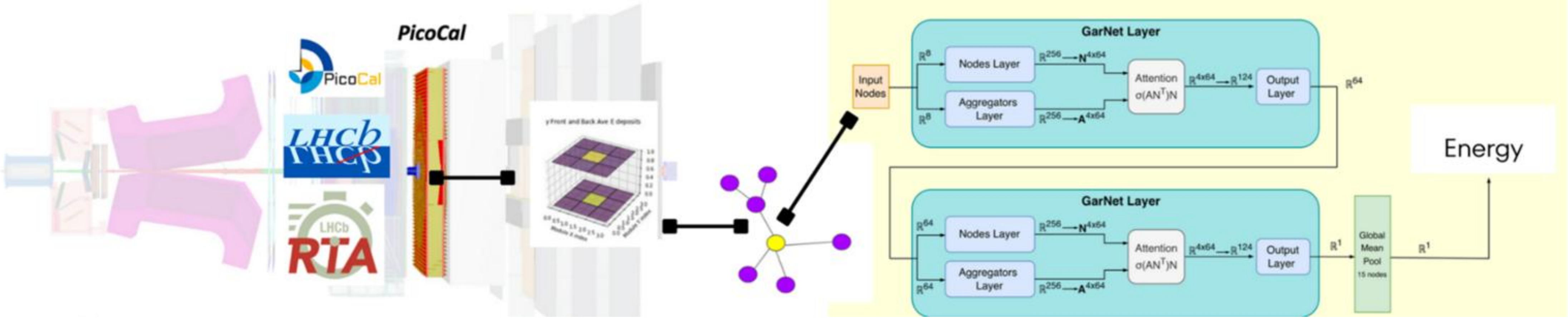
ASIC requirements	
Pixel pitch [μm]	≤ 48
Loss of hits [%]	≤ 1
Lifetime TID [MGy]	> 12
ToT resolution/range [bits]	6
Power budget [W/cm^2]	2
Power per pixel [μW]	23
Threshold level [e^-]	≤ 500
Pixel rate hottest pixel [kHz]	> 180
Max discharge time [ns]	< 29
Bandwidth per ASIC of 2 cm^2 [Gbit/s]	> 250

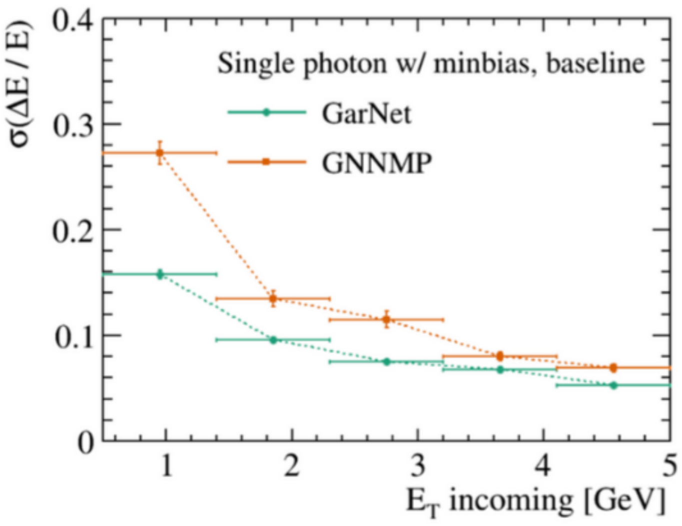
Smaller pitch at larger r to maintain U-I resolution

Dose Achievable with 28nm TSMC CMOS

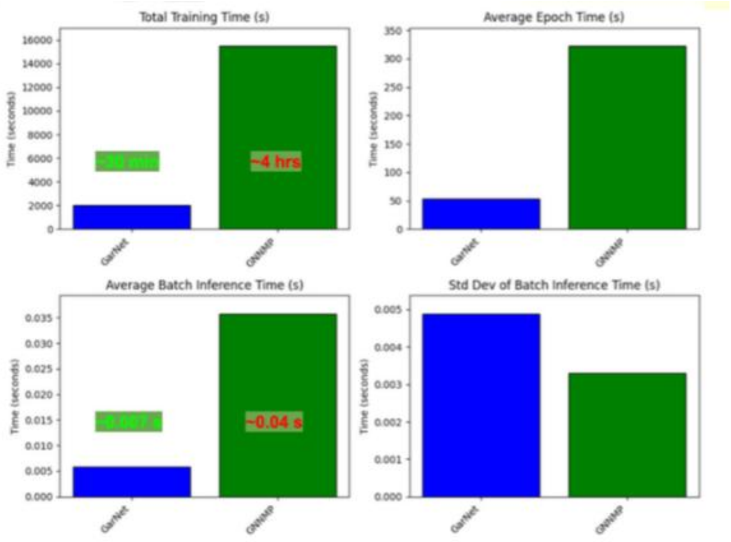
Innermost r: ~64 tracks per bx & 3.8 Ghits/s requires large b.w. Implementing data reduction on ASIC

Towards a lightweight graph neural network for LHCb's next-generation calorimeter





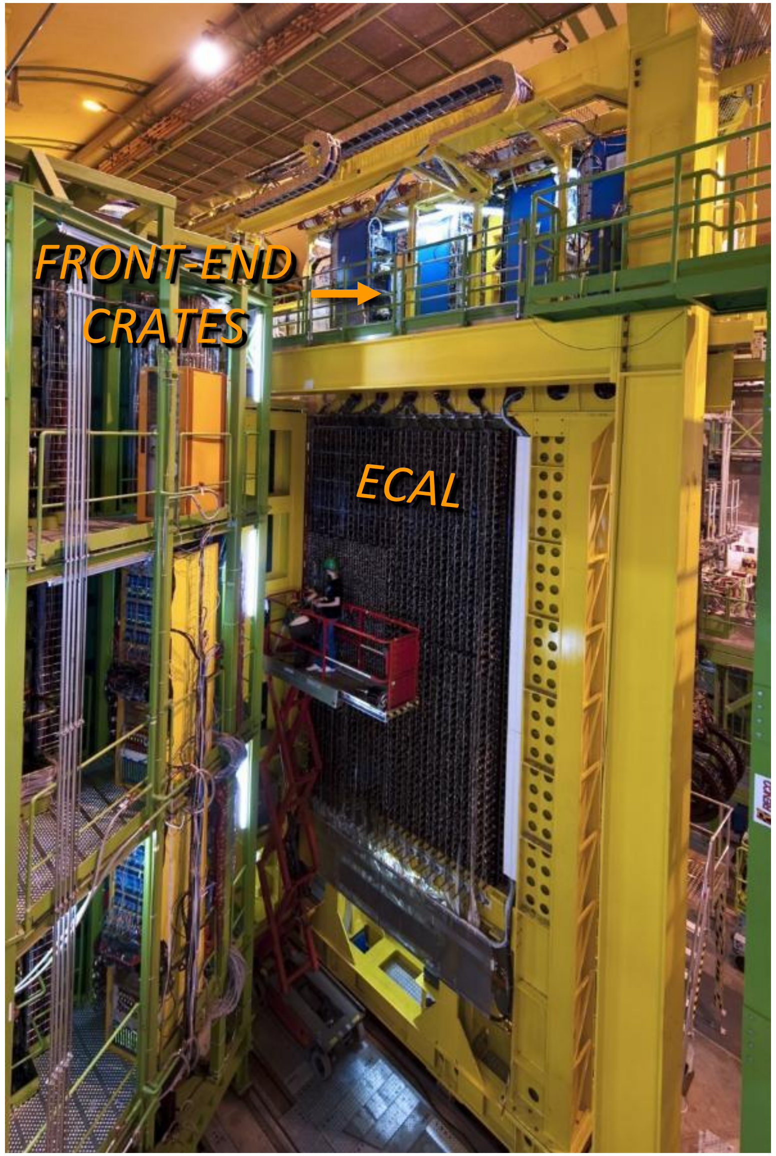
Superior Energy resolution

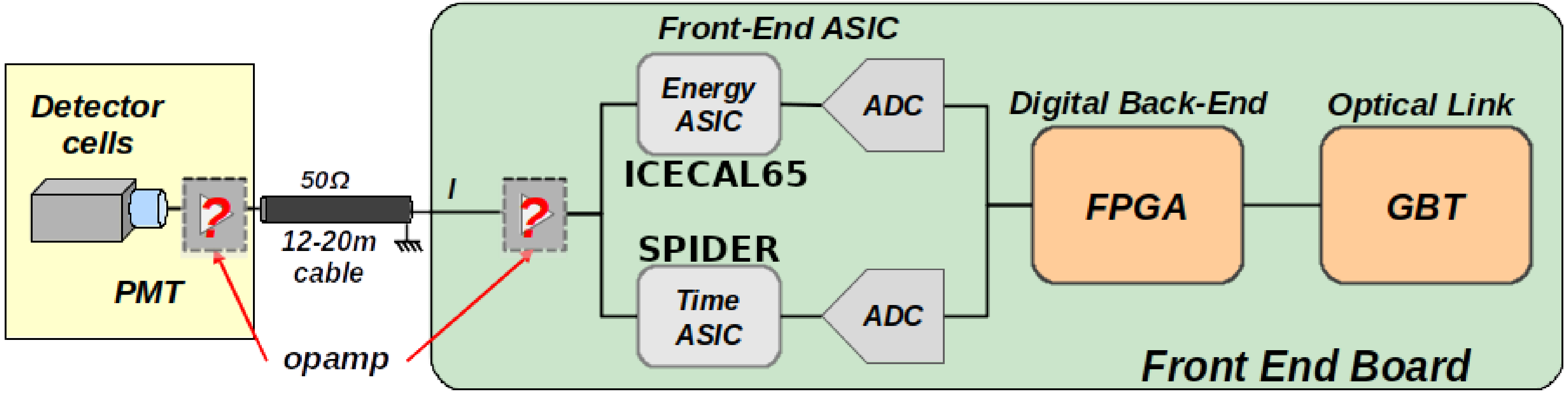


~8x speedup

- Creating a path towards HLT1 reco
- ONNX format and Distilled versions actively being explored with even more promising initial results
- To be tested with the Allen framework with PicoCal

PicoCal readout electronics

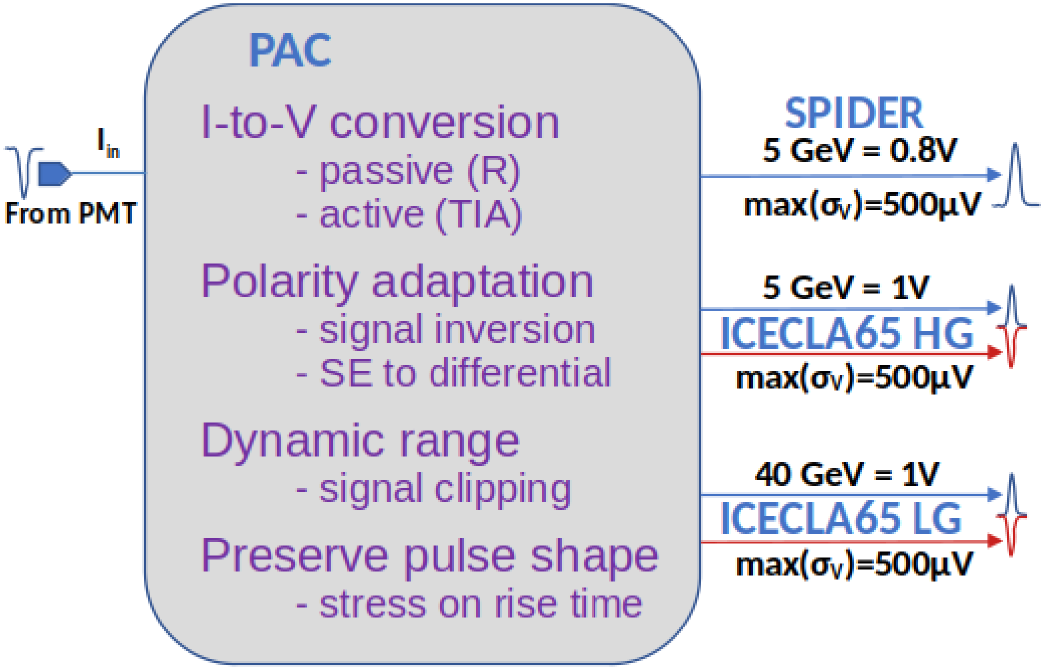


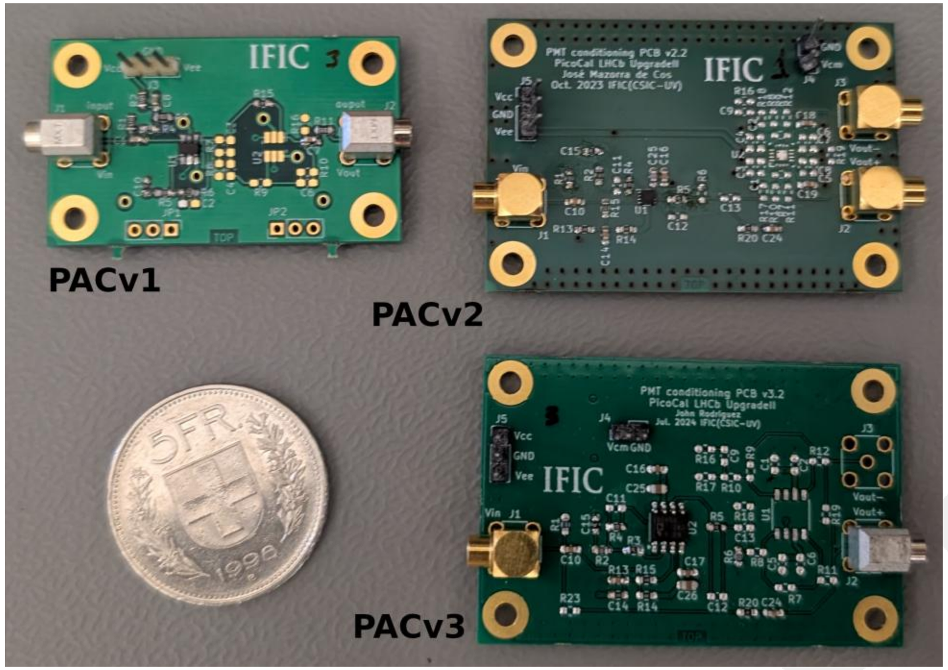


- Photodetectors readout solution follows the same scheme as in current ECAL
  - Minimal light transport with PMT sensors near modules
  - Electronics in crates on top of the detector (reduced radiation)
  - Connection via analog link (coaxial 50Ω) up to 20m between modules and FEE (IFIC)
- Aims at energy (12bit,ET≈40GeV) and time (σt≈10ps) measurements using different technologies (SpaCal/Shashlik, W/Pb, GAGG/Polystyrene)
- ASICs using PMT signal under development in TSMC 65nm (V_{supply}=1.2V)
- Separate energy and timing processing paths:
  - ICECAL65 designed by UB, IFIC and UPC
  - SPIDER designed by IJC Lab, LPC
- PMT conditioning circuit for ASIC input range on base or front-end board (IFIC)

PicoCal: PMT Acquisition & Conditioning Circuit

- COTS based two stage amplifier with intermediate divider/filter.
- Several prototypes with different footprints for testing multiple OpAmps.
- Commercial OpAmps force tradeoff among speed, stability and dynamic range (process 2ns t_{rise}/250MHz BW signal over 40mA/2V range with 50Ω conversion)

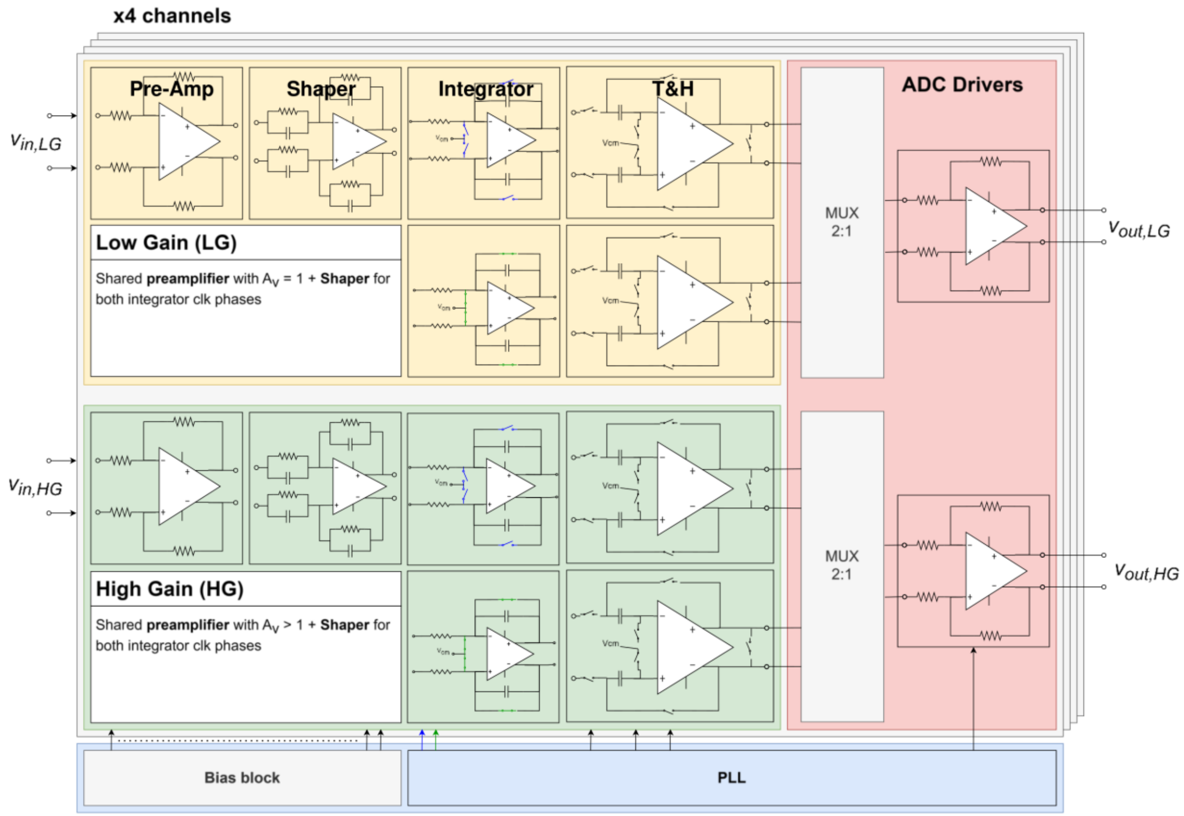


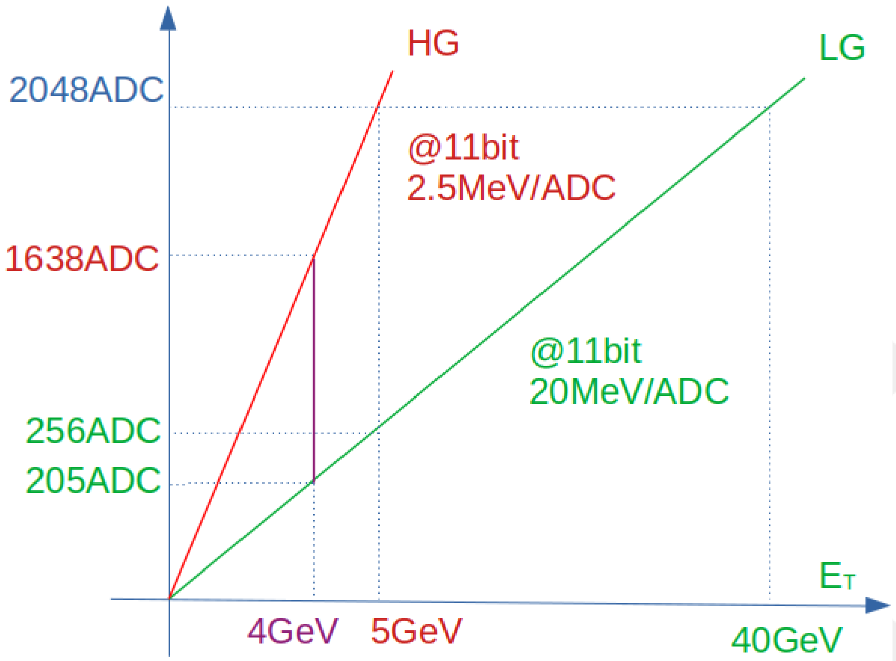


- Intensive lab test to produce a configuration for each board compatible with SPIDER (v1) and ICECAL65 LG (v2 and v3) energy and voltage
- Results show good linearity and <10% rise time loss in all cases
- All boards tested at SPS, analysis and comparison to lab results ongoing

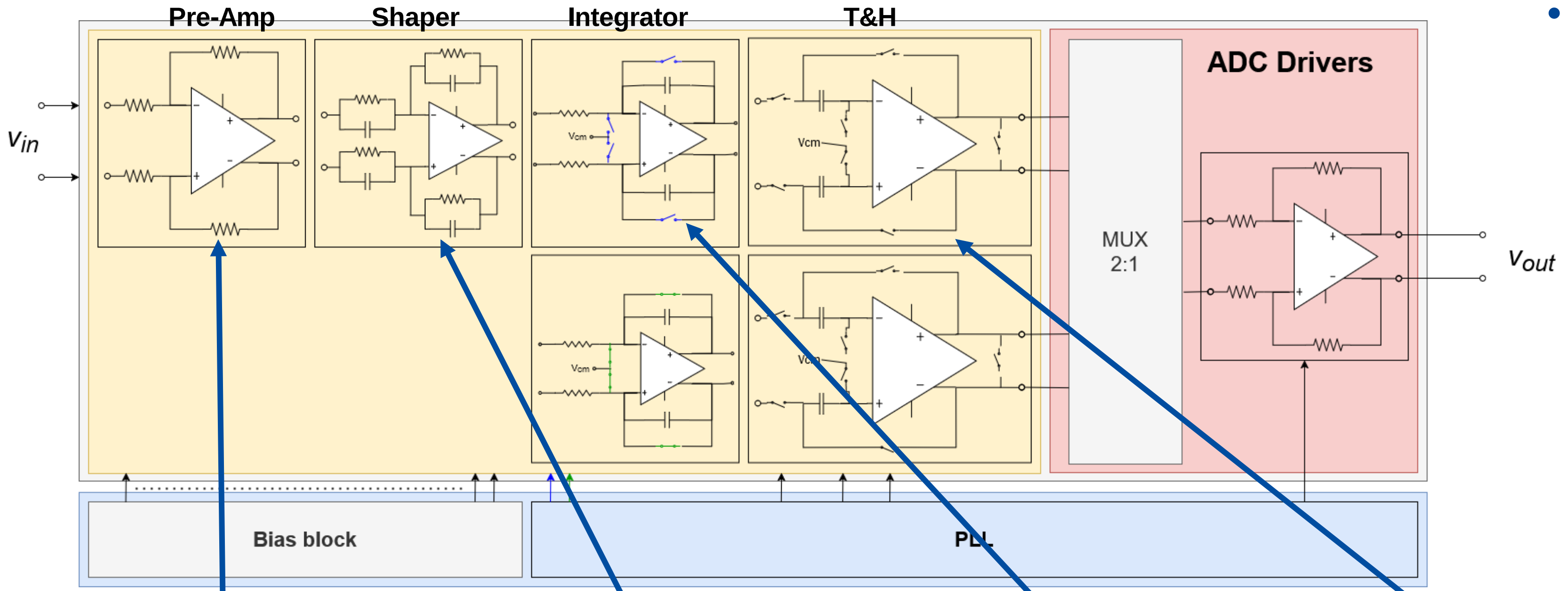
PicoCal: Energy ASIC

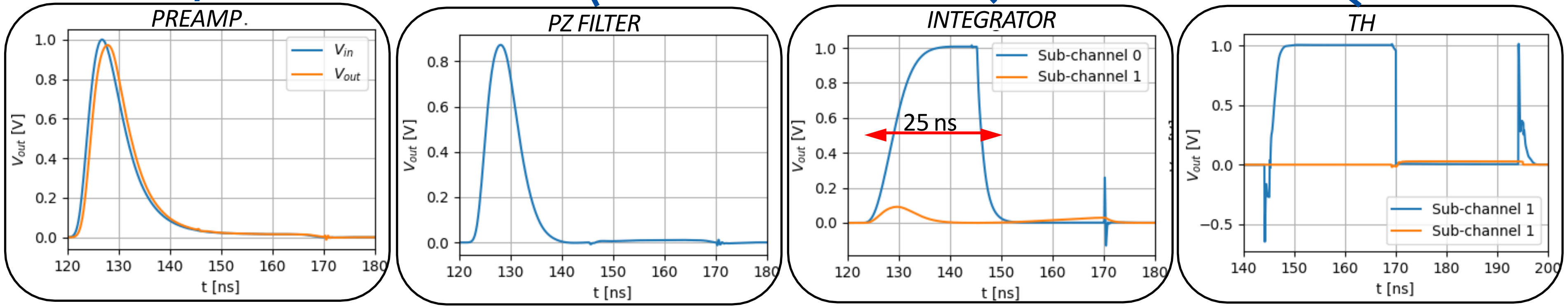
- Two 11bit processing paths with factor 8 between their gains
- Automatic internal selection of gain with fast comparator
- Common acquisition and filtering per gain path with double time interleved switched section for integrator reset
- Per channel clock phase selection to synchronize and set ADC sampling





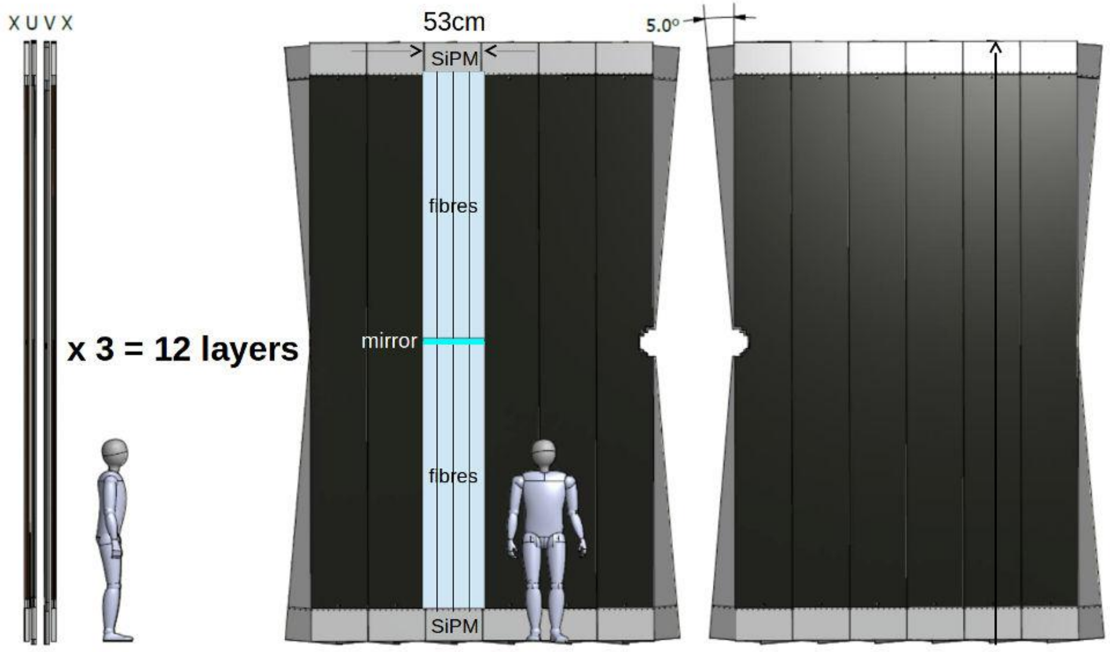
Energy ASIC Analog Channel

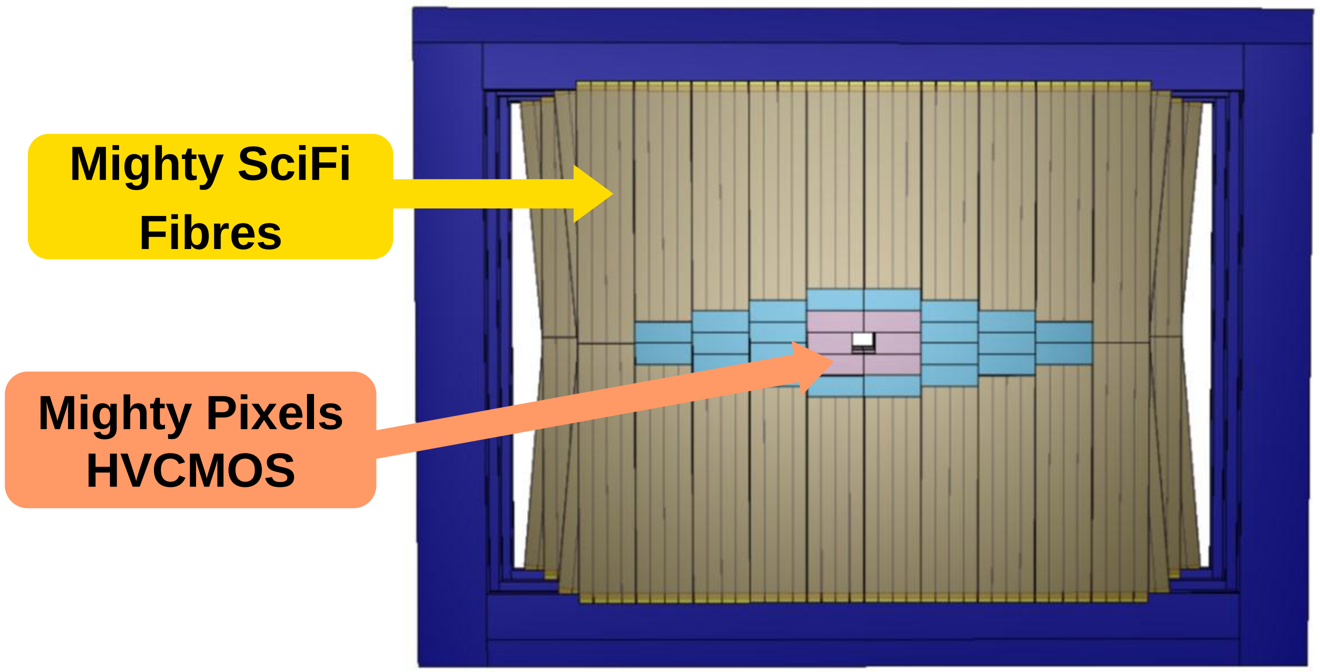




- Analog channel fulfills the specifications
  - HG and LG adjusted in the preamp
  - Precision for 11 bits (HG/LG)
    - Noise < 1 LSB
  - Shape the input signal to fit it within the 25 ns window for all SpaCal technos
  - < 1% variation for ±2 ns to adapt to arrival time fluctuations (Plateau)
  - Adjustable parameters for filtering and gain
- Design status: blocks layout done

Mighty SciFi readout electronics





- LS4 radiation levels require new detectors/electronics! (IFIC, UB, UPC)
- Mighty Tracker: three stations with four layers each in XUVX configuration
- CMOS MAPS (Si pixel) inner region / scintillating fibers + SiPMs outer region

PACIFIC (Upgrade I, current)

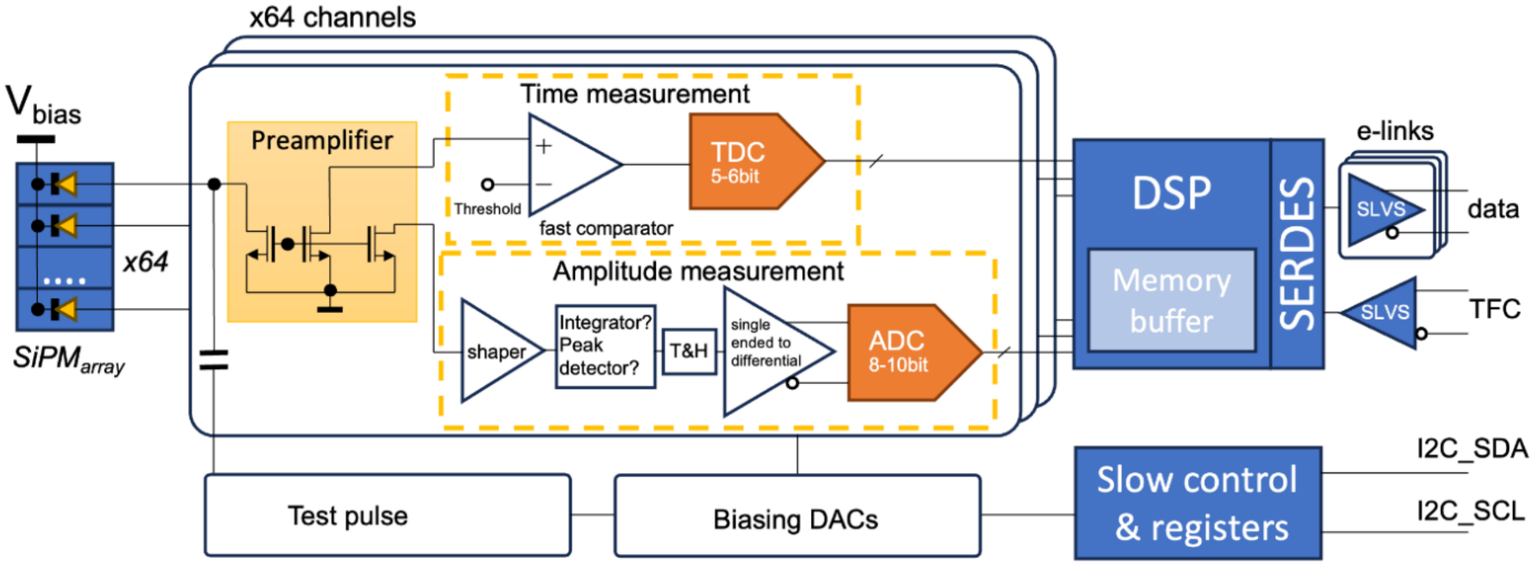
- Mostly analog design
- Multi-channel
- Simple digitization
- I2C slow control

PACIFIC++

- Analog processing chain
- Multi-channel
- Complex digital: digitization/clustering/timing
- IpGBT control/direct connection

PACIFIC++

- SiPM readout ASIC with anode DC coupling and current mode input
- Two processing paths with 10bit ADC and 6bit TDC respectively
- Integrated digital processing (cluster) and Gbps serialized output
- Double interleaved scheme for integrators to allow continuous operation
- Low power single-ended and differential OTAs required for analog chain (power 1-2mW; GBW 250MHz; SR 200mV/ns; noise 500µV)

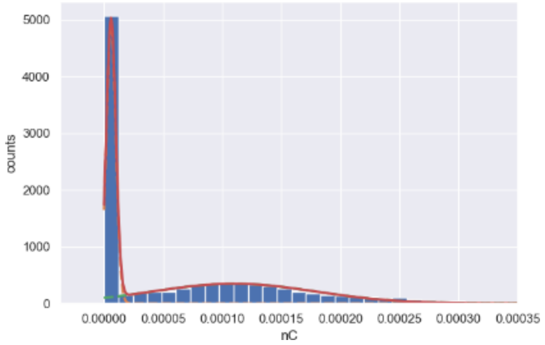


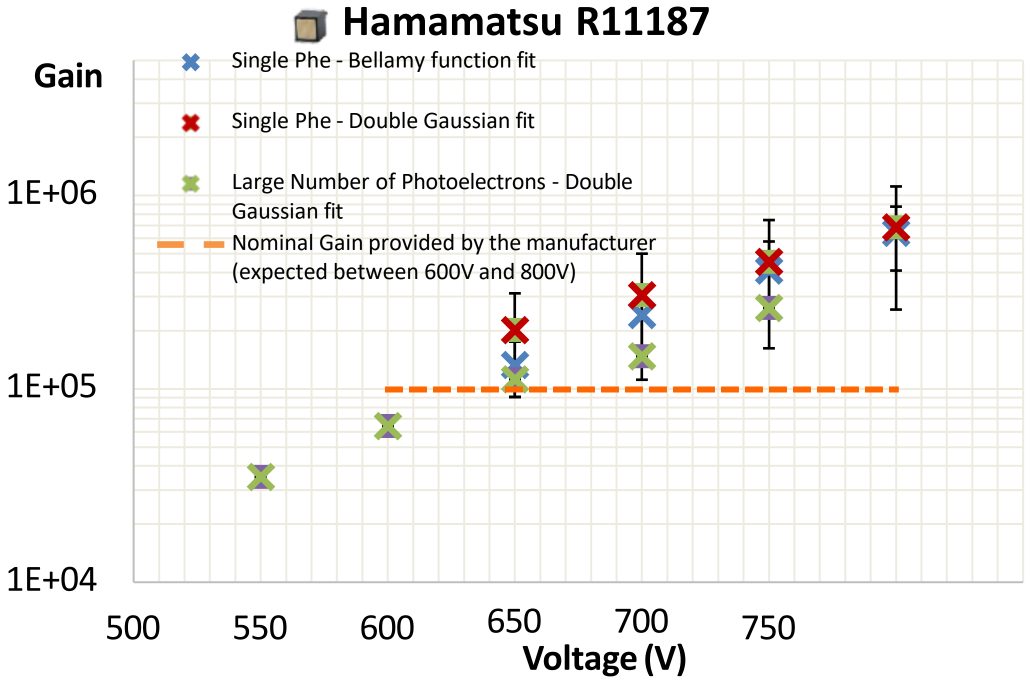
Parameter	PACIFIC++
Technology	**65 nm**
Number of channels	64
Channel connection	Single ended, DC coupled
Signal polarity	Positive
Gain	4 different gains
Sensor bias	**Not needed**
Power consumption	1.2V 0.5 W + 2.5V 0.5 W
Shaping	Tuneable tail cancelation
ADC	**ADC 10 bits**
TDC	**≈0.4 ns, 6 bits**
Calibration	Integrated charge injection
DSP	**Clustering and raw output**
I/O interface	**eLinks @ 1.28 Gbit/s**
Slow control / TFC	I2C / eLink

- Submission of 1st prototype by 2026

PMT studies at UB

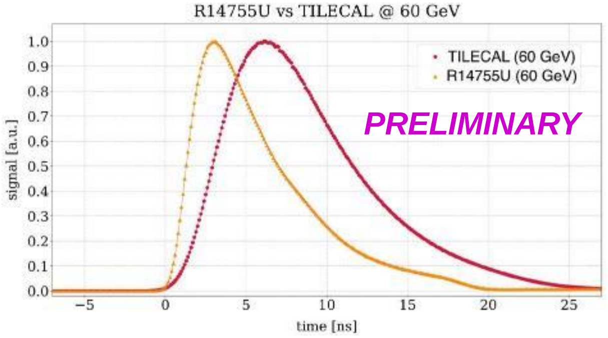
- Gain studies
  - Single Phe fit with 2 Gaussian or with Bellamy distribution
  - High N_{phe} statistical methode





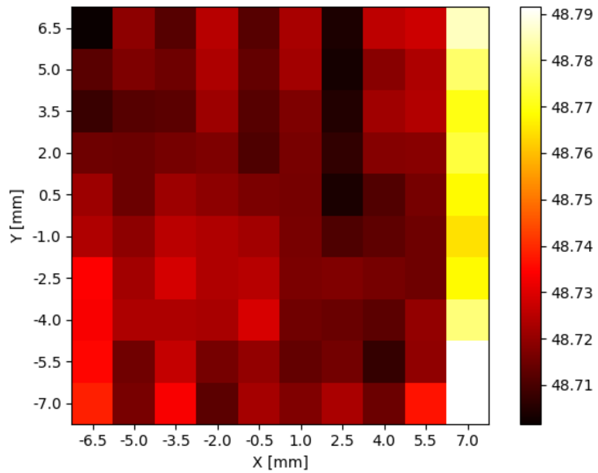
- Time resolution uniformity scan over photo-cathode and for different bias and light conditions

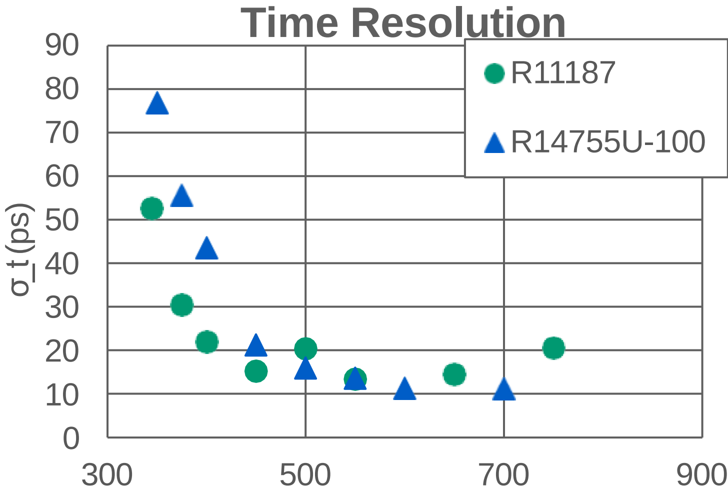
Grid of points, (laser)



Arrival time uniformity over R11187

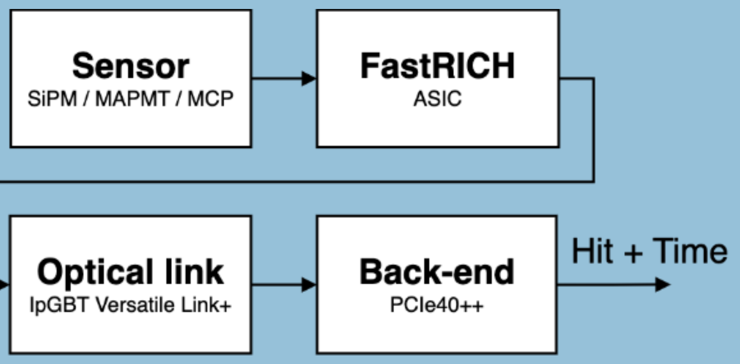
- ✓ total std = 32 ps



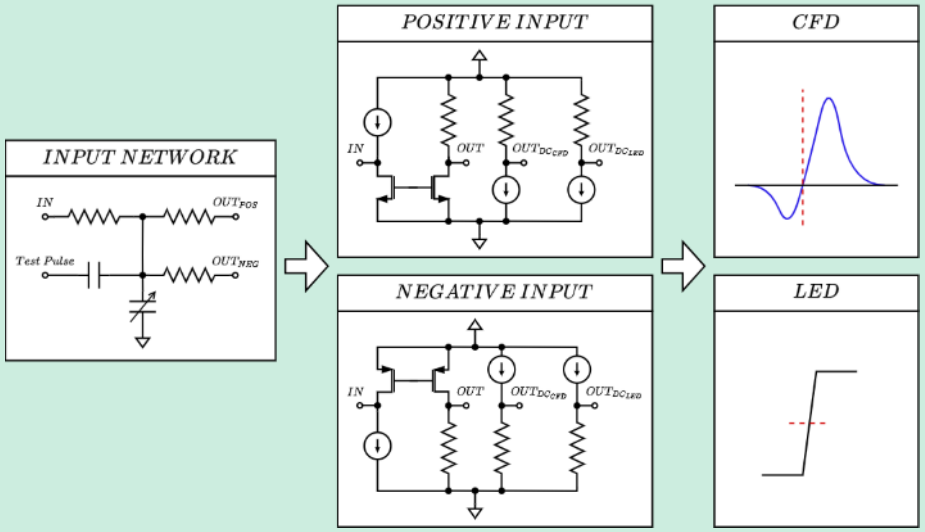


FastRICH ASIC – Analog FrontEnd (Positive Input Stage)

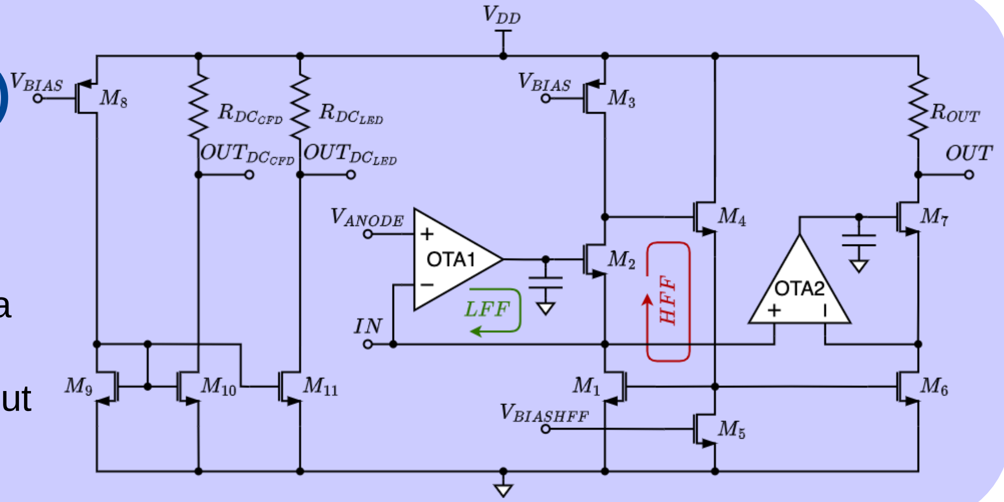
- **HL-LHC Run 5 RICH system**
  - Challenging rise in particle multiplicity and hit occupancy during HLLHC
  - The increased irradiation level FPGAs → radiation-hard ASIC
  - in order to keep the high particle ID → time resolution of better than 100 ps
  - Upgrade to SiPM



- **FastRICH ASIC**
  - 65 nm tech
  - Based in FastIC
  - Specific for RICH
  - CFD, LED and TDC included
  - Radiation Tolerant



- **Positive Input Stage (for SiPMs)**
  - Designed at ICCUB
  - Current-mode with Zin < 50Ω
  - Optimized for small area (1x1 mm² SiPMs)
  - Pseudo-differential output voltage



Spain@futureLHCbRTA

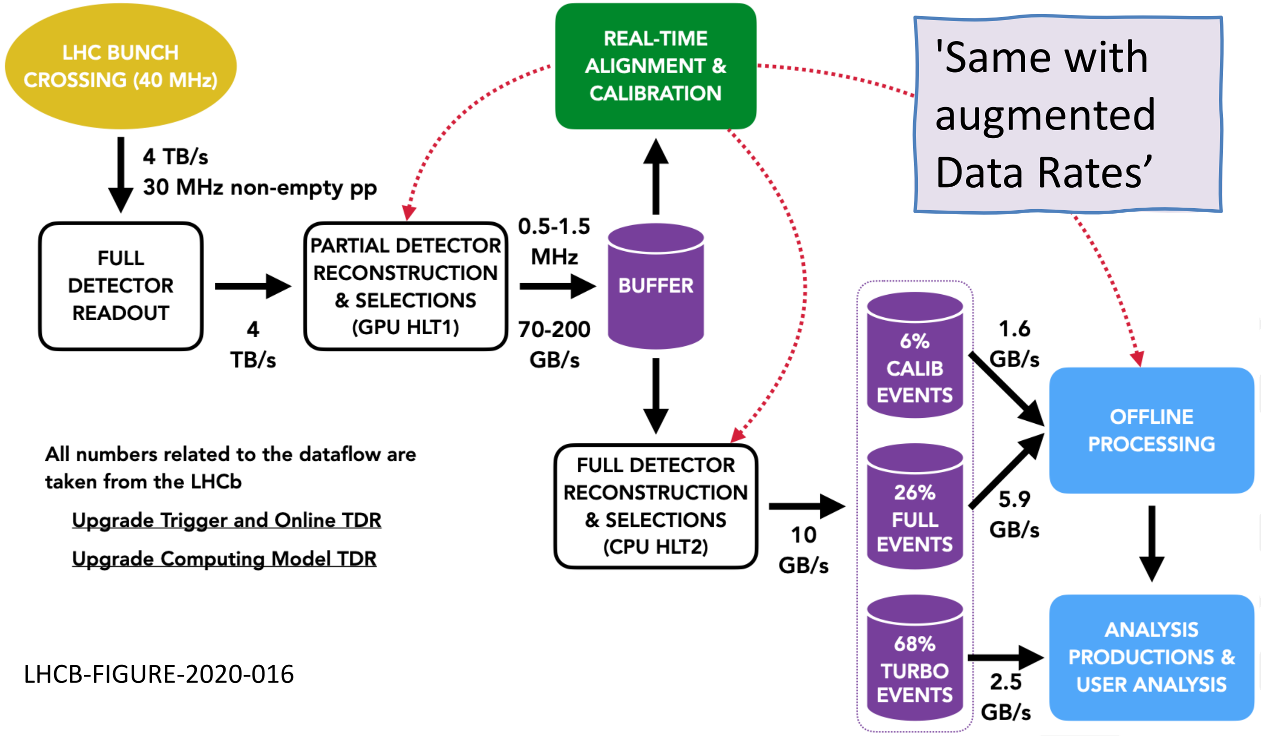
"The planning for the RTA and Online systems assumes that this underlying logic will continue in the Upgrade II period, albeit with new algorithms to make use of timing information."

LHCb Upgrade II Scoping Document   CERN/LHCC 2024-10

UNIVERSITAT DE BARCELONA

IFIC INSTITUT DE FÍSICA CORPUSCULAR

laSalle UNIVERSITAT RAMON LLULL



LHCB-FIGURE-2020-016

Assuming continuity

- Calorimeter Reconstruction - GNNs (UB, LS-URL)
- Tracking (Valencia, Corunha)
- LLP trigger lines (Valencia)
- Retina DWT– FPGA Velo Reconstruction (Valencia)
- Neutral PID (LS-URL)
- Trigger lines (all)
- Flavour Tagging persistency (Corunha)

→ LHCb RTA


R&D

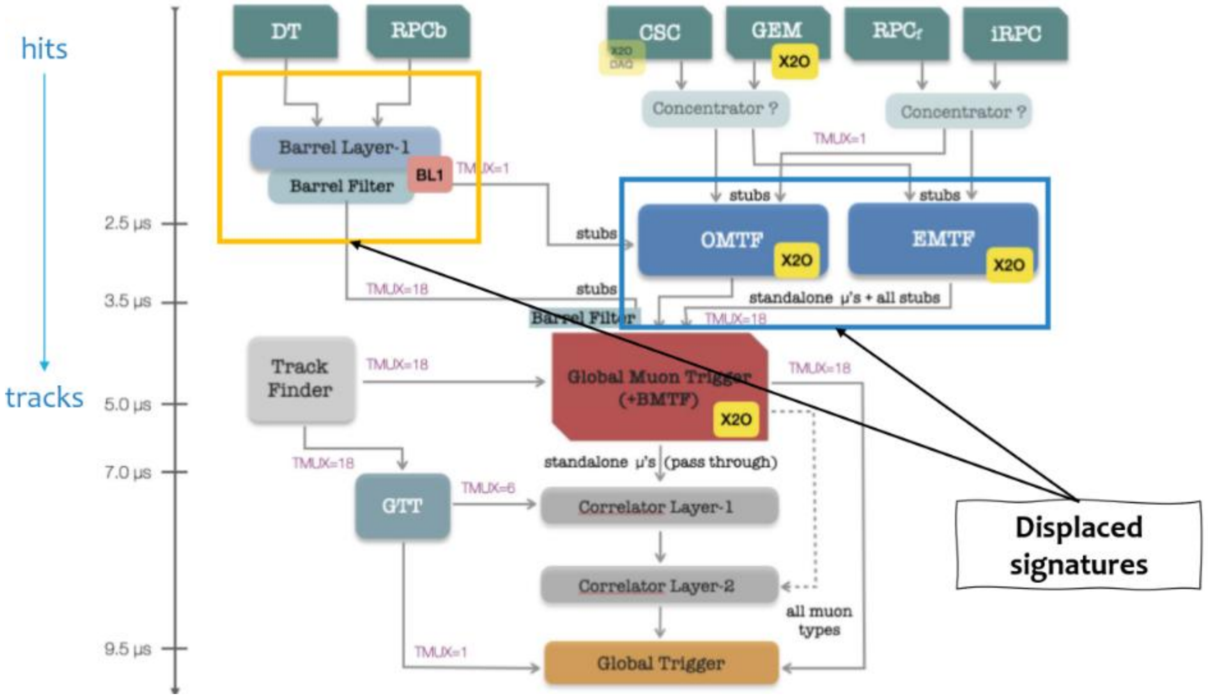
INTREPID Project

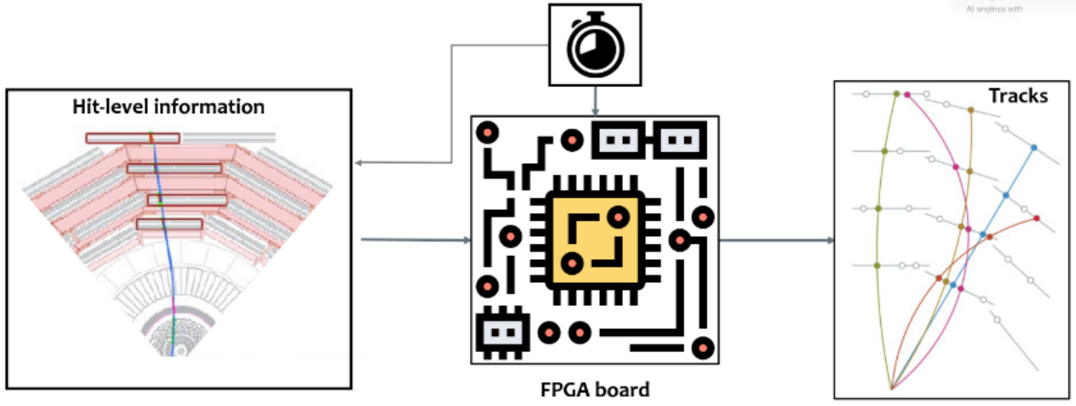
- Got funding from the ERC to explore alternative technologies and ideas which could not be otherwise investigated that could potentially lead to a significant breakthrough.
- **Project focuses on muons signatures**, but ideas can be ported elsewhere and targets to expand the sensitivity to long-lived / displaced signatures.
- For the **HL-LHC and beyond**:
  - Muon trigger for the HL-LHC (in collaboration with CIEMAT): expand existing low-latency algorithms to detect and trigger on non-standard signatures such as hadronic showers or slow charged particles.
  - GNN for real-time (O(μs)) muon reconstruction, using Versal ACAP and the AI engines.
- Hardware/Setup:
  - Setting up a local test stand for benchmarking firmware.
  - Various devices available for testing: Xilinx Kintex, Virtex Ultrascale+, Versal 7nm AI.
- Person power:
  - 4 PhD students (full time), 1 postdoc (full time), 2-3 senior (0.5 FTE each)

Funded by the European Union
European Research Council
Established by the European Commission

What are the INTREPID goals?

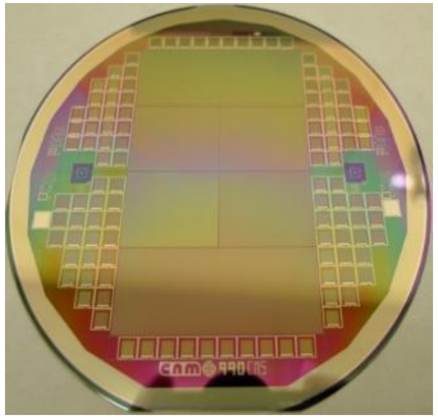
- LLP signals might be easily missed or misinterpreted in LHC data.
- Optimizing the techniques within the current architecture to improve detection efficiency without requiring significant hardware upgrades.
- **Explore alternative technologies and ideas which could not be otherwise investigated that could potentially lead to a significant breakthrough.**
  - Can we profit from using hit-level information?
  - Use of 7nm technology?



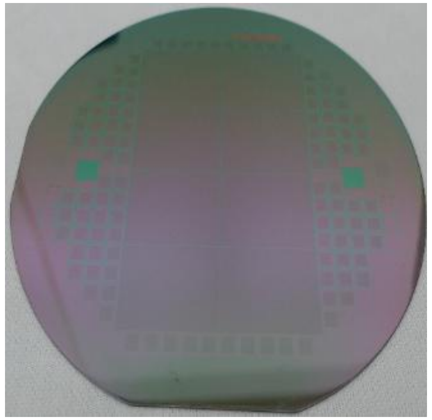


Funded by the European Union
European Research Council

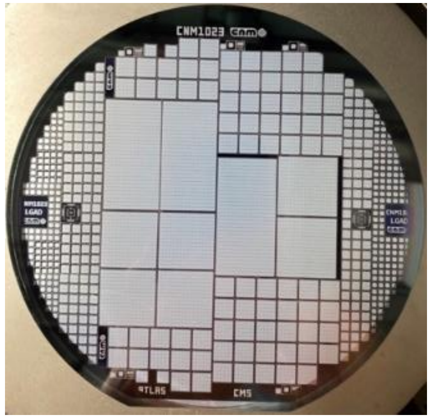
Technological Processes Developed @ IMB-CNM



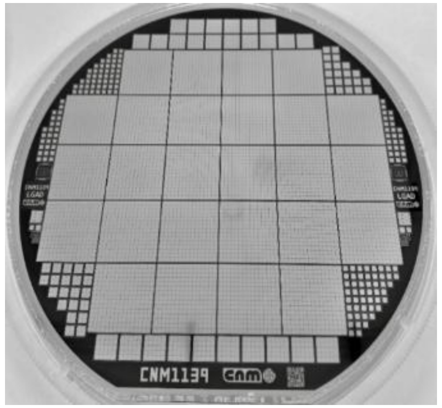
Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **3D-SS** sobre substratos SiSi. Primera generación



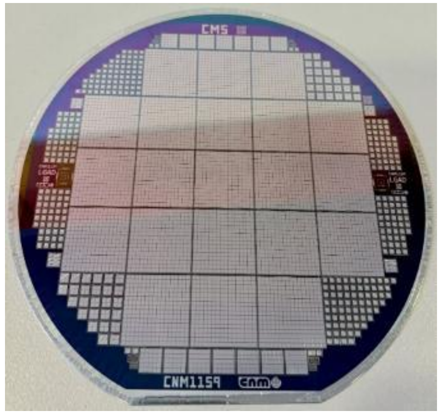
Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **3D-SS** sobre substratos SiSi. Segunda generación, Nivel N+



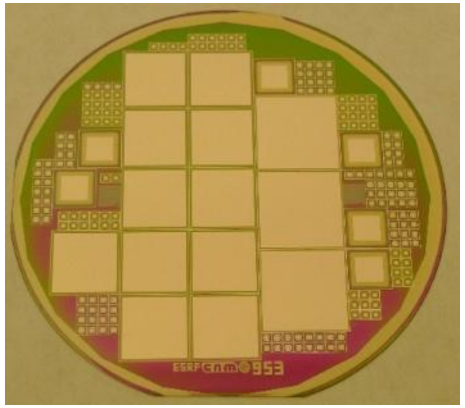
Oblea de 150 mm de diámetro en la que se integran prototipos de detectores **LGAD** delgados sobre substratos epitaxiales y **perfil original**



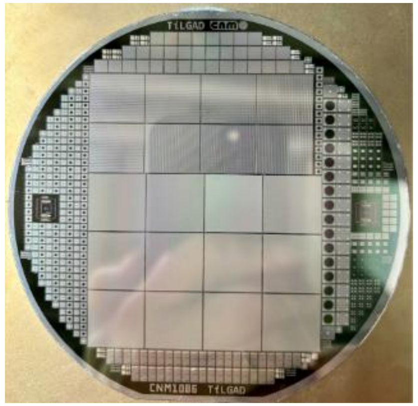
Oblea de 150 mm de diámetro en la que se integran prototipos de detectores **LGAD** delgados sobre substratos Si-Si. Módulos **15x15** con **perfil original**



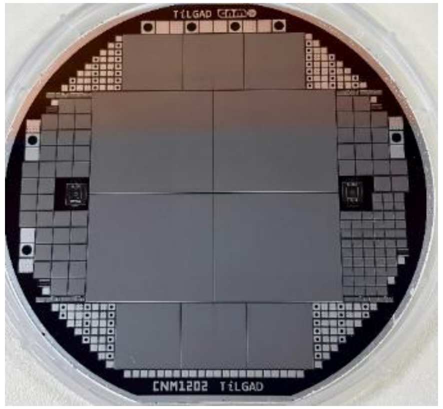
Oblea de 150 mm de diámetro en la que se integran prototipos de detectores **LGAD** delgados sobre substratos epitaxiales. Módulos **16x16** con **perfiles original y profundo**



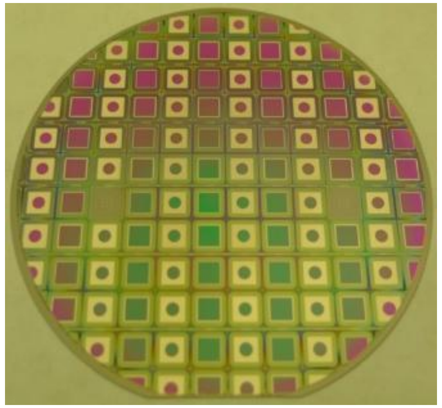
Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **iLGAD** de segunda generación con **perfil original**



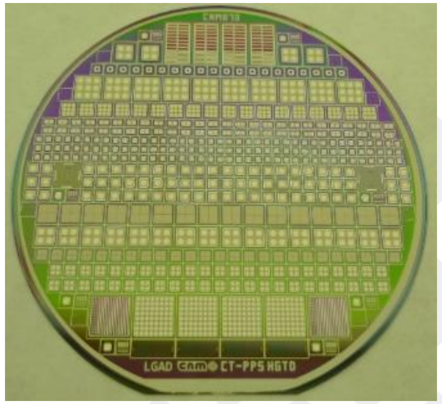
Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **Trench iLGAD** con diseño **Timepix3**



Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **Trench iLGAD** con diseño **Timepix4**



Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **nLGAD** de primera generación

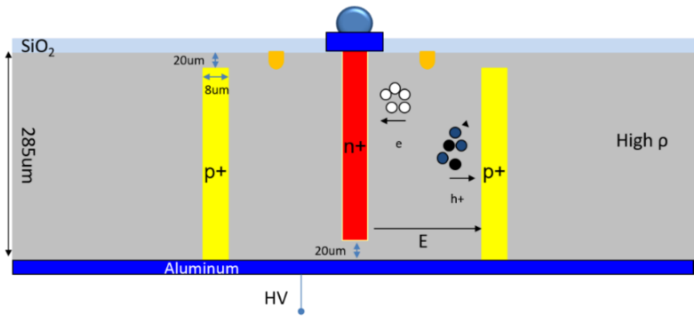


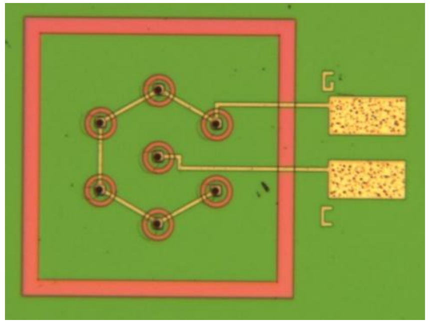
Oblea de 100 mm de diámetro en la que se integran prototipos de detectores **nLGAD** de segunda generación

Current Detector development @ IMB-CNM

3D timing for future tracking. Atlas and CMS timing layers :

- 3D Technology stabilization (100mm → 150mm)
- Devices for extremely harsh environments ($>2\times10^{15}$ n/cm^2) :
  - Silicon 3D timing devices
  - Future timing layers based on 3D technology



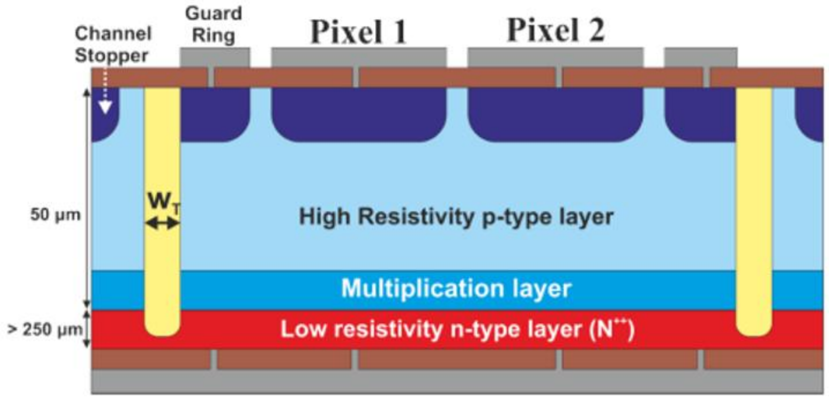


SiC detectors for Particle Physics and Nuclear Physics (IEM-CSIC):

- Devices for extremely harsh environments:
  - Silicon Carbide (SiC) based devices
- SiC diodes for X-ray detection and Beam monitoring

LGAD timing for timing and tracking applications :

- Inverse LGADs and Trenched iLGADs → 100% fill factor while maintaining precise tracking and timing information
- Deep Junction LGADs
  - More radiation hard (<2×1015 n/cm2)
- Technology Stabilization, increasing yield in 150mm wafers and large sensors
- N-type LGAD development for DUV and soft X-ray detection



imasenic

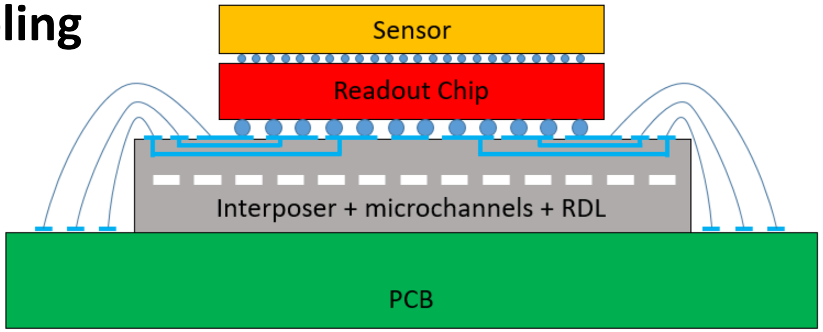
CMOS imaging sensor simulation (Imasenic and DRD3):

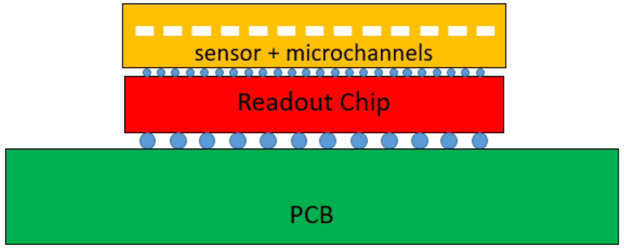
- Development of a simulation framework for the production of HV-CMOS detectors

Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

WP5 - Technology cooperation // T5.5 Collaborative projects with CSIC. Leader: CSIC. FMD-OFC, IZM

Task 5.5.1: Microchannel cooling





Miguel Ullán (IMB-CNM, CSIC)

CSIC — Consejo Superior de Investigaciones Científicas

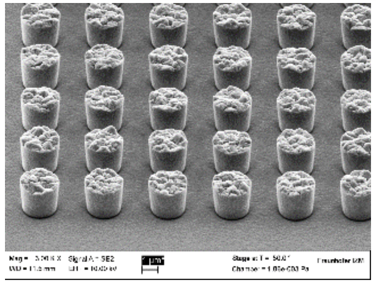
- **Integration of embedded microchannels with RDL in silicon interposers**
- **Cooling microchannel fabrication in sensors or ASICs**
- **Qualification of cooling concept**

Fraunhofer IZM

- **ASIC thermo-test chip fabrication**
- **IO pitch reduction for hybrid assemblies**
- **Heterogeneous integration**

Focus IZM: IO pitch reduction for hybrid assemblies

Sub-10µ-pitch



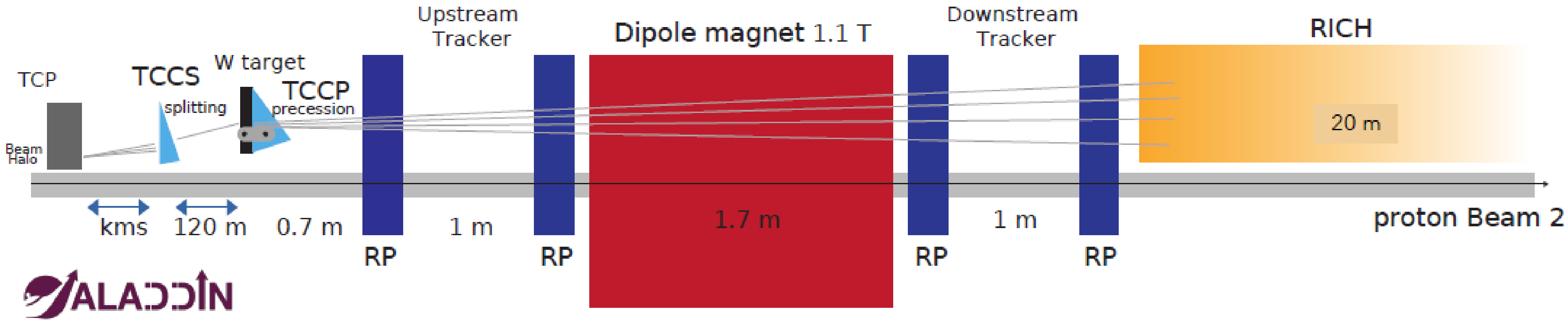
4µm pitch Au pillars

➡ **Services offered for (future) pilot-line customers:**

- Microchannel cooling for HPC and RF – Application
- Hybrid Assembly Technologies for HPC – Application

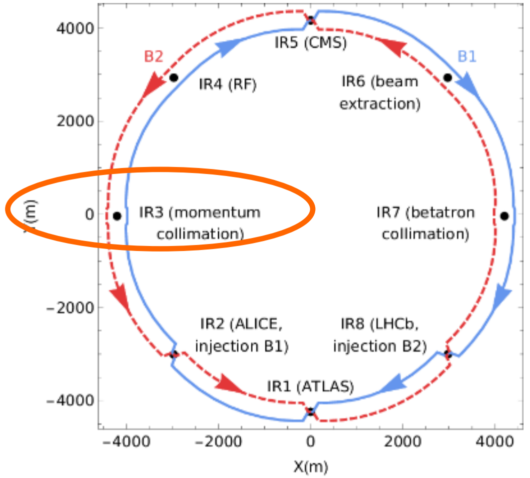
Aladdin Experiment

- In-vacuum fixed-target experiment for direct measurement of magnetic and electric dipole moments of charm baryons at the LHC. Ultimately explore τ lepton
- Letter of Intent (LoI) in July 2024, endorsed by LHCC. Technical proposal by June 2026



ALADDIN

An Lhc Apparatus for Direct Dipole moments INvestigation



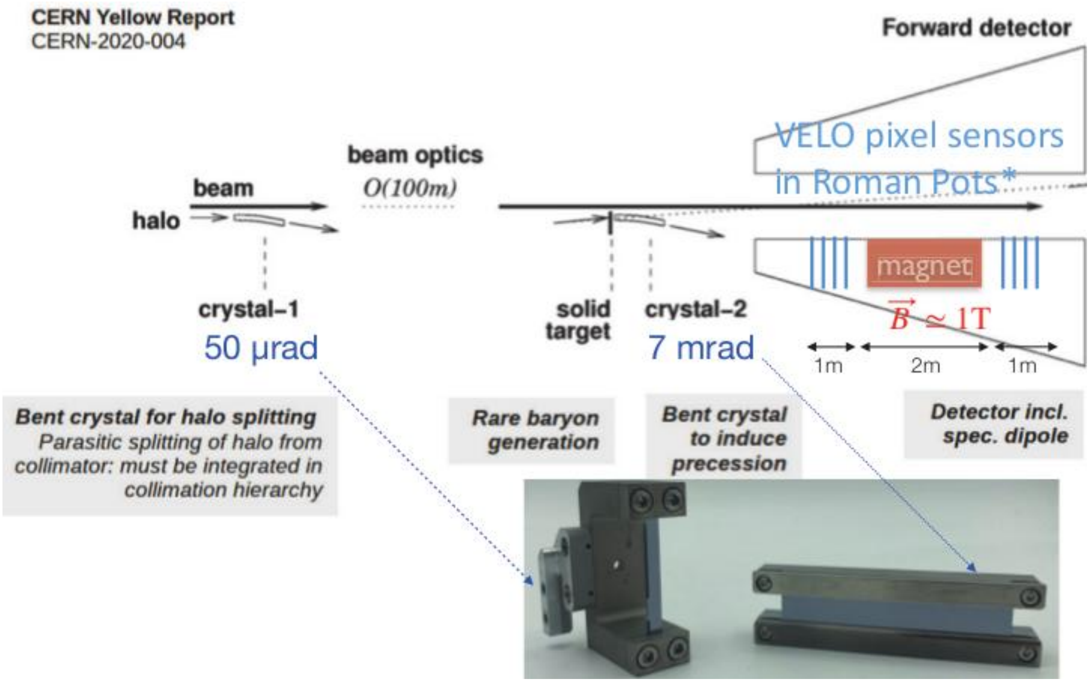
Crystal 1 (TCCS): halo extraction of the LHC beam
Tungsten target - 2 cm
Crystal 2 (TCCP): spin precession of baryons with charm
Spectrometer: baryon reconstruction with a 1.9 Tm magnet
Particle identification detector – RICH (for p, K, p PID up to 1 TeV)

- Strong synergy with LHCb physics program and LHCb Upgrade II technologies
  - VELO PicoPix, RICH, DAQ, Real Time Analysis

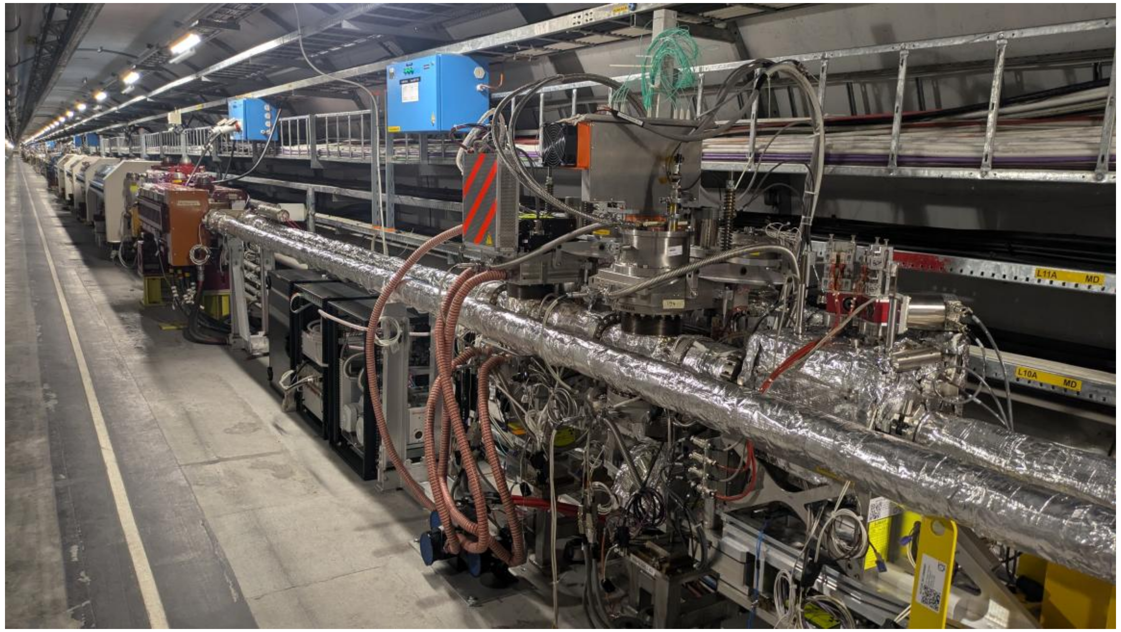
https://cds.cern.ch/record/2905467

https://aladdin.web.cern.ch/

Twocryst: Aladdin Proof-of-Principe at LHC IR3



TWOCRYST



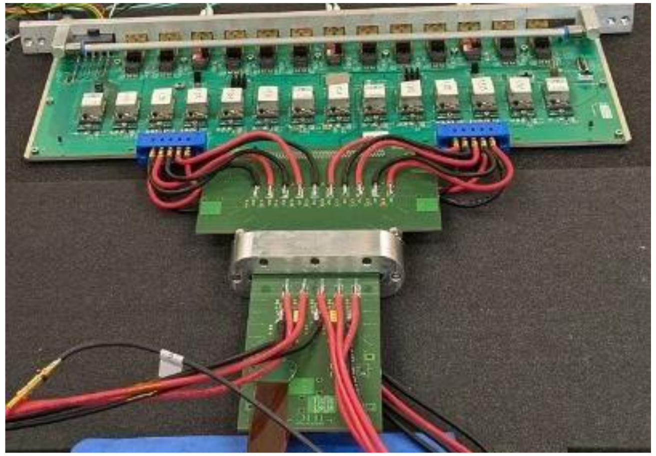
Demonstrate:
- Machine operation & achievable PoT
- Detector setup & measurement of TeV regime channeling

- Machine: beam manipulation using bent crystals
  - Bent crystals: Si with mechanical bending as baseline. Deflection of beam halo towards W target
  - Goniometers for precision bent crystal positioning
- Magnet: compact spectrometer dipole magnet
  - Warm dipole magnet already available in situ (1.9 T m) as baseline (orbit corrector)
- Detector: compact with high granularity, covers very forward region ($\eta > 5$)
  - LHCb VELO silicon pixel sensors & electronics inside Roman Pots (from ATLAS-ALFA)

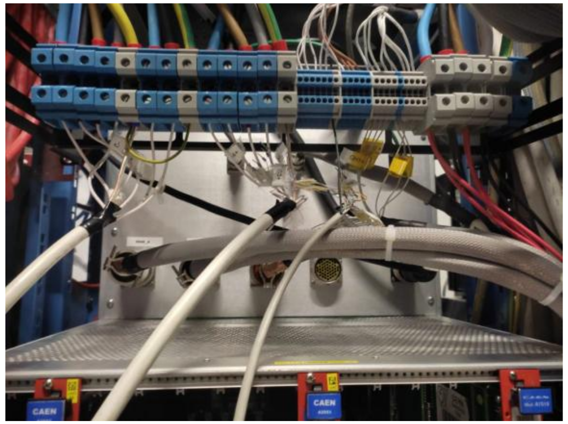
https://twocryst.web.cern.ch

TWOCRYST contributions

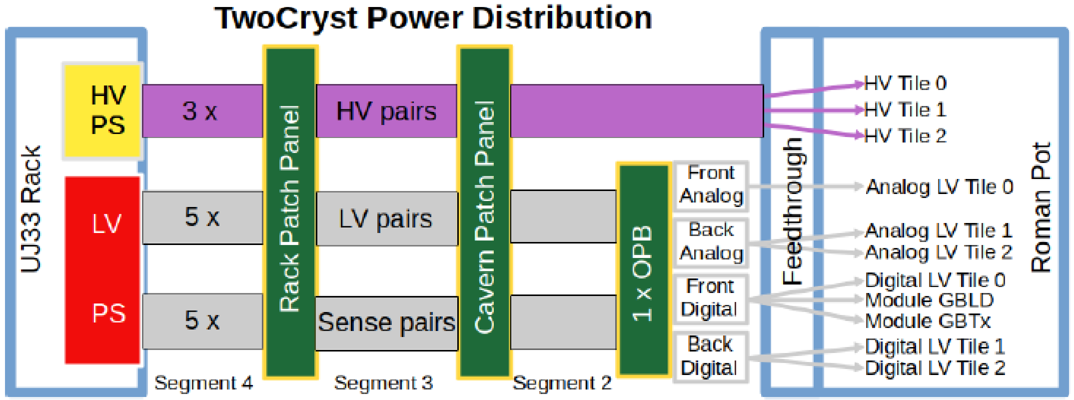
Voltage Feedthrough Board (VFB)



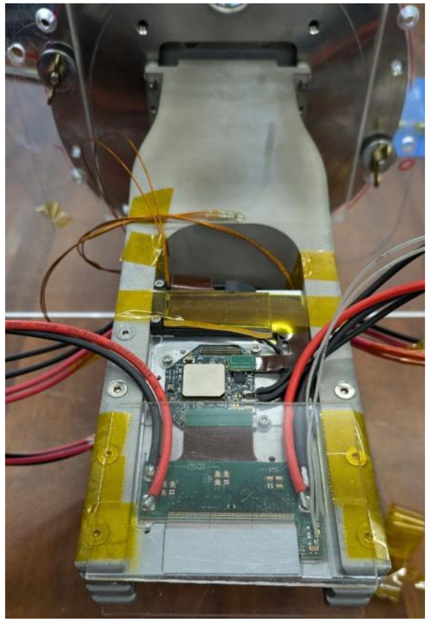
Power Patch Panels



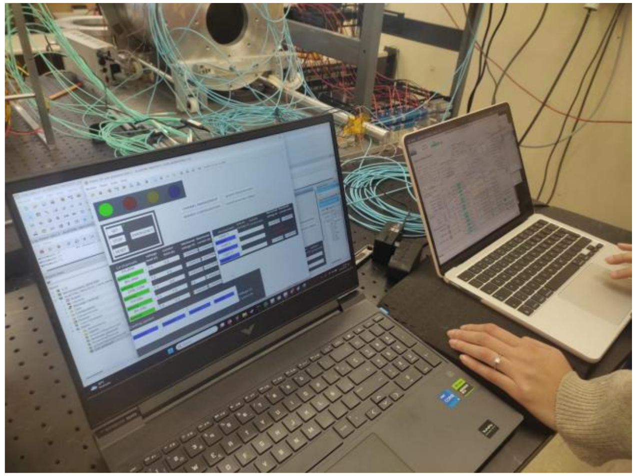
Power distribution system & 300 m cabling inside LHC tunnel



Flexible Front-End PCBs (RP)

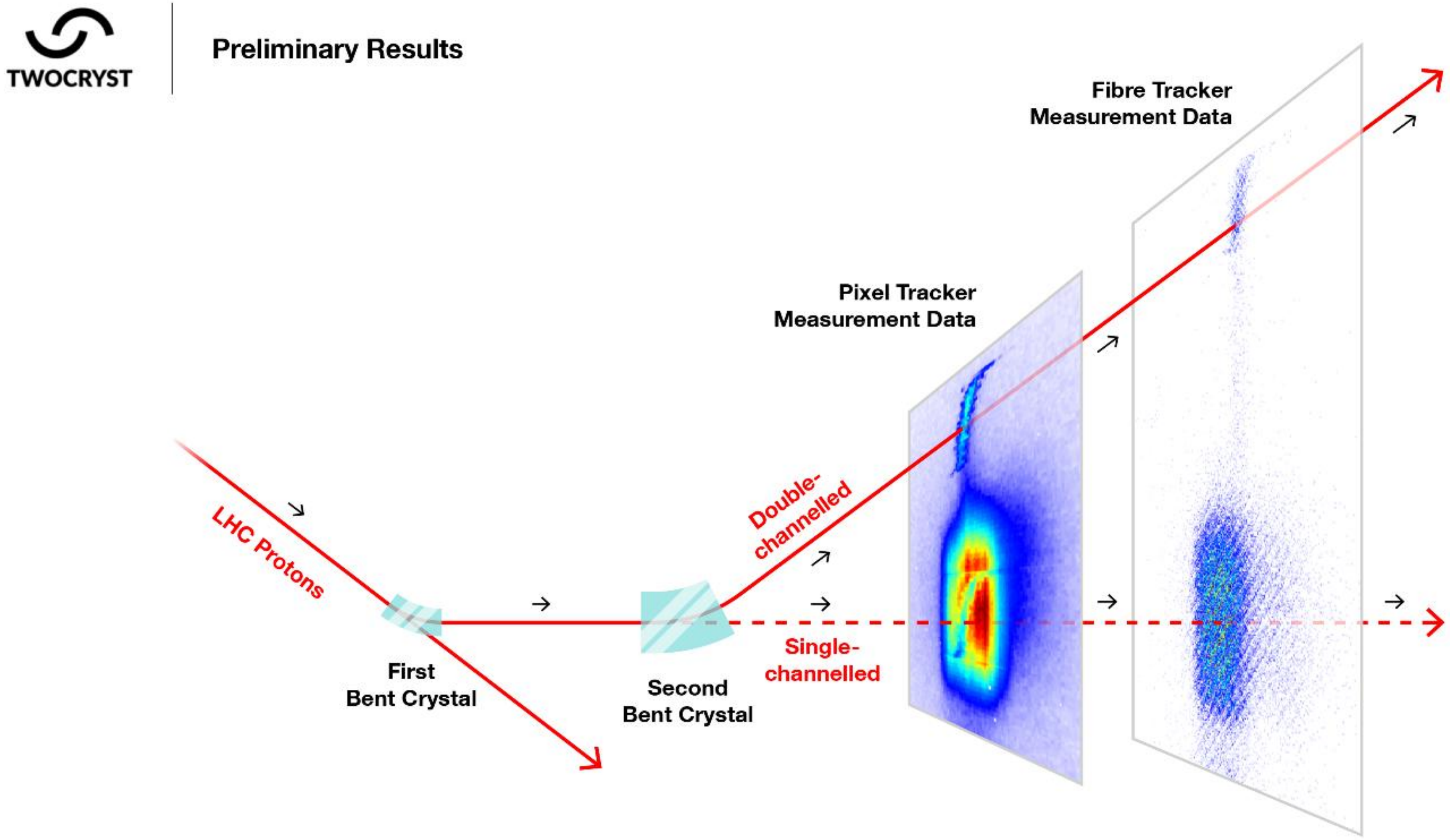


Monitoring & control system (SCADA)



Installation & commissioning

TWOCRYST preliminary results



MDs 21-22 June 2025

https://www.home.cern/news/news/experiments/towards-new-physics-bent-crystals

Thanks for your attention

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