Status of the Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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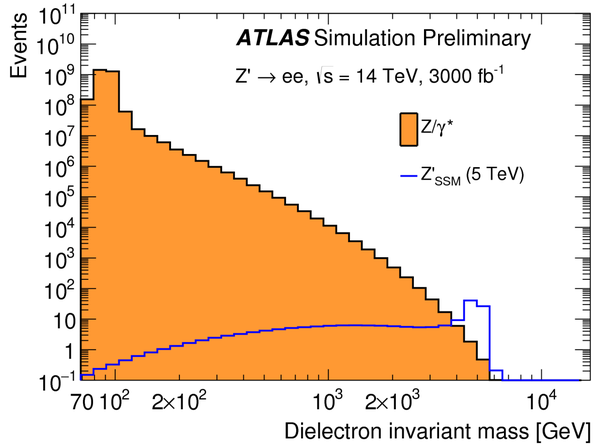
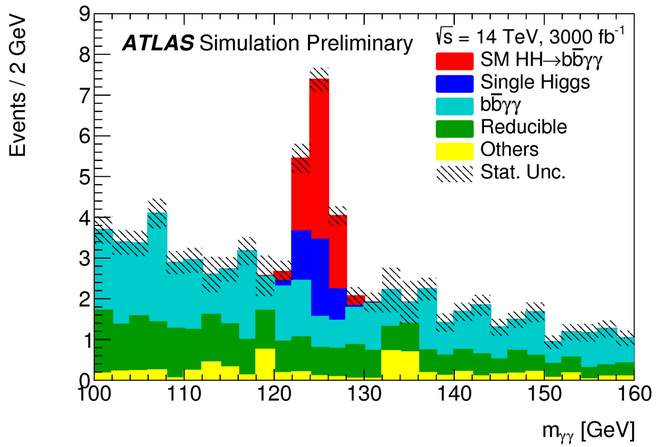
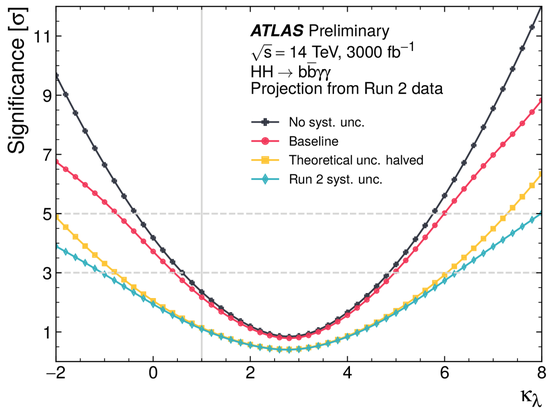
Why do we need the HL-LHC upgrade?

- **High-Luminosity** LHC will **increase** the **amount** of collisions by a **factor 10**.
  - **More collisions** provide **more statistics**: we can look into very **rare processes**!
- The **ATLAS physics program** will focus on key **Standard Model** measurements and the search for **new particles**.
  - **Electron** and **photon energy**, **position** and **timing** measurements are **critical**: LAr upgrades to meet these stringent demands.



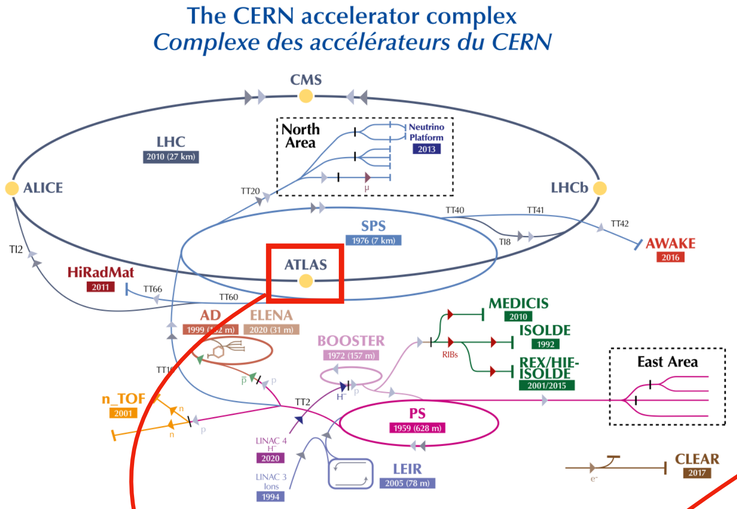
High dynamic range needed for very high energy electrons from eg. a massive Z' decay. See ATL-PHYS-PUB-2018-044.

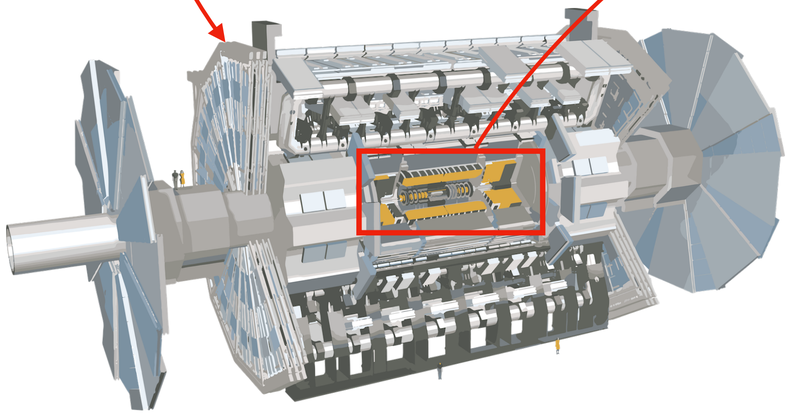




Precise mass resolution (i.e. small peak on large background) need for instance for di-Higgs observations. See ATL-PHYS-PUB-2018-053 & ATL-PHYS-PUB-2022-018.

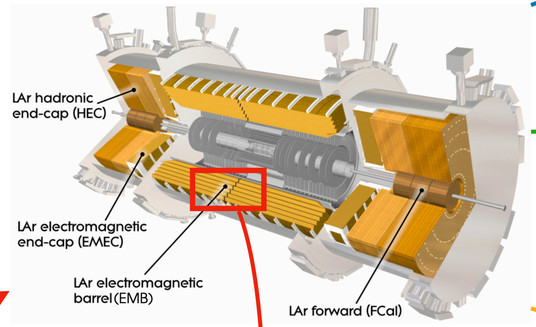
The ATLAS Liquid Argon Calorimeter

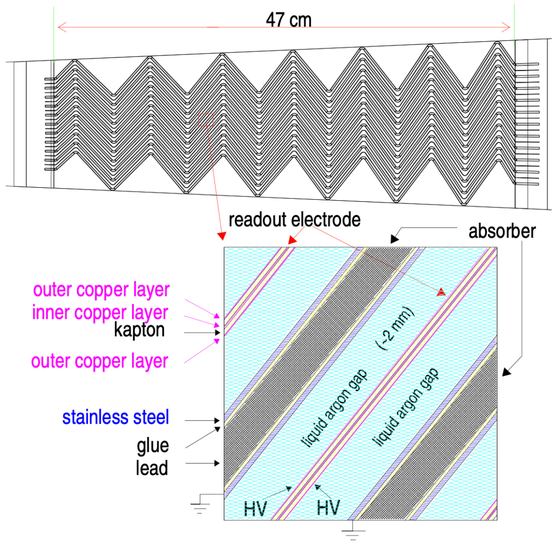




The ATLAS Detector

The Liquid Argon (LAr) Calorimeter





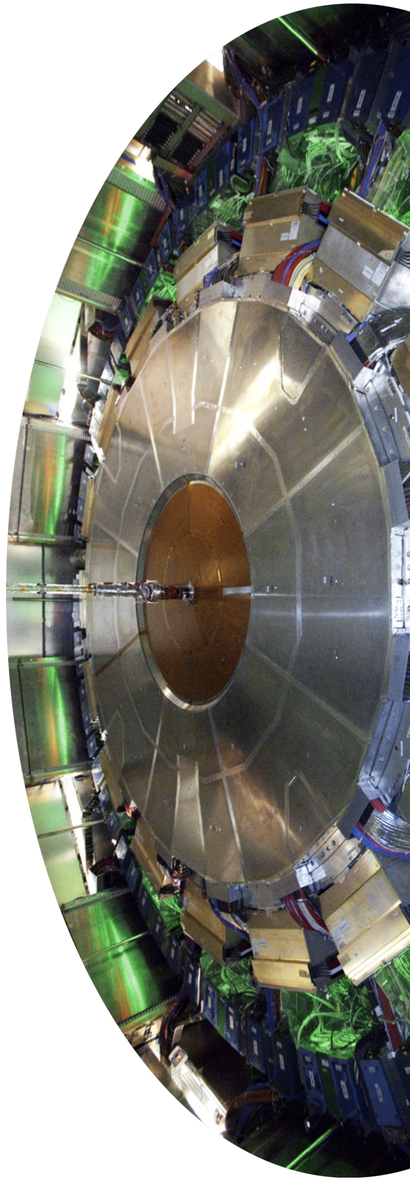
Measures: **energy, position** and **timing** of electromagnetic showers (photons, electrons and jets).

Design: a **sampling calorimeter** with **active** (LAr) and **passive** (lead) layers in **accordion** geometry.

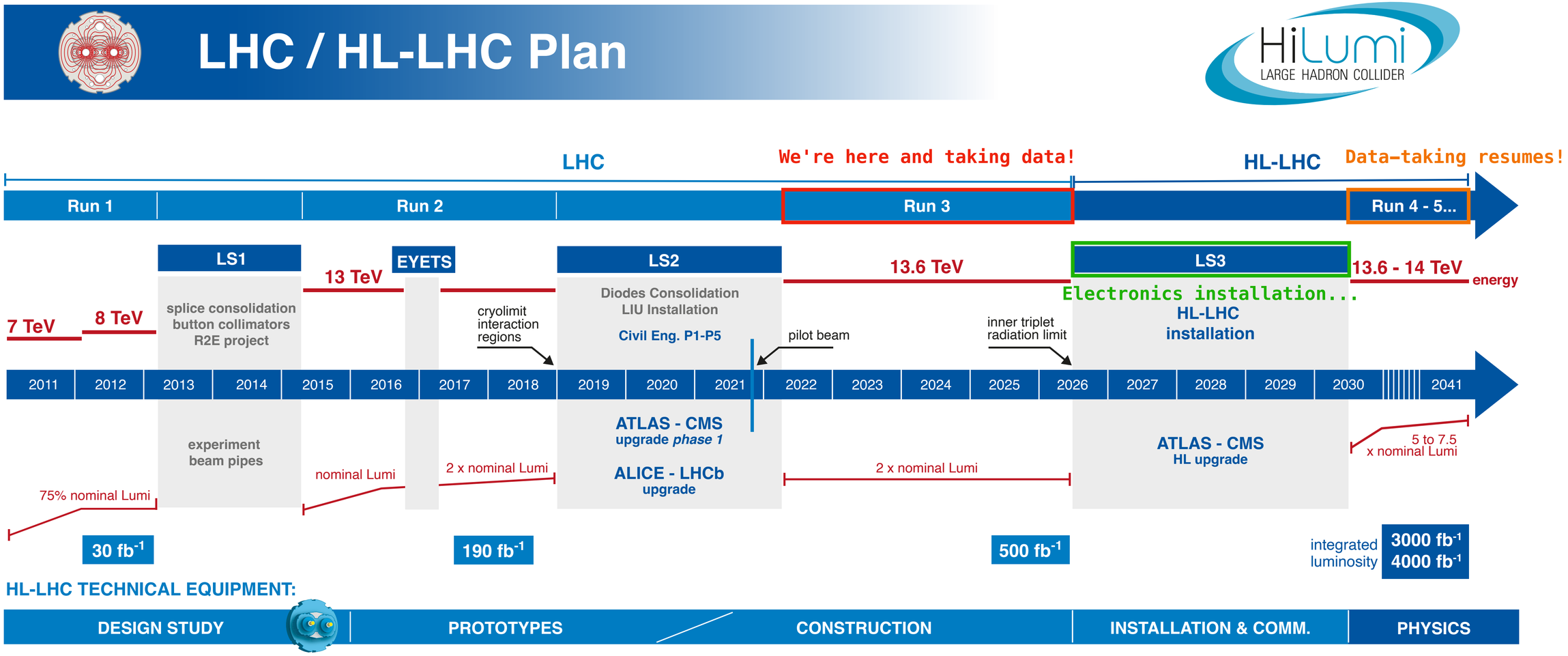
Readout: electronics sample **182k cells** at **40 MHz** and send **digitised** pulse off the detector for **analysis** and **triggering.**

Accordion structure of the **EMB.** The **top** figure is a view of a **small sector** of the **barrel** calorimeter in a plane **transverse** to the LHC **beams.**

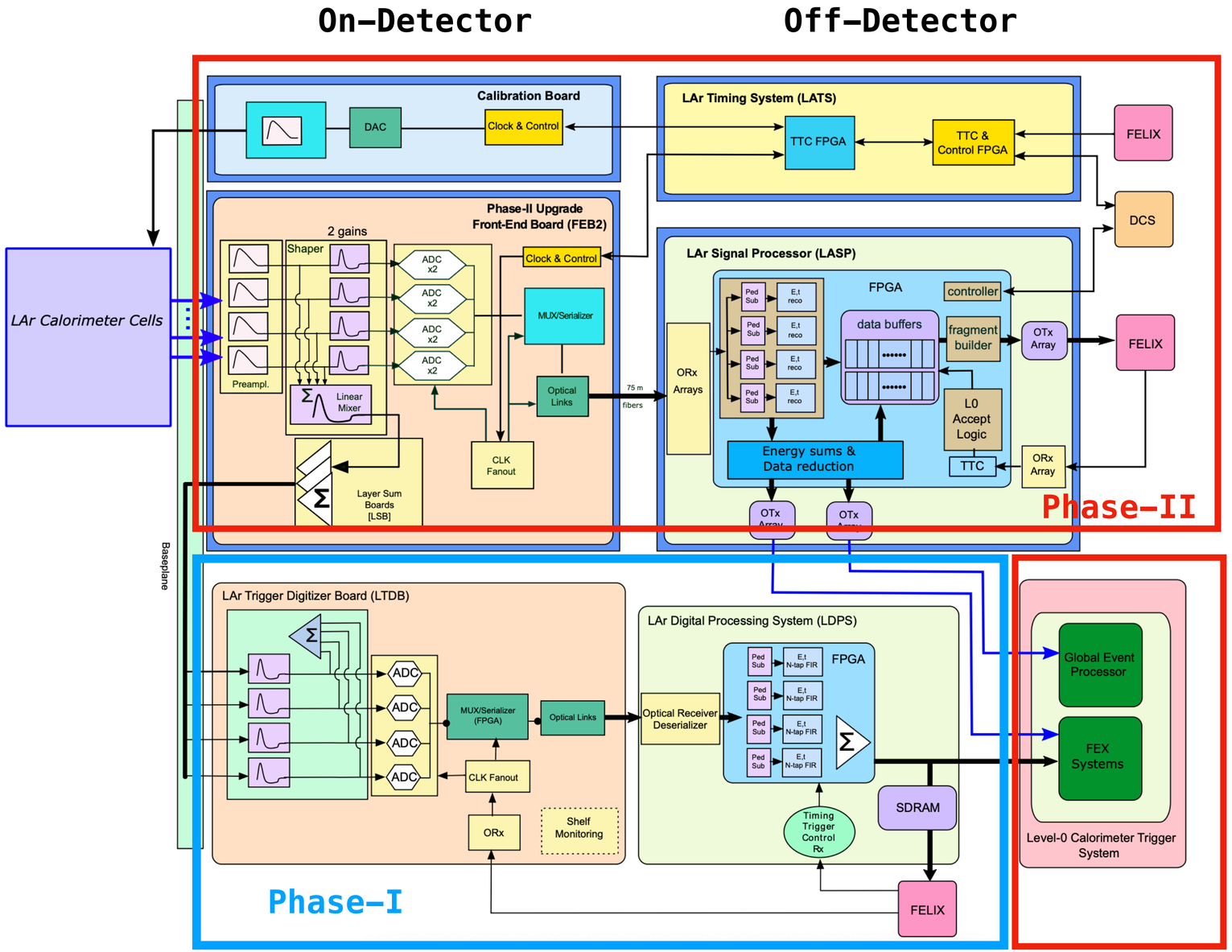
The **HW** of the **LAr Calorimeter** will **stay the same: only** the **electronics** will be **upgraded** and **this** is precisely the **topic** of this **talk.**



Timeline


LHC / HL-LHC Plan
HiLumi
LARGE HADRON COLLIDER
LHC
We're here and taking data!
HL-LHC
Data-taking resumes!
Run 1
Run 2
Run 3
Run 4 - 5...
LS1
EYETS
LS2
LS3
7 TeV
8 TeV
13 TeV
13.6 TeV
13.6 - 14 TeV
energy
splice consolidation
button collimators
R2E project
cryolimit
interaction
regions
Diodes Consolidation
LIU Installation
Civil Eng. P1-P5
pilot beam
inner triplet
radiation limit
Electronics installation...
HL-LHC
installation
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2041
experiment
beam pipes
ATLAS - CMS
upgrade phase 1
ALICE - LHCb
upgrade
ATLAS - CMS
HL upgrade
75% nominal Lumi
nominal Lumi
2 x nominal Lumi
2 x nominal Lumi
5 to 7.5
x nominal Lumi
30 fb-1
190 fb-1
500 fb-1
integrated
luminosity
3000 fb-1
4000 fb-1
HL-LHC TECHNICAL EQUIPMENT:
DESIGN STUDY
PROTOTYPES
CONSTRUCTION
INSTALLATION & COMM.
PHYSICS
HL-LHC CIVIL ENGINEERING:
DEFINITION
EXCAVATION
BUILDINGS
CORES

An overview of the LAr readout



Phase-II (HL-LCH)

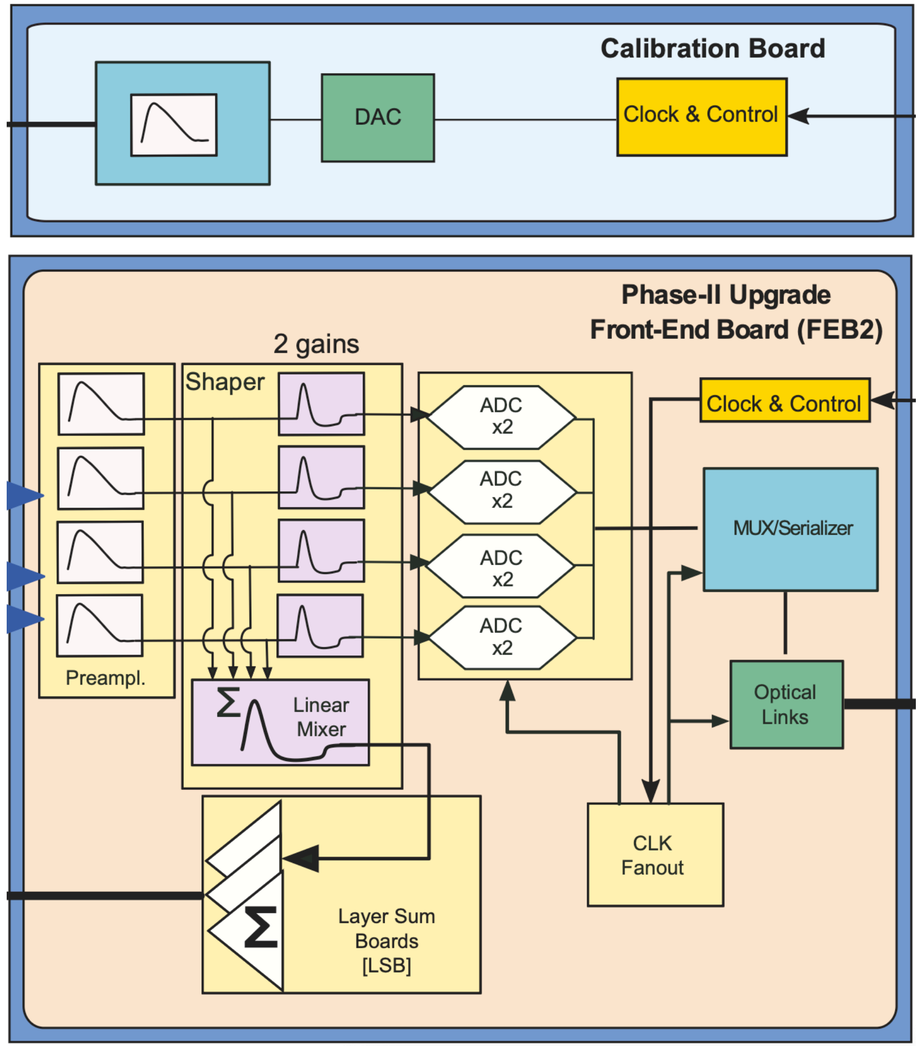
- Cover the **full energy range** in a single cell (~ 50 MeV electronic noise to 3 TeV).
- **16-bit** dynamic range with **11-bit** precision by leveraging **two** overlapping 14-bit **gain** scales.
- **Nonlinearity** below **0,1%** at ~ **300 GeV.**
- **Electronics noise lower** than the Minimum Ionising Particle (**MIP**) energy (the intrinsic LAr resolution).
- **Radiation tolerance** for the **full** HL-LHC **dose** which is largest at the barrel.

Phase-I (RUN 3)

- Digital trigger **installed** and commissioned in **2019-2022**.
- Already **leveraged** for **Run 3**.
- Part of **Phase-II L0 trigger** system.

On-Detector Electronics

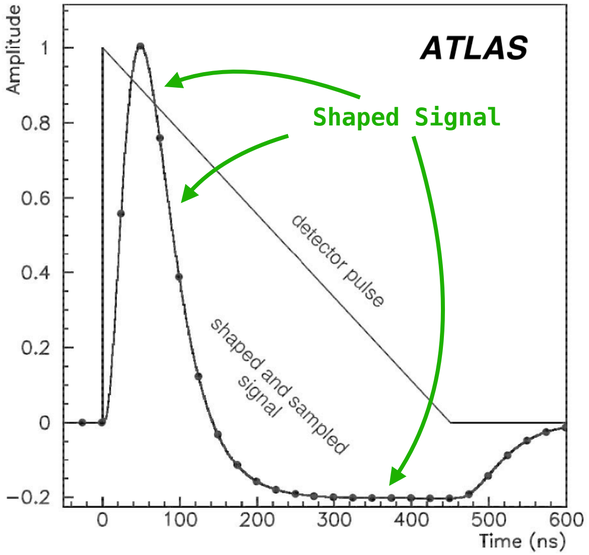
An overview of the On-Detector electronics



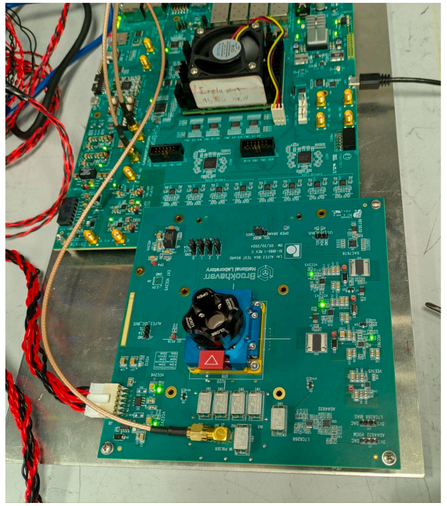
- **<u>Calibration</u>**:
  - Injects known LAr-like pulse at input.
  - Contains a pulser and a DAC.
- **<u>Front End Board (FEB) 2</u>**:
  - **Pre-Amplifier/Shaper** (PA/S)
    - **HEC**: **only** the **shaper**; the **amplifier** is in the **cryostat**.
  - **ADC**
  - **Layer Sum Boards** (LSB).
  - **Serialiser** chip (**lpGBT** in data mode).
- Readout includes **5** LAr-specific **ASICs**.

Pre-amplifiers and shapers

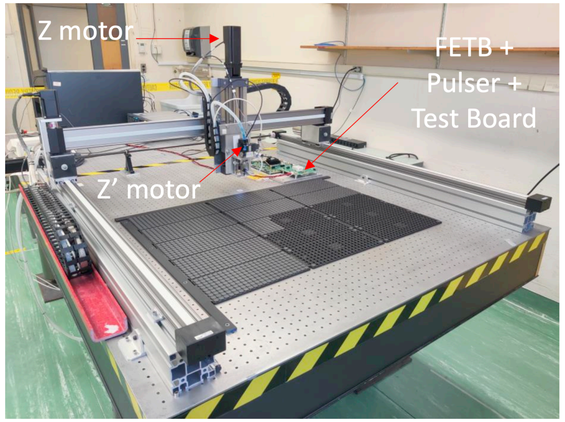
- **Analog processing** of signals:
  - **Amplification** and split into **2** (high and low) **gains**.
  - Leverage a **bipolar CR-(RC)^N shaping** function.
  - **Differential output** into **ADC** and **L0 trigger**.
- **<u>ASICS</u>**: **ALFE2** (EM & FCAL) and **HPS** (HEC).
  - Using **130 nm CMOS** technology.
- Have to **test 50k** chips: **automation** is needed!
  - Based on a **robotic setup**: 1 test ~ 20 s.
  - **Irradiation** tests **ongoing**.



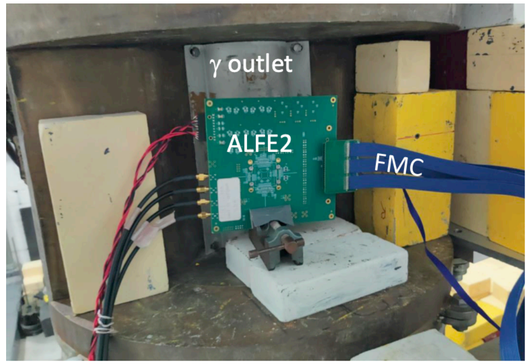
LAr Pulse & Shaped Signal



Production Test Board



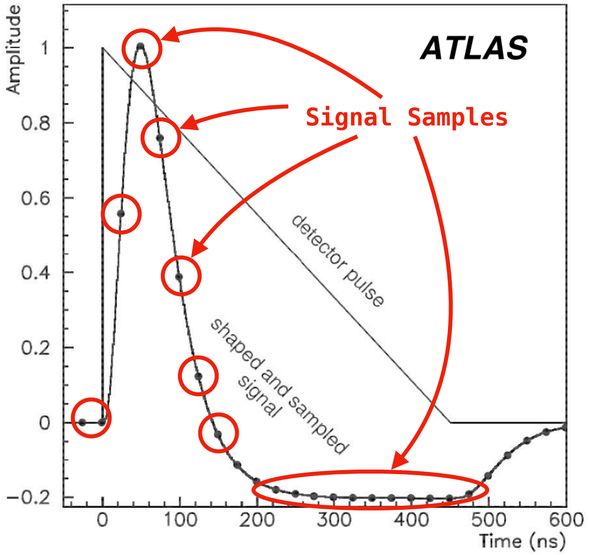
Robotic Test Setup



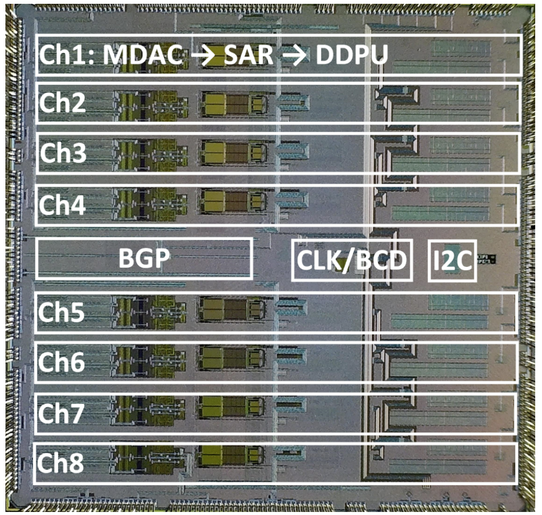
BNL's Irradiation Facility

ADC

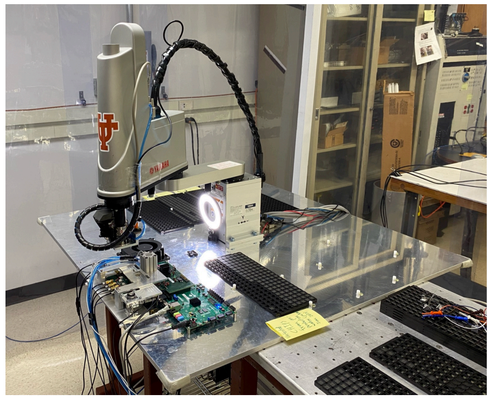
- **Digitisation** of PA/S outputs:
  - At **LHC** bunch crossing **rate** of **40 MHz**.
  - **14-bit** dynamic **range** and **11+** bit **precision**.
- **<u>ASIC</u>: COLUTA**
  - Using **65 nm CMOS** technology.
  - **15-bit** output @ **40 MHz**.
- Have to **test 50k** chips: **automation** is needed!
  - Based on a **robotic setup**: 1 test ~ 20 s.
  - **Irradiation**, **vibration** & **thermal** tests **done**.
  - Mass **production** started in **2025**.



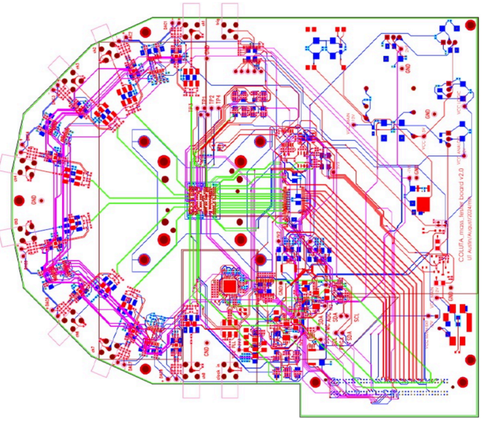
LAr Pulse & Shaped Signal



Closeup of a COLUTA



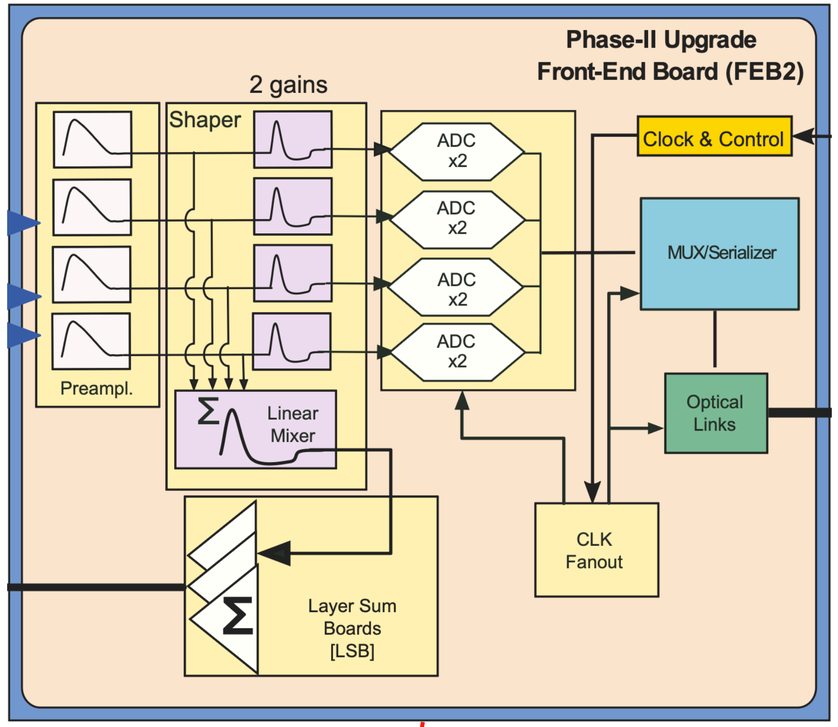
Robotic Test Bench

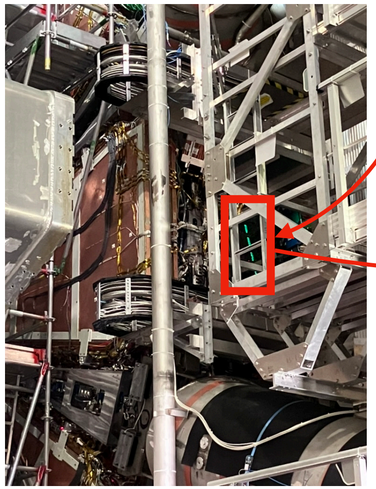


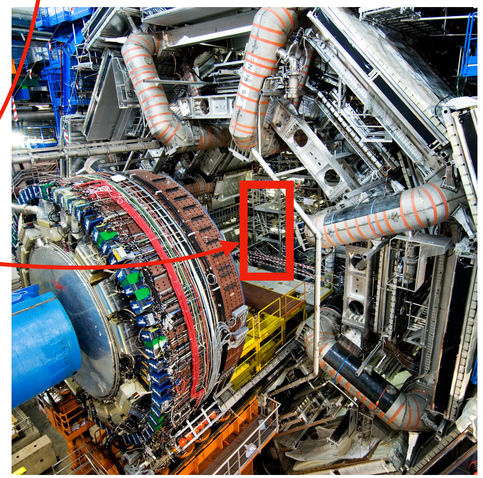
Production Test Board

Front End Board 2

- Key **FEB 2 specifications**:
  - **Readout** of **128** calorimeter **channels** with **2 gains** at **40 MHz**:
    - **LAr** will **need** a total **1524 FEB2s**!
  - **Low coherent noise** per channel (less than 5% of the total noise per channel) and **low crosstalk** (less than 1%).
  - For **large pulses**:
    - **Energy** resolution: $\sigma(E)/E < 0.25\,\%$
    - **Time** resolution: under 100 ps.
  - **Optical data**, **clock** control and **monitoring** links using Versatile Link (VL)+ (**lpGBT** & **VTRX+**) devices.
  - **Power** consumption under **128 W** per board.
  - **On-board power** provided by a single **48 V input**.



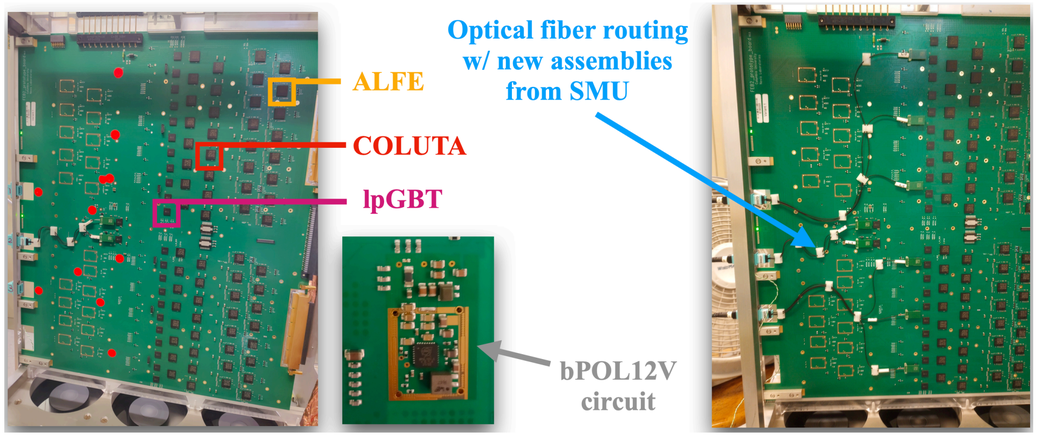




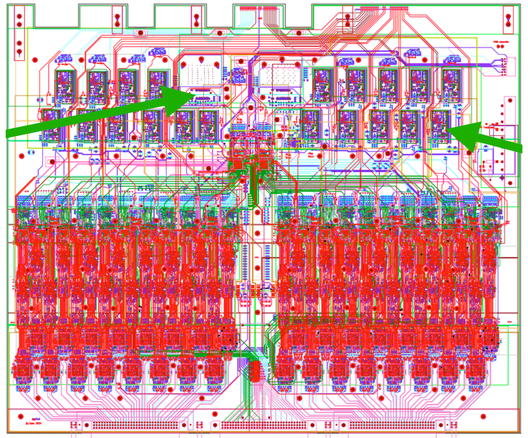
FECs with FEB boards currently in the detector

The FEB2 prototype

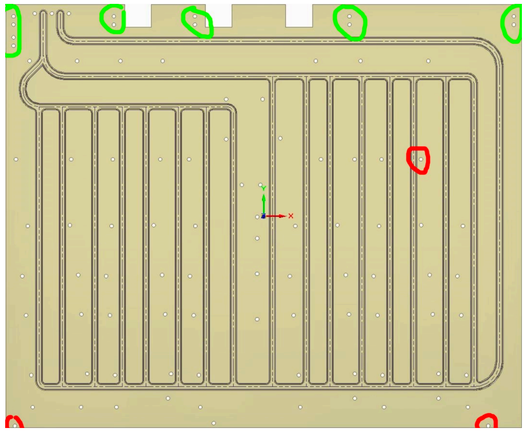
- **Last manufactured iteration** of the design.
- Will **use** the **updated lpGBTv2** chips.
- A **noise issue** has been observed: **addressed** in the **FEB2 v2.6**.
- **Produced** and tested **10** FEB2 v2.5 **boards**:
  - **Including** power bus **noise mitigation**.
  - **Distributed** across **several institutes** for **testing/integration.**
- Operating **temperature** is a **critical factor**.
- **Water-based** cooling for **heat** dissipation.



FEB2 v2.5 with outlined components

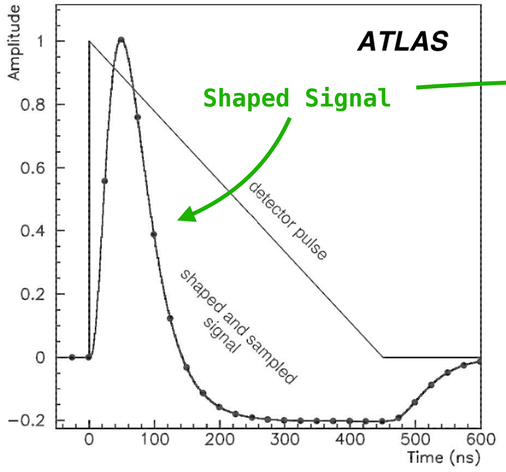


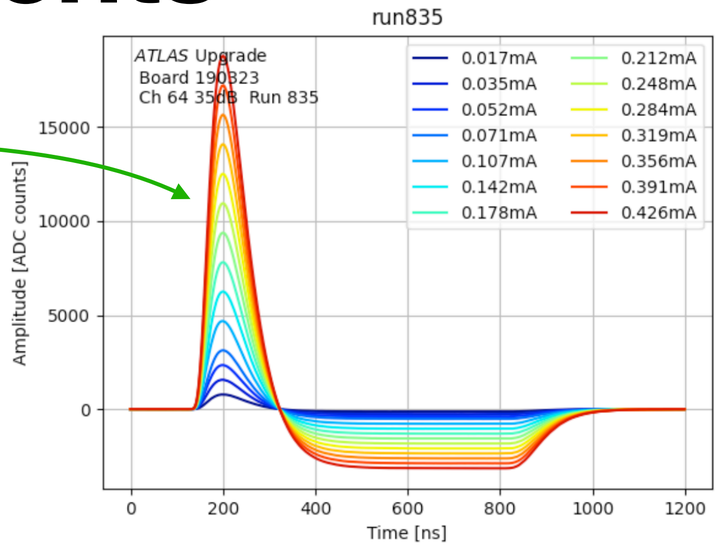
FEB2 v2.5 Prototype



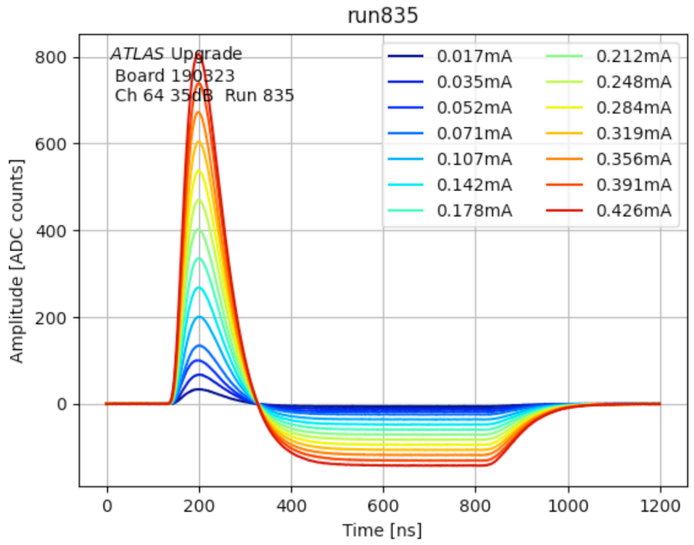
FEB2 Cooling Plate

FEB2 measurements



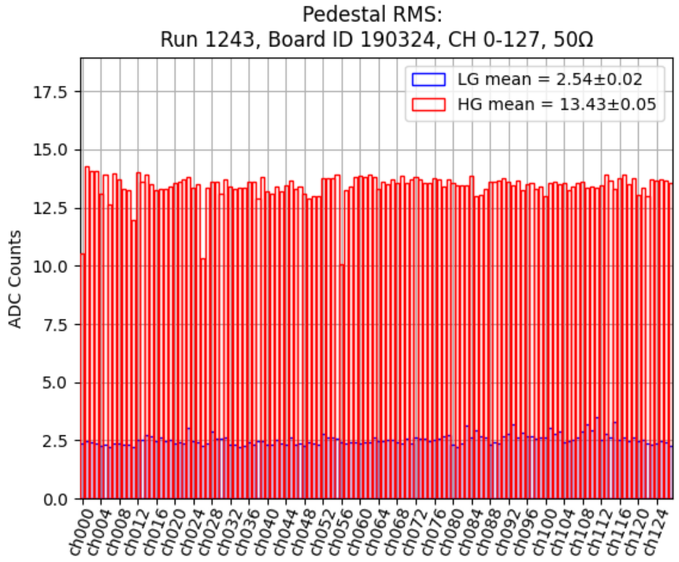


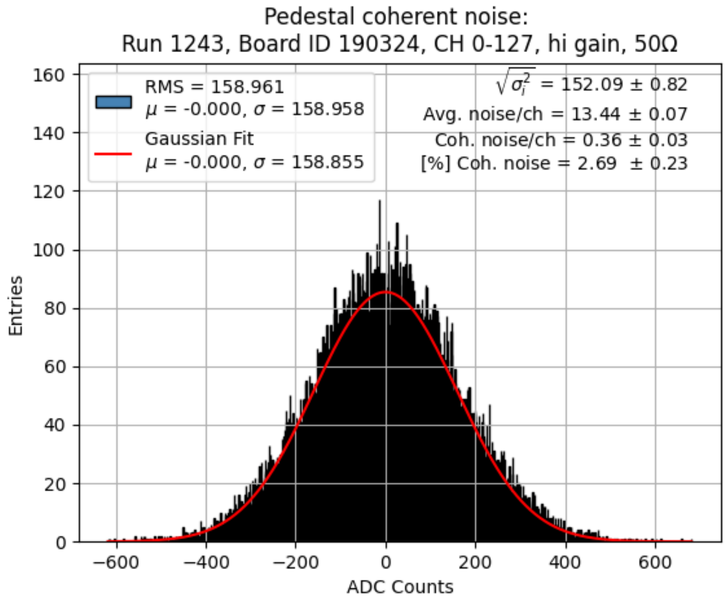
High Gain, Channel 64, 35 dB attenuator



Low Gain, Channel 64, 35 dB attenuator

Average high gain noise per channel of 13.4 ADC counts

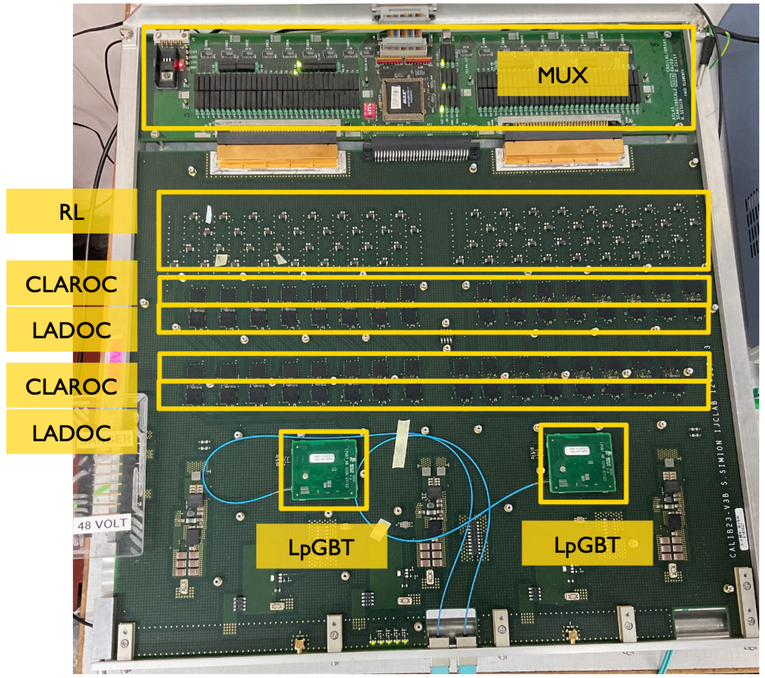




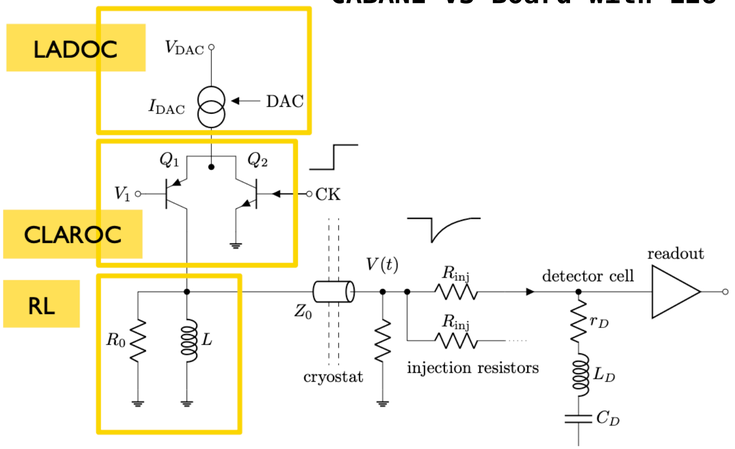
Coherent noise per channel of 2.7%

CABANE calibration board

- **Injects** LAr-like **pulses** with known amplitude:
  - Allows **calibrating** the **readout** and **gain** scale.
- **Need** to **calibrate 180 k** calorimeter **cells**:
  - We'll install **122** calibration **boards**.
- **<u>ASICs</u>**:
  - **CLAROC**: pulse generator with 180 nm XFAB technology.
  - **LADOC**: 16-bit DAC with 130 nm CMOS technology and sub 0.1% non-linearity.
- **ASICs passed irradiation** tests.
- **Production** for the **122** boards **starting** now.



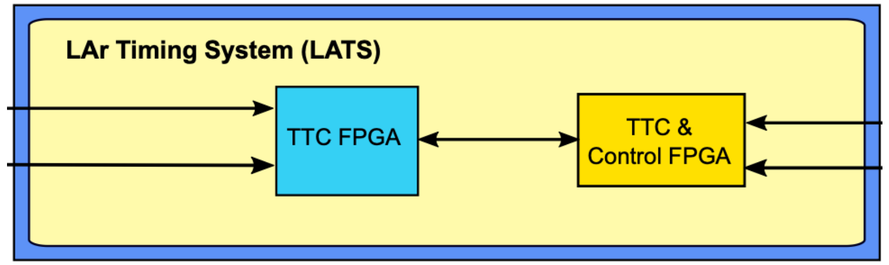
CABANE v3 Board with 128 Channels

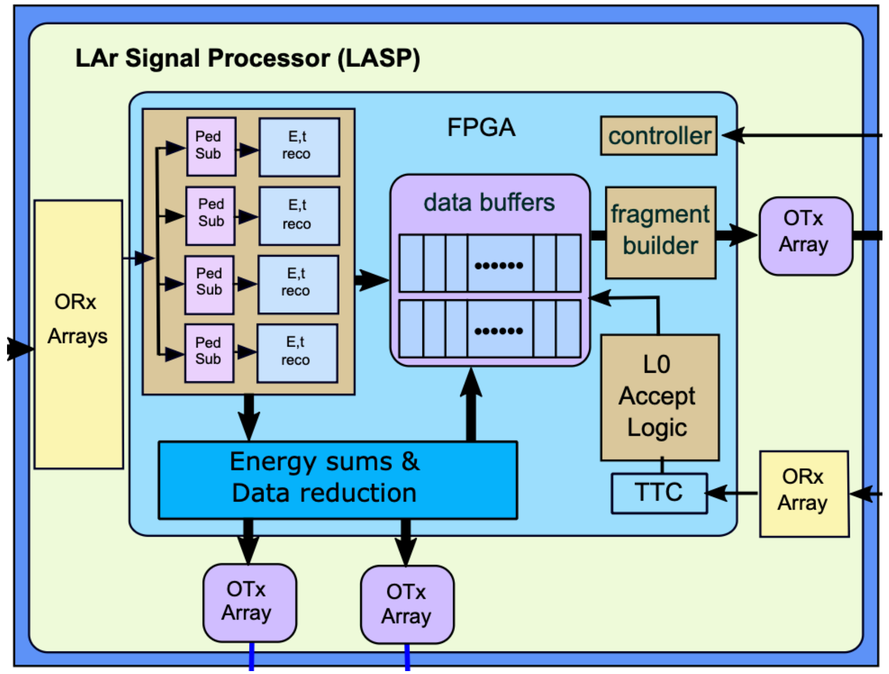


Simplified pulsing principle schematics

Off-Detector Electronics

An overview of the Off-Detector electronics





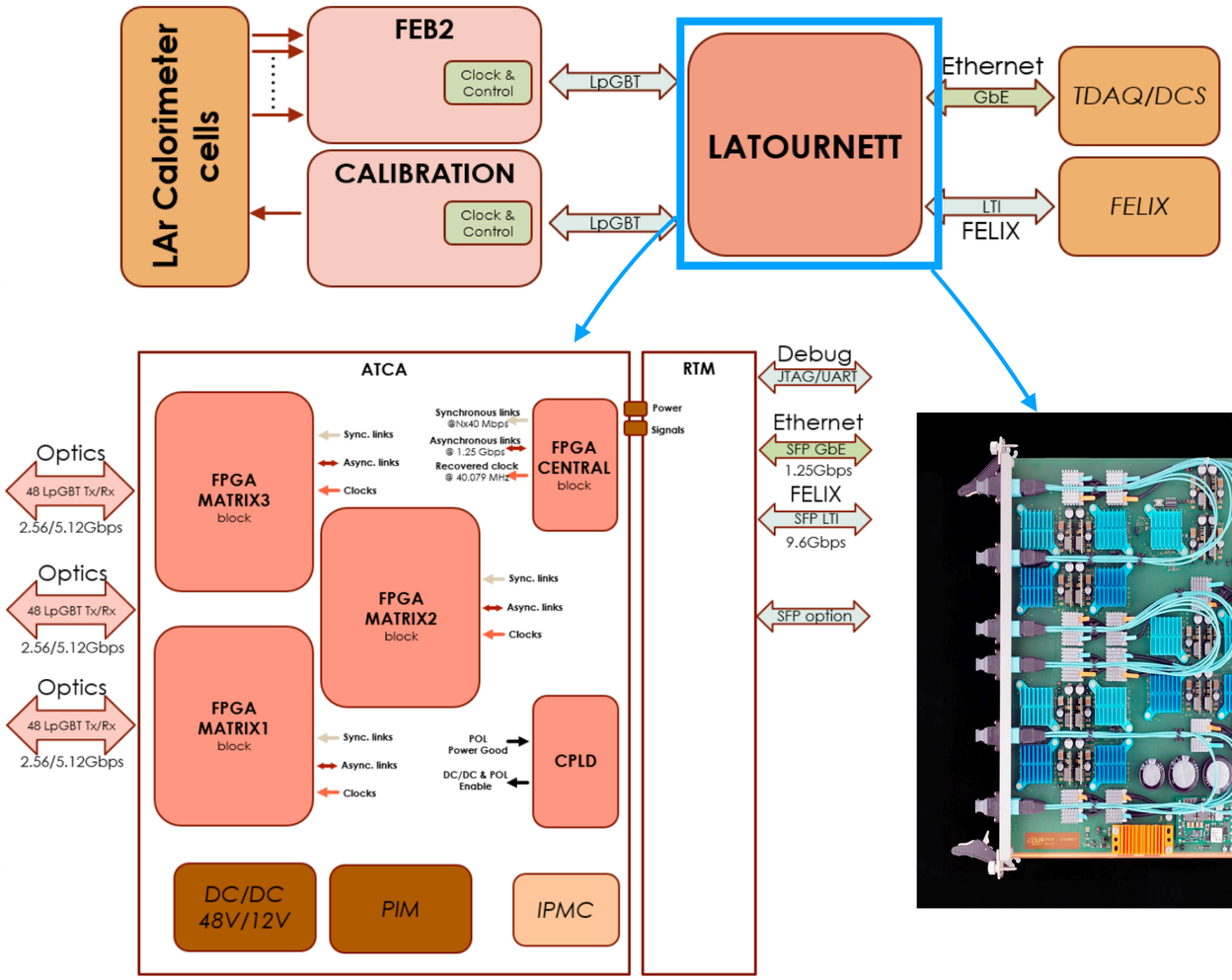
- **<u>Timing System</u>**:
  - Manages **clock**, **control** and **monitoring**.
  - Consists of **6600 fibres**!
- **<u>Signal Processing:</u>**
  - **Readout** of **345 Tbps** from **frontend**.
  - Consists of **+33000** 10 Gbps **links**!
  - **Compute energy** and **time** for each LAr cell.

LAr Timing System

- **Trigger, Timing and Control** (TTC) distribution, **configuration** and **monitoring**.
- Based on the **lpGBT** protocol.
- **Core** component: **LATOURNETT**:
  - **Distributes LHC clock** (40 MHz), Bunch Crossing Reset (**BCR**), **calibration commands** and **monitoring**.
  - **Configures FEB2** and **CABANE**:
    - Up to **72** On-Detector **boards** controlled **per LATOURNETT**.
    - A total of **30 LATOURNETT** boards.
  - Each **board** contains **13 Cyclone 10 GX** FPGAs, a **MAX 10** FPGA and a **CERN IPMC**.
  - **Leverages** a **passive Rear Transition Module** (RTM).

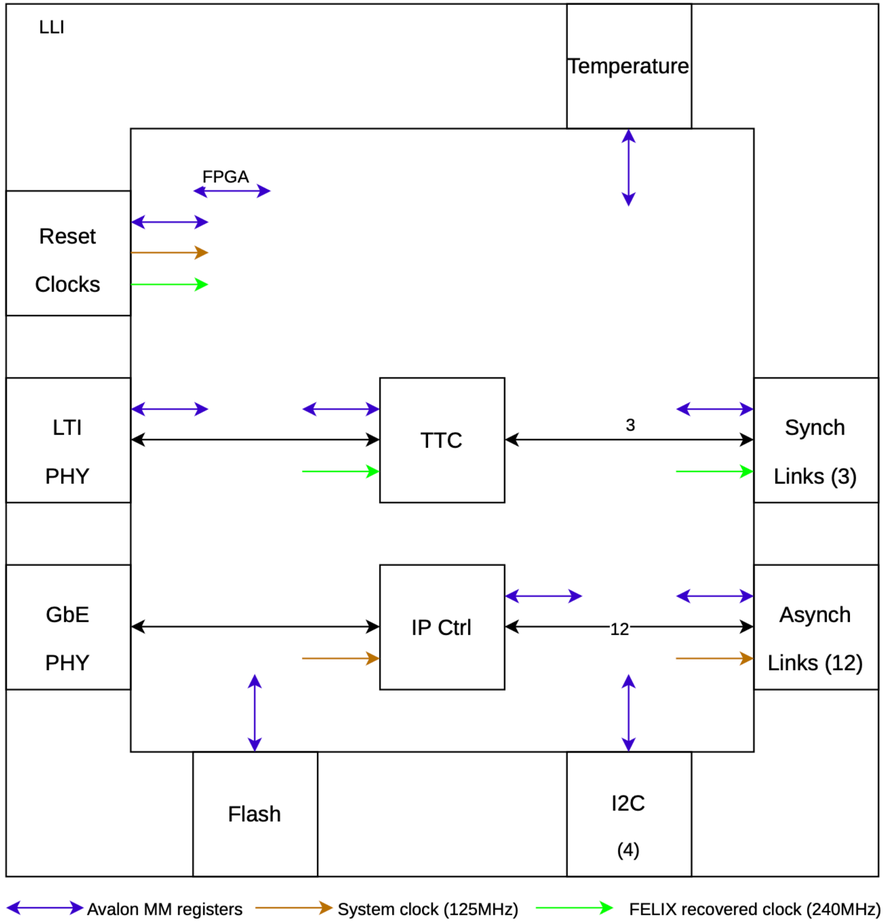
The 'real' La Tournette

Proposed Architecture

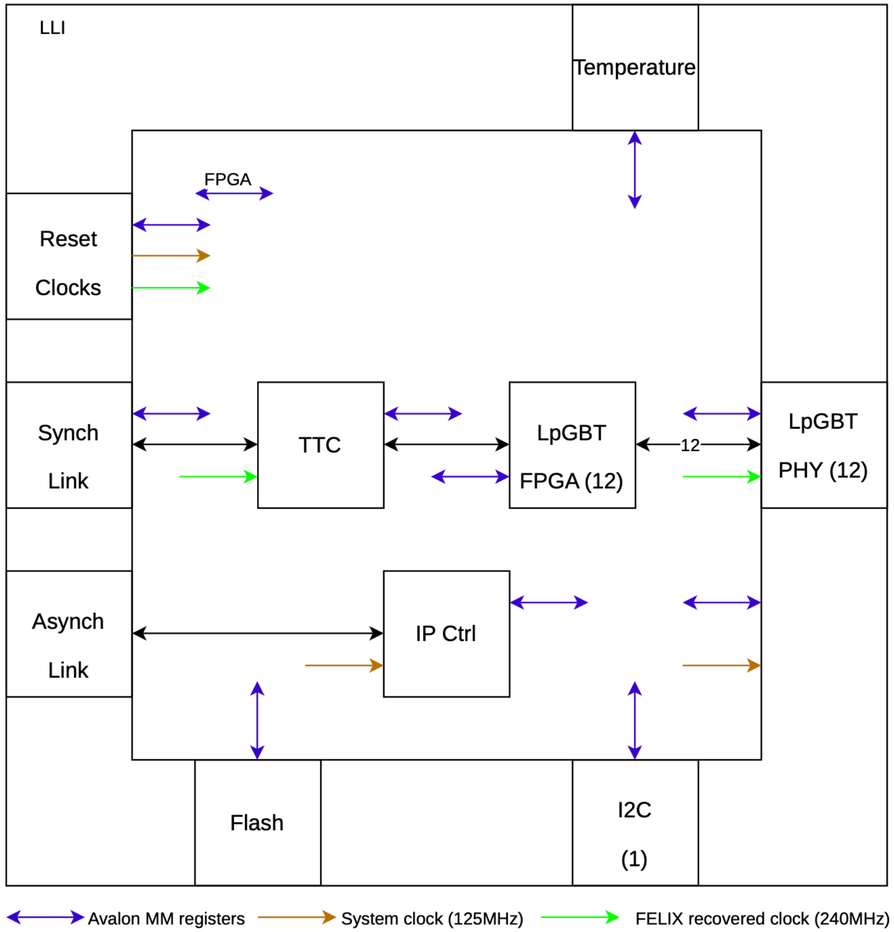


LATOURNETT firmware

Central FPGA



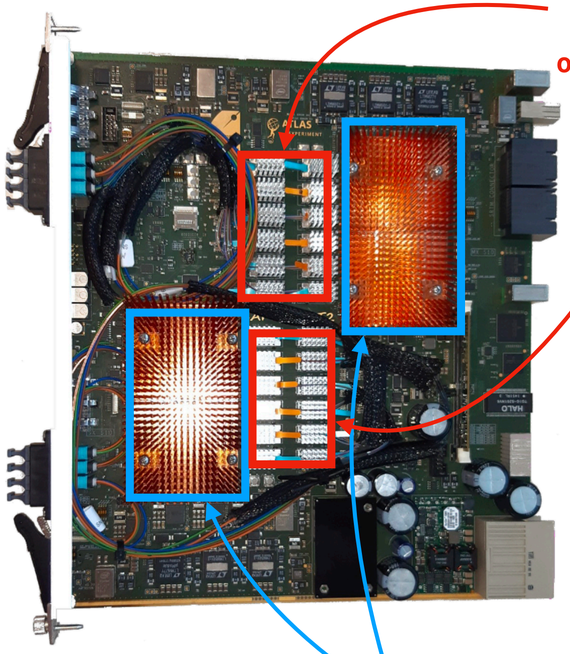
Matrix FPGA



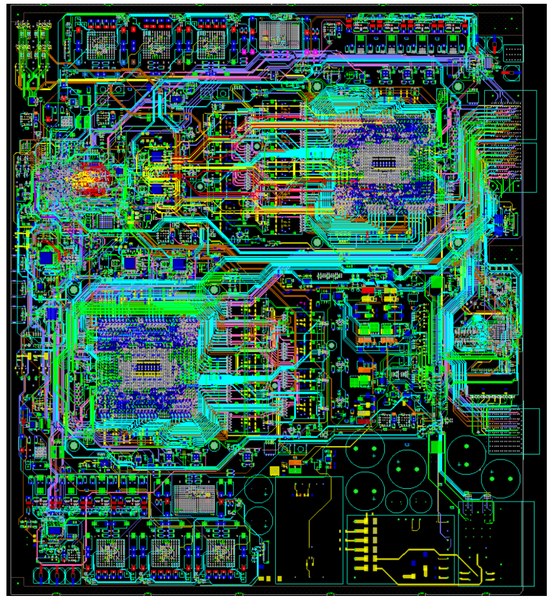
Development efforts have been instrumental in advancing the integration of system components. The current state of the firmware has allowed us to leverage a FELIX board together with a LATOURNETT devkit, a CASA calibration board, a FEB2 and a LASP to read out data at the Electronics Maintenance Facility at CERN.

Liquid Argon Signal Processor

- Applies **digital filtering** to **FEB2** data and:
  - **Computes time** and **energy** on each **BC**.
  - **Sends** it to Data Acquisition (**DAQ**) and **trigger**.
- **Hardware**:
  - **LASP** ATCA **blade**:
    - **278** boards in total.
    - **2** Intel **Agilex 7 FPGAs** per blade.
    - **3 FEB2s** per **FPGA**.
  - **Smart RTM** (sRTM):
    - **TTC input** and **25 Gbps** data **output**.



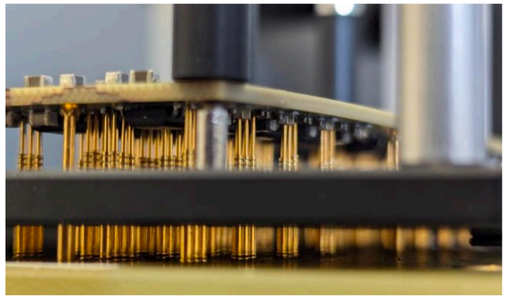
The LASP Test Board. It uses Intel Stratix 10 FPGAs and 6 boards are at different institutions for testing and integration work.



Routing Status on the LASP prototype board.

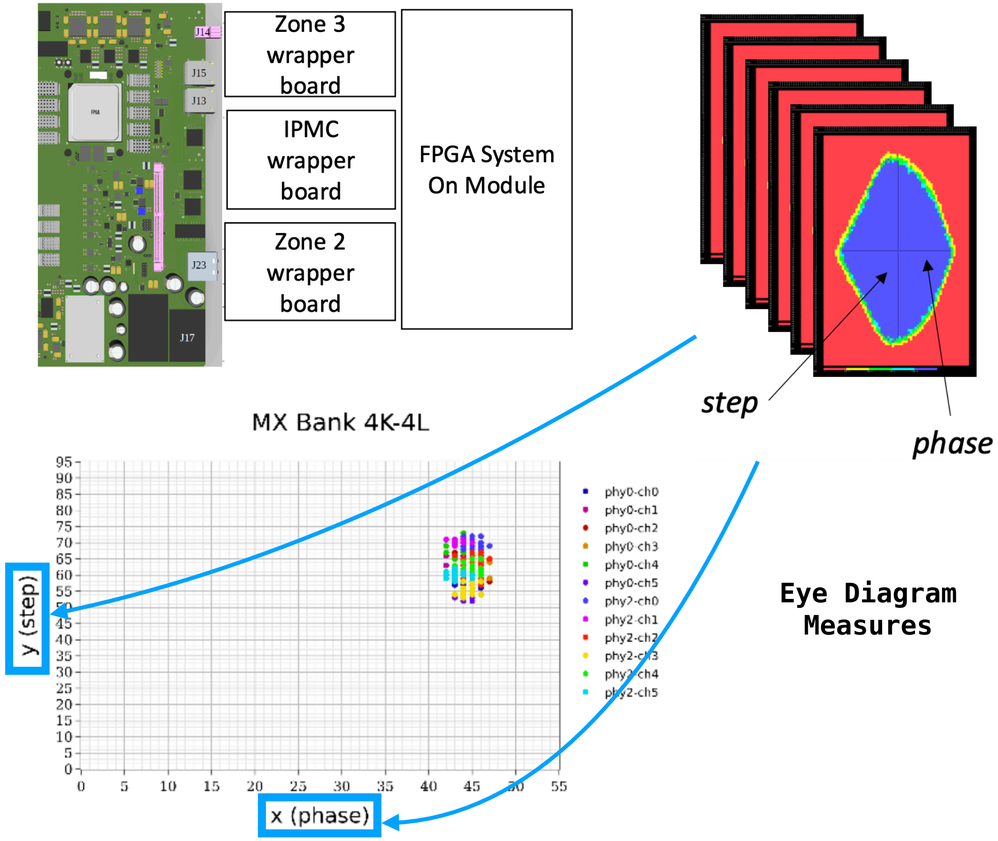
LASP test bench

- **Verify** both **HW** and **FW** operate as expected.
- **Aimed** at testing **mass-produced boards**.
- Planning **setup** allowing **testing** of specs with:
  - An **Agilex 7 DevKit**, FPGA Mezzanine Cards+ (**FMC+**) and a **FELIX** for **data I/O** and **checking**.
  - Use of an **INGUN** interface for accessing all the test points.
  - **JTAG** tests based on **XJTAG**.
  - Use of **wrapper boards** for accessing **backplane** connectors.
  - **Eye diagrams** look **good** and are **stable**.
- Plan to **exercise test bench** with first available **LASP Prototypes**.



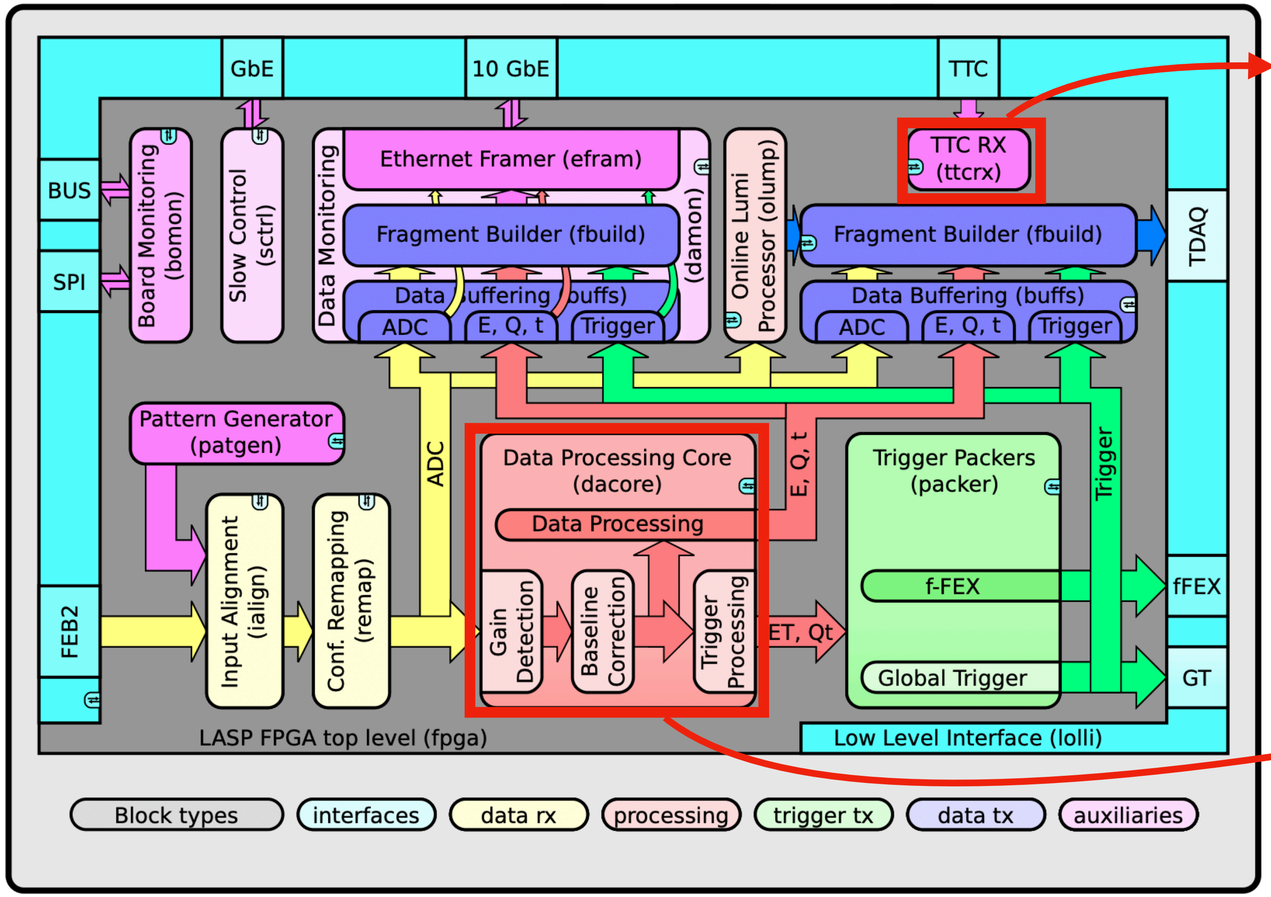
INGUN Connector

XJTAG setup with the LASP T2



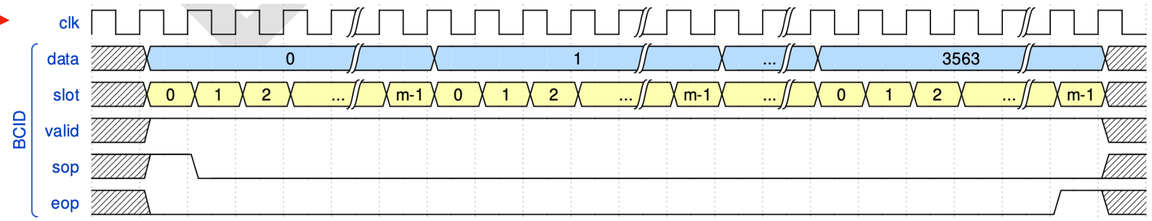
Eye Diagram Measures

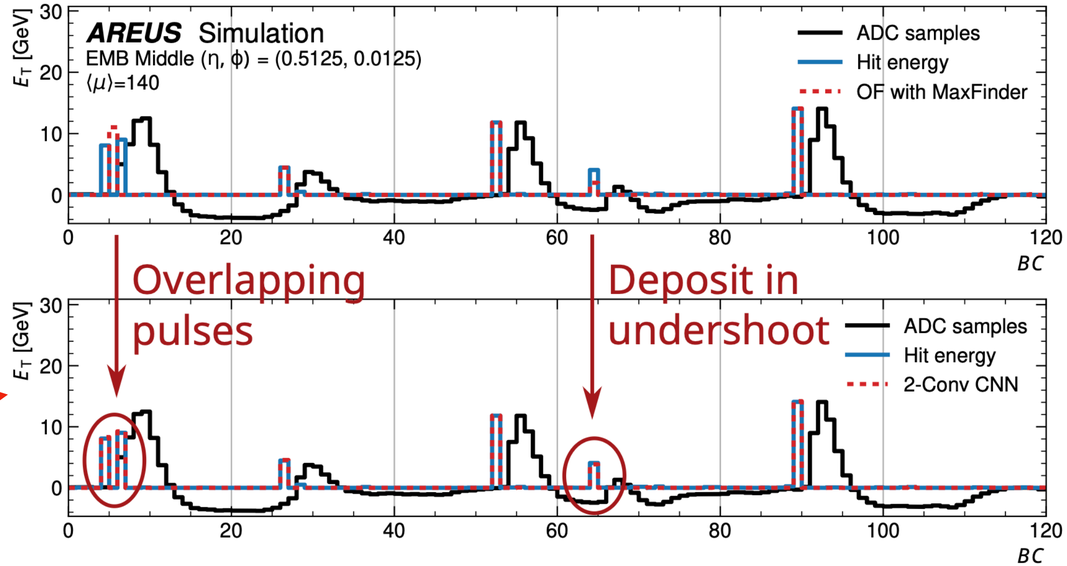
LASP firmware



Architecture of the LASP Firmware for a single FPGA

Bunch Crossing (BC) Identifier within the FW. The CLK runs at 320 MHz, 8 times faster than the 40 MHZ LHC clock. The End Of Packet (EOP) signal is the BCR sent by the Central Trigger Processor (CTP).



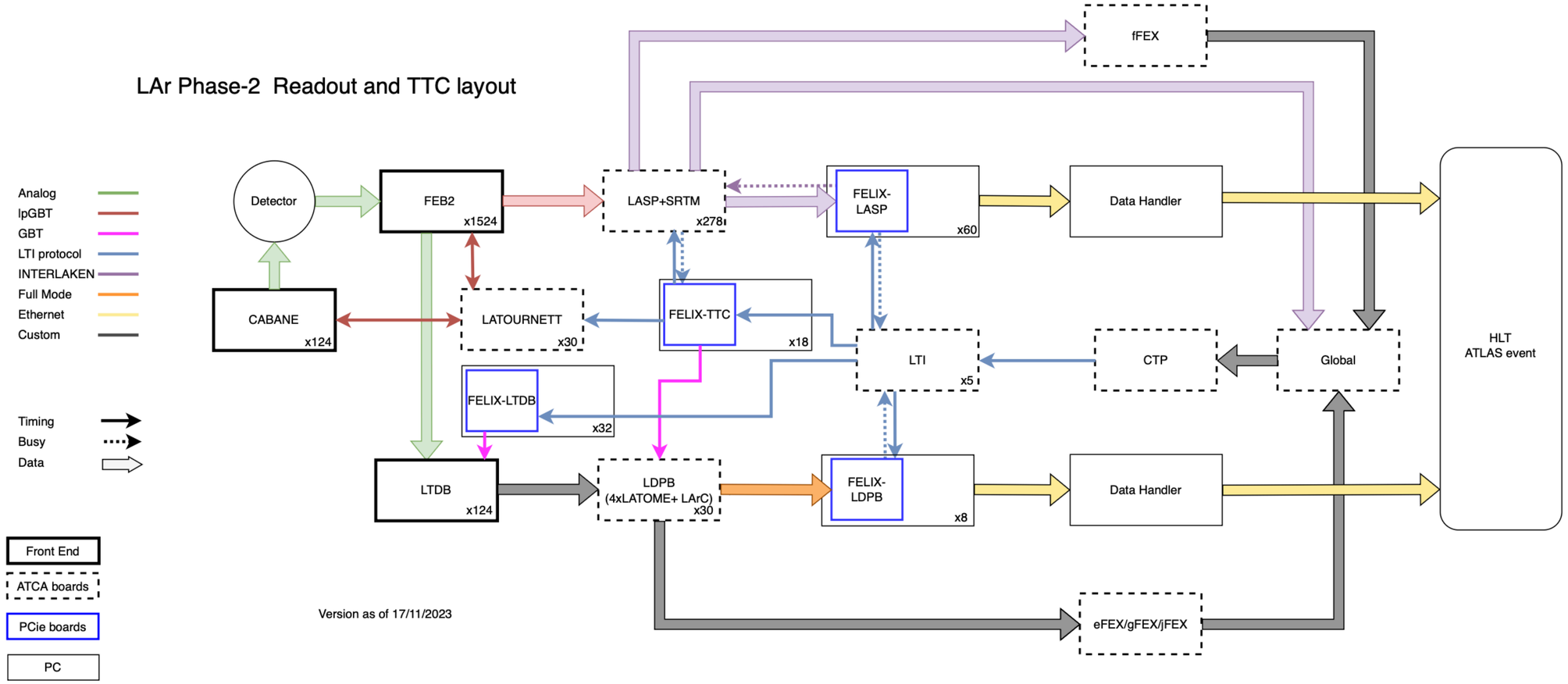


Comparison of energy reconstruction with the current Optimal Filtering Algorithm and a 2-layer Convolutional Neural Network (CNN).

Integration

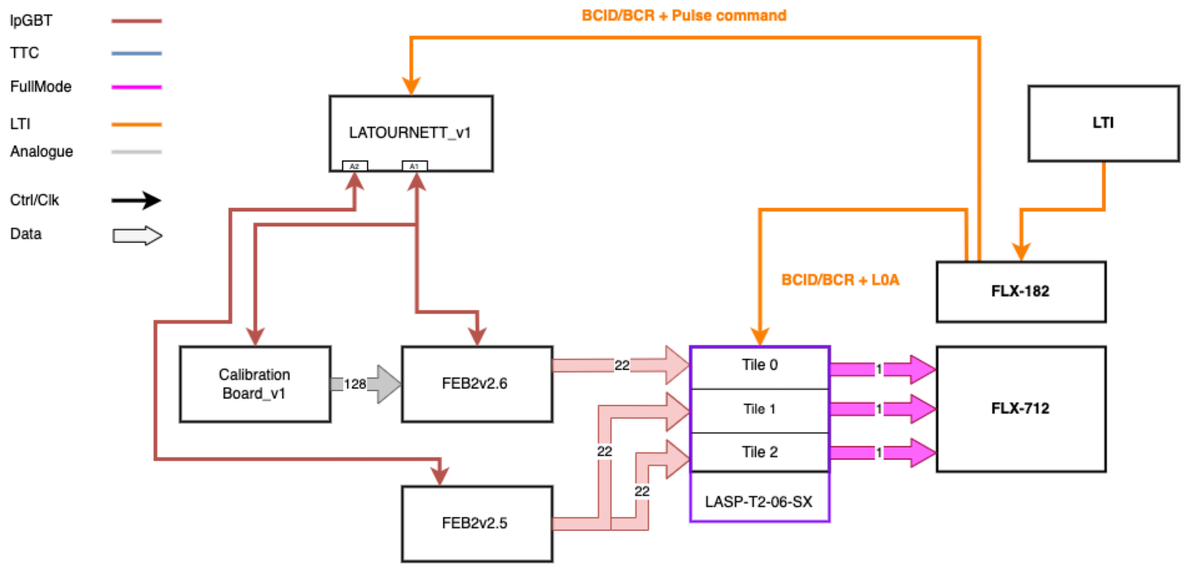
LAr as a system

- **Components** might **work** in **isolation**… but **integration** is **crucial** within **LAr** and **ATLAS**.
- **Integration** is **key** for **insights** into **installation** and **commissioning** and **full-chain tests.**



The Electronics Maintenance Facility (EMF)

- **EMF** (CERN) houses a **'small scale' setup**:
  - **Data** can be **acquired** from a **FEB2** and **stored** for offline **analysis**.
  - It contains **all** the needed **HW functionality**.
- The **testbed** has greatly **helped development** and **integration**:
  - **<u>Online Software</u>**: OPCUA, FW Control, DCS.
  - **<u>Offline Software</u>**: Reconstruction and analysis.
  - **<u>Integration</u>**: GBT, lpGBT, FULLMODE, LTI…



Current setup at EMF

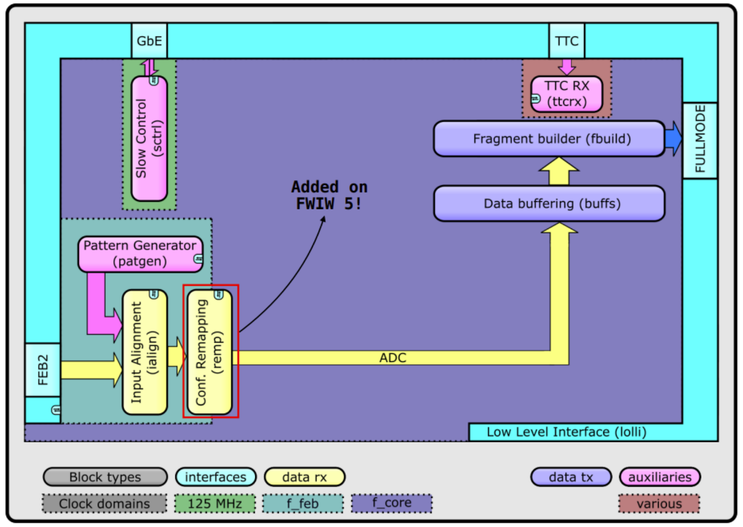
Firmware and Integration Weeks

- **Dedicated weeks** for:
  - **Pushing** firmware **development**.
  - **Integrating prototypes** and test **boards**.
  - **Building** a **team** spirit.
- Held at **CERN** and **Brookhaven** (BNL).
- **Since** their **inception** we:
  - **Scaled** the **FW** to read **3 FEB2s per** Stratix 10 **FPGA**.
  - **Added support** for the **LTI** protocol.
  - **Increased** the **FW's robustness**.
  - **Optimised** the **data-taking procedure** and FW **operation**.

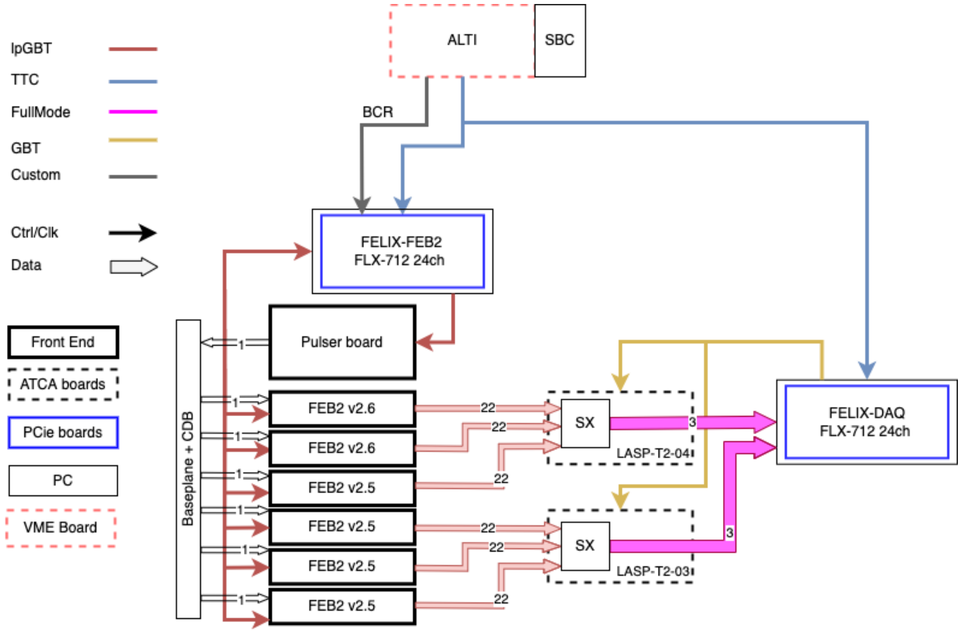
Part of the team working at BNL during FWIW 7

The Half Crate Test I

- The **FWIW**'s initial **milestone** was the **Half Crate Test** (HCT):
  - **<u>Objective</u>**: **reading** out **14 FEB2**s installed in a Front-End Crate (FEC) **simultaneously**.
- In the **last week** of **October 2025** we **read** out **6 FEB2s**.
- The **HCT** really **pushed** the **LASP FW development** effort **forward**!
- We **expect** to have **14 FEB2s ready** by **early 2026**.
- The desired performance **measurements** are **expected** by **March 2026**.
- We're **on schedule**!



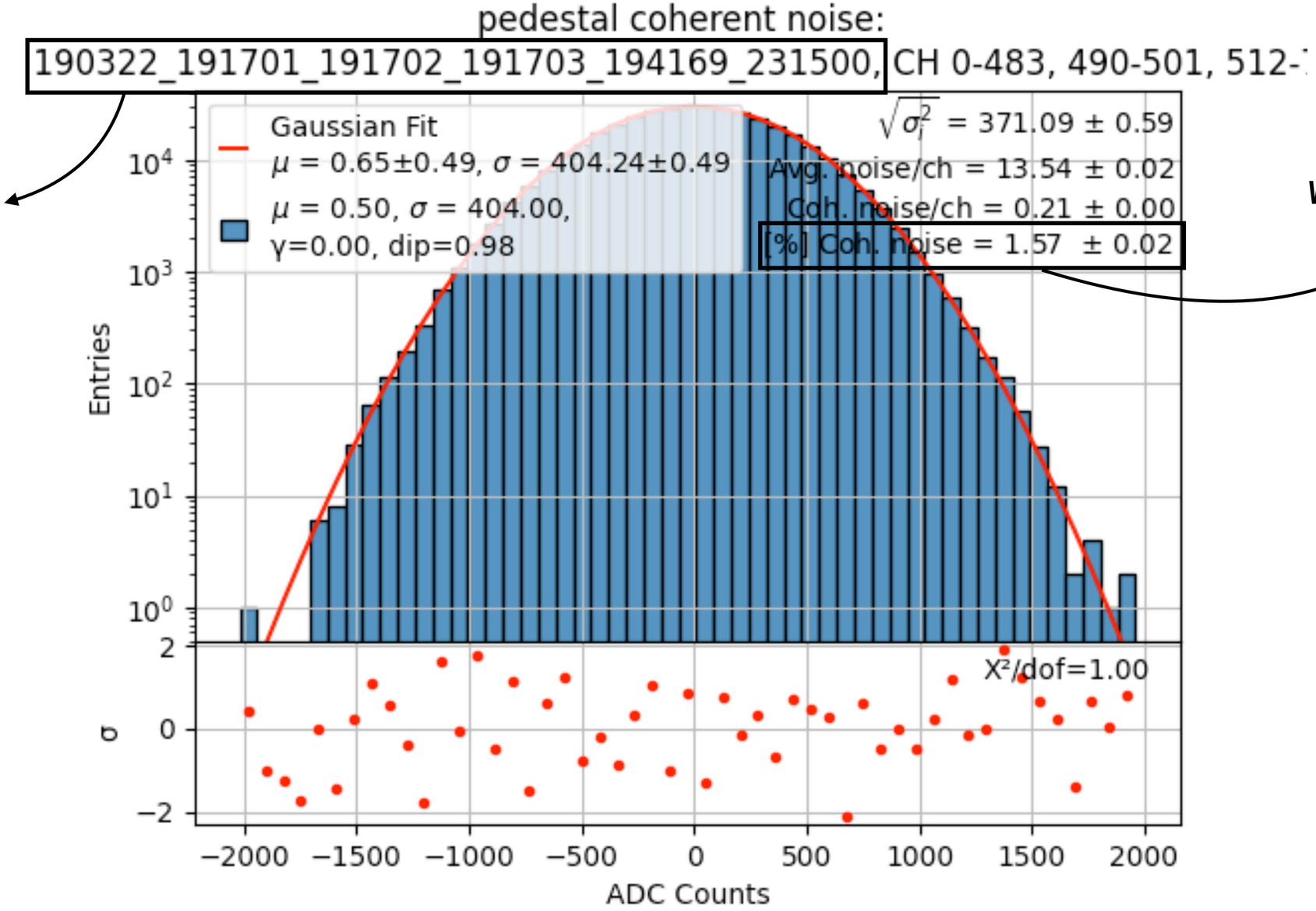
The Half Crate Test Firmware



Setup achieved at the end of October 2025

The Half Crate Test II

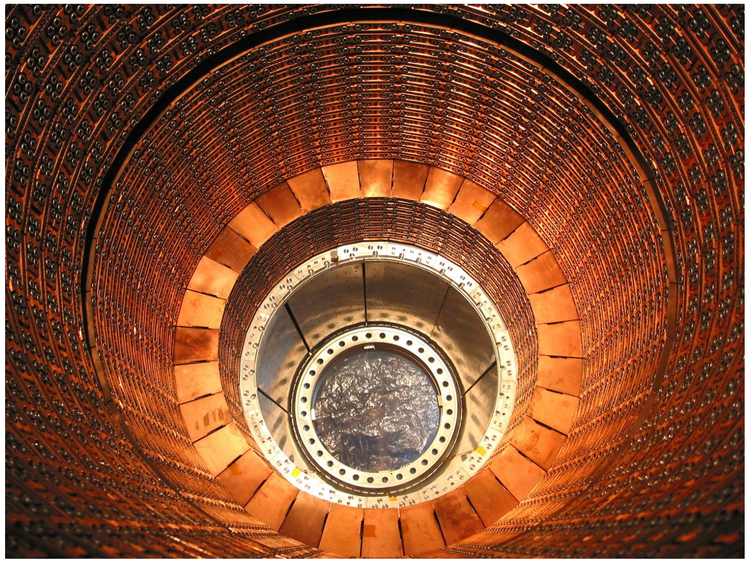
6 FEB2s
(755 channels)



Well below the target 5%!

Summing up

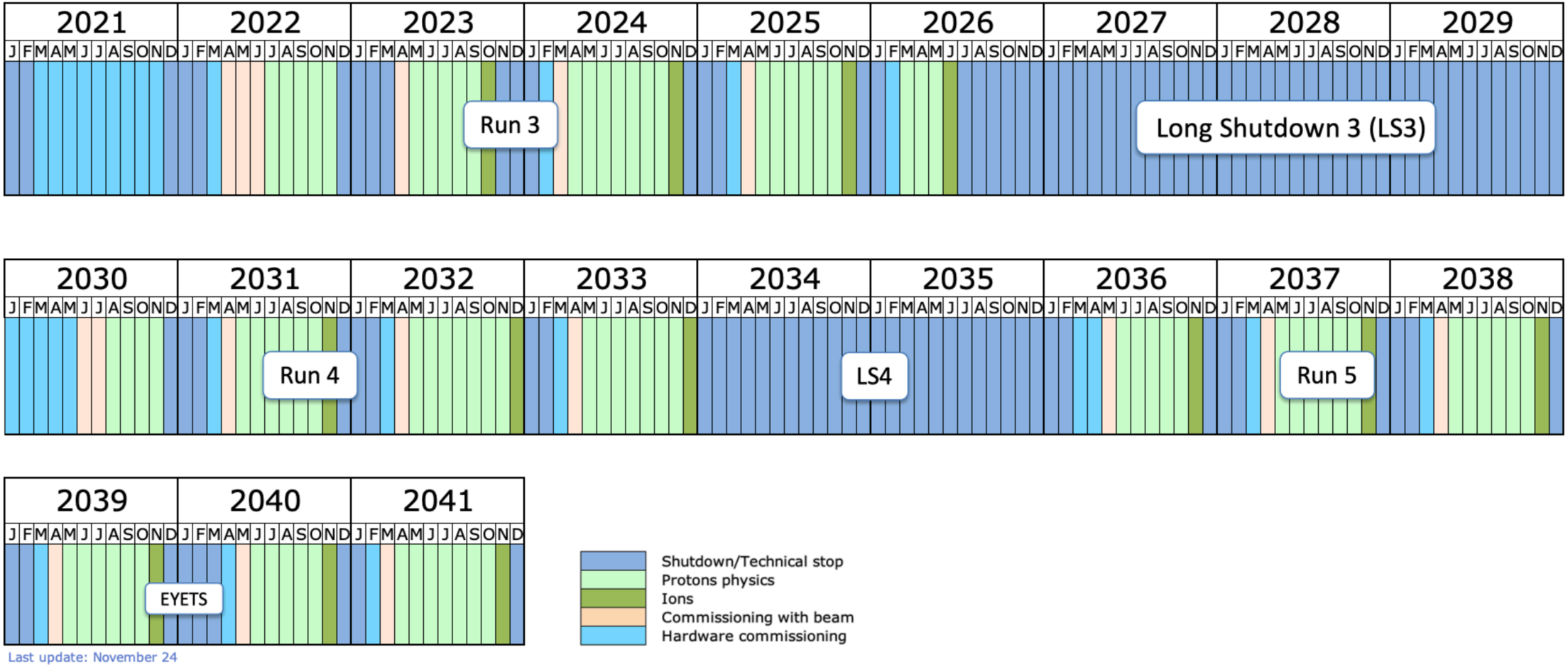
- The **LAr calorimeter** is **vital** for the **success** of **ATLAS** in the **HL-LHC**:
  - **Most** of the **precission** LAr **electronics** (on/off detector) will be **replaced** by **2030** in time of the HL-LHC (except part of HEC).
  - The **new electronics** should **last** until **2041**.
- The **HL-LHC upgrade** for **LAr** is **progressing nicely**:
  - **Custom** LAr-specific **ASICs** in **production**.
  - On/off detector **prototype boards** becoming **available** and being **tested**.
  - **Integration will** be (and already **is**) a **crucial activity** in the **context** of **LAr** and **ATLAS**.
- All in all, we are **on schedule** for the **installation** in the cavern **beginning** in **2027** at the **end** of **LHC Run 3**.



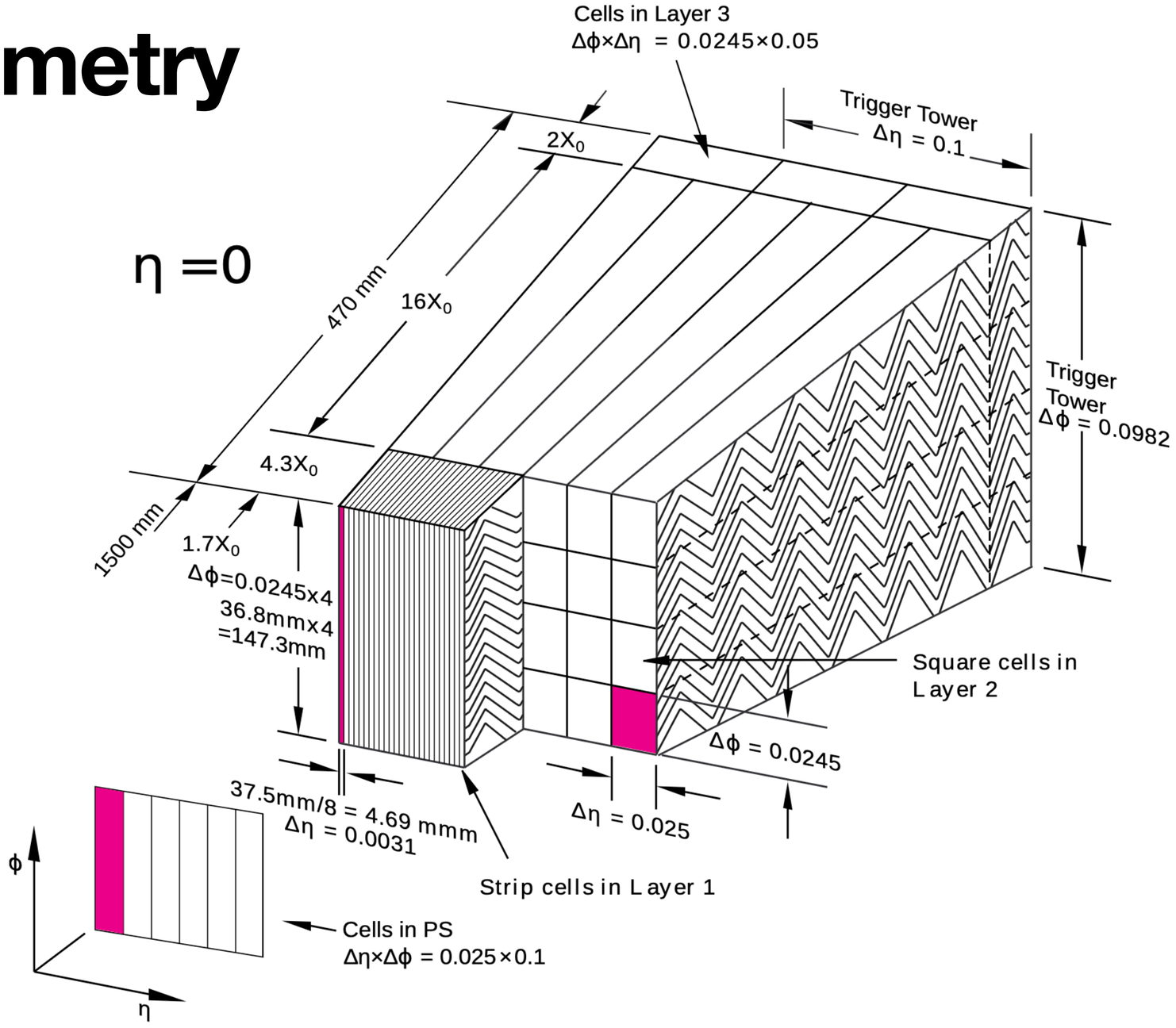
Any questions?

Backup Slides

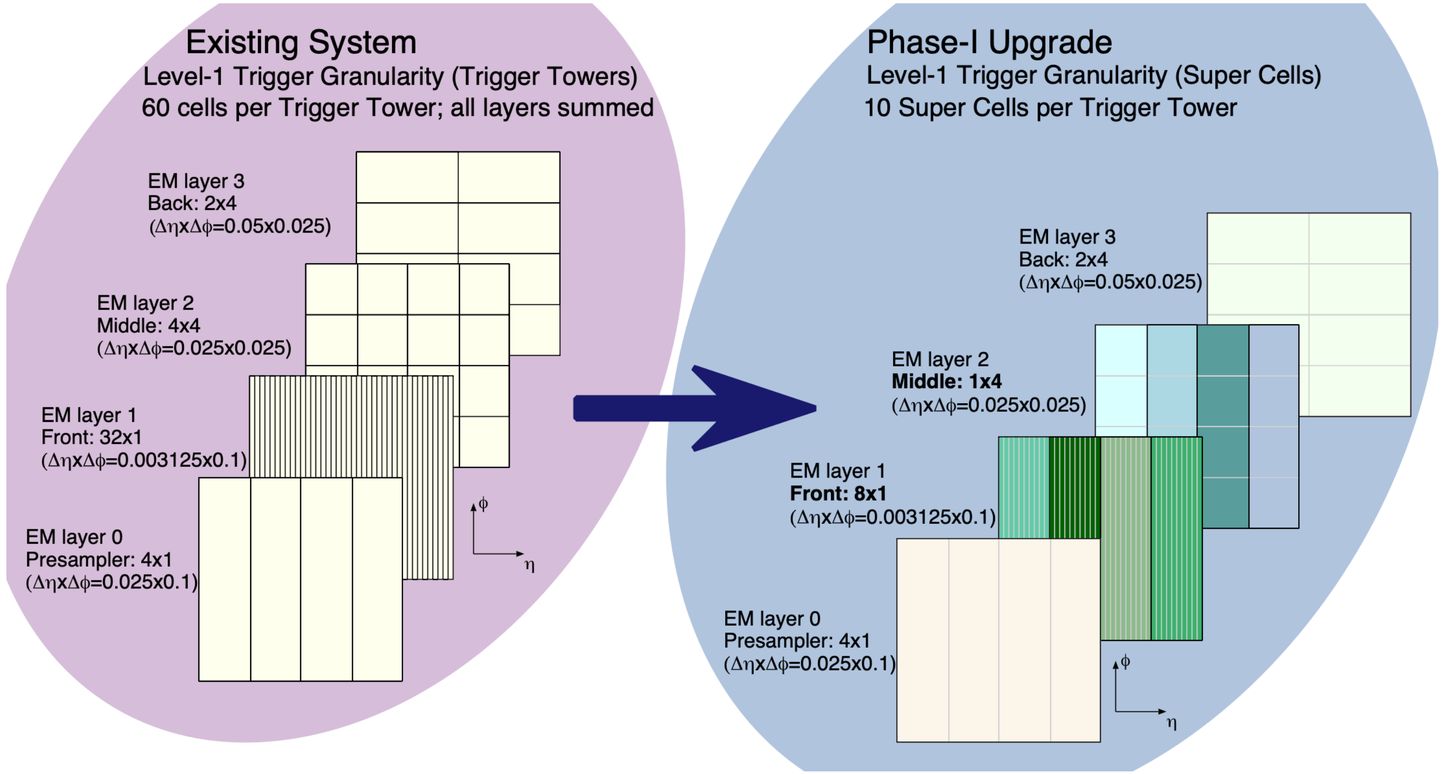
Long term LHC schedule

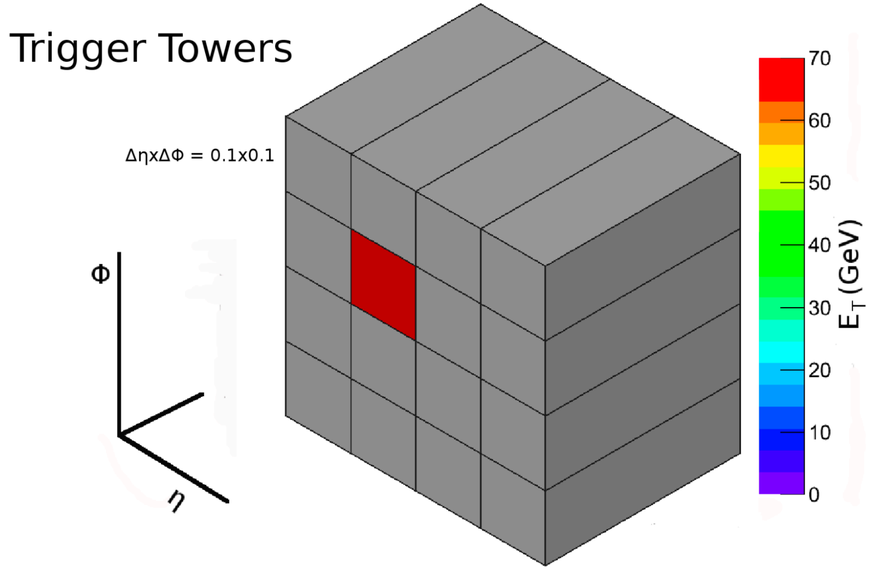


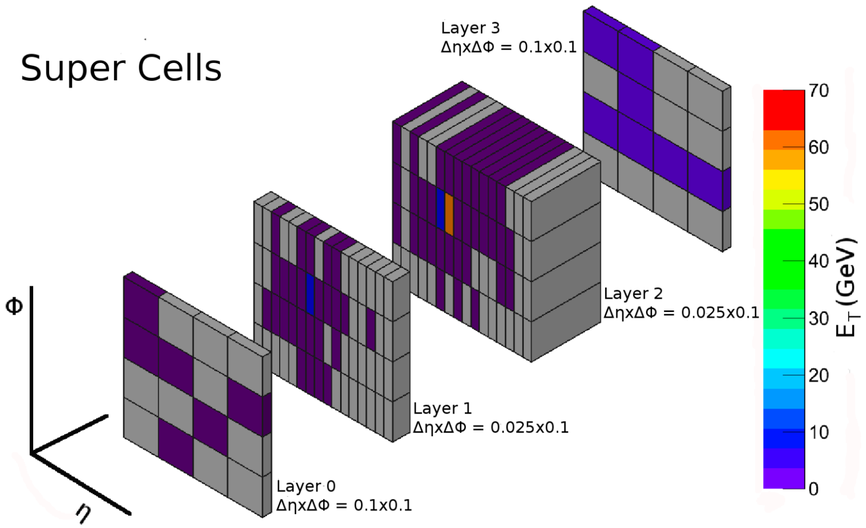
LAr geometry



Phase-I trigger granularity upgrade



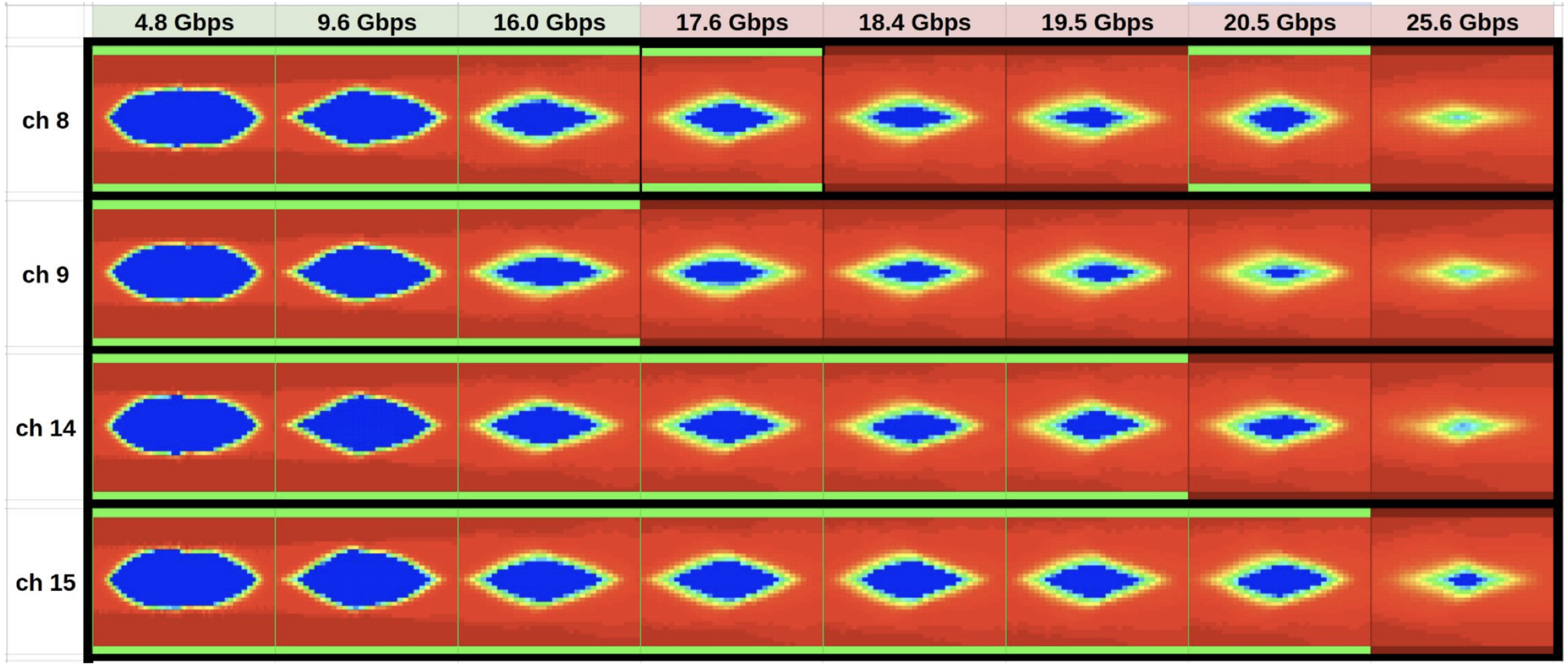




LASP-sRTM to TDAQ

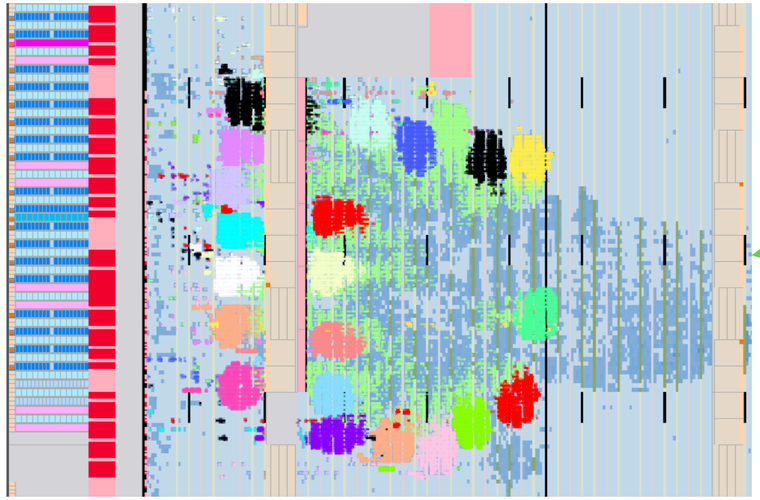
TDAQ AG2

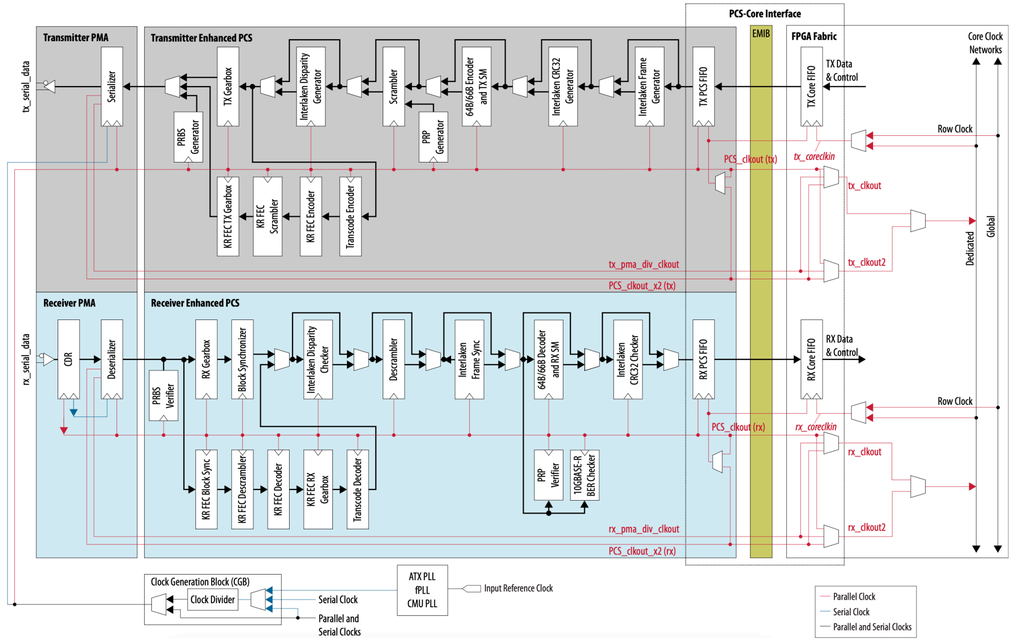
TDAQ AG1



LASP 44-link HCT FW on chip

Closeup of
lPGBT logic for
22 FEB2 links





Stratix 10
Transceiver PCS
data path diagram