Monolithic Pixel Sensors for Future Collider Experiments

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Introduction

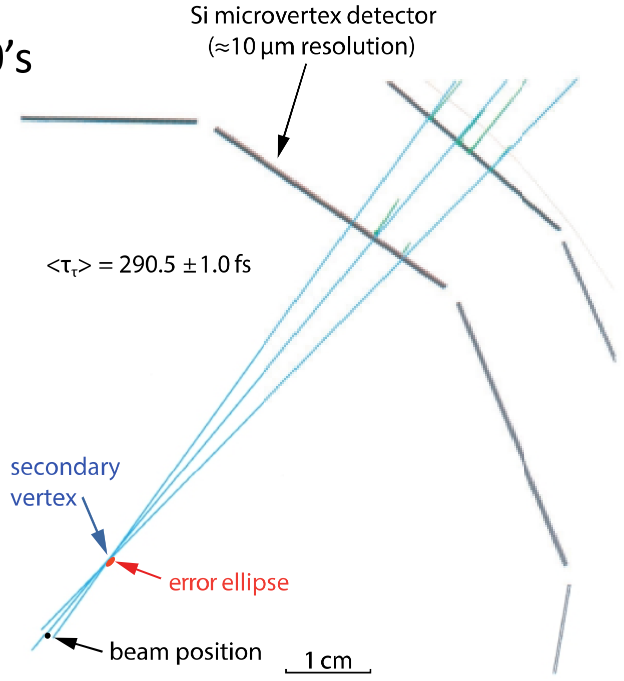
- Semiconductor detectors have been used for energy measurements since the 1960's

- In the 1980's, the availability of microfabrication technology, with the possibility of structuring the electrodes at the 50-100 μm level has vastly improved the position resolution, down to 10 μm or below.

→ Secondary vertices from short-lived particles (tau, B, D) become accessible

- It has radically changed the way experiments are thought of and conducted

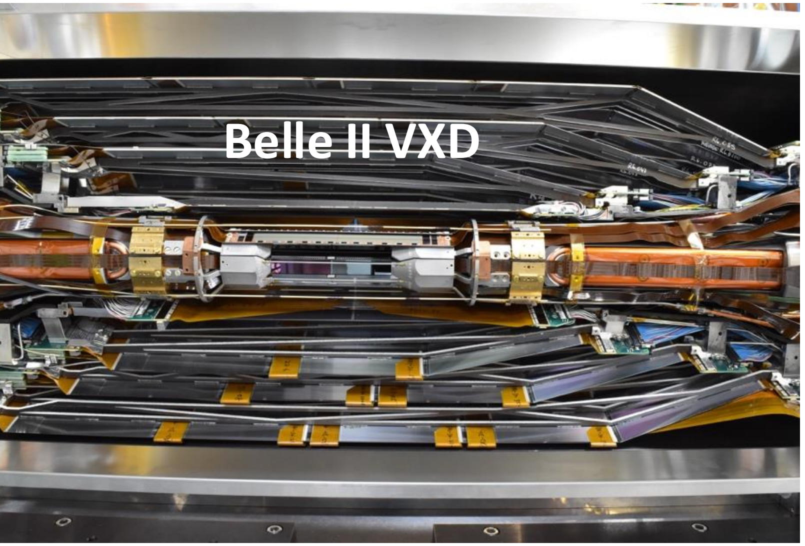
- Today, virtually every high energy physics experiment deploys semiconductor detectors

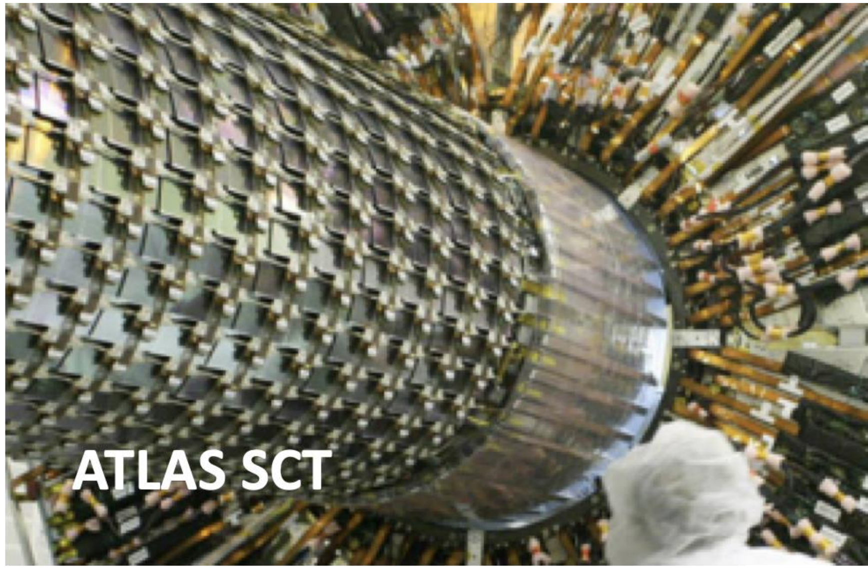


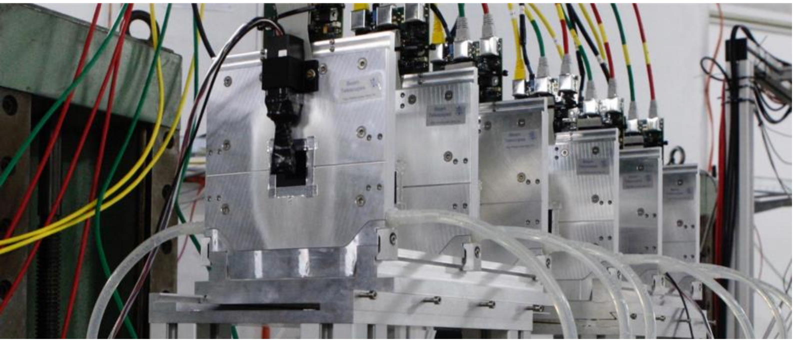
(c) Enlarged detail (200:1).

Fig. 8.1 Event display of the reaction $e^+e^- \rightarrow Z^0 \rightarrow \tau^+\tau^-$ in which one of the two τ leptons decays into three pions. Panels (b) and (c) show enlarged details demonstrating the precise measurement of track hits in the silicon microvertex detector and the recognition of a so-called 'secondary vertex' (OPAL detector at the e^+e^- collider LEP, source: CERN).

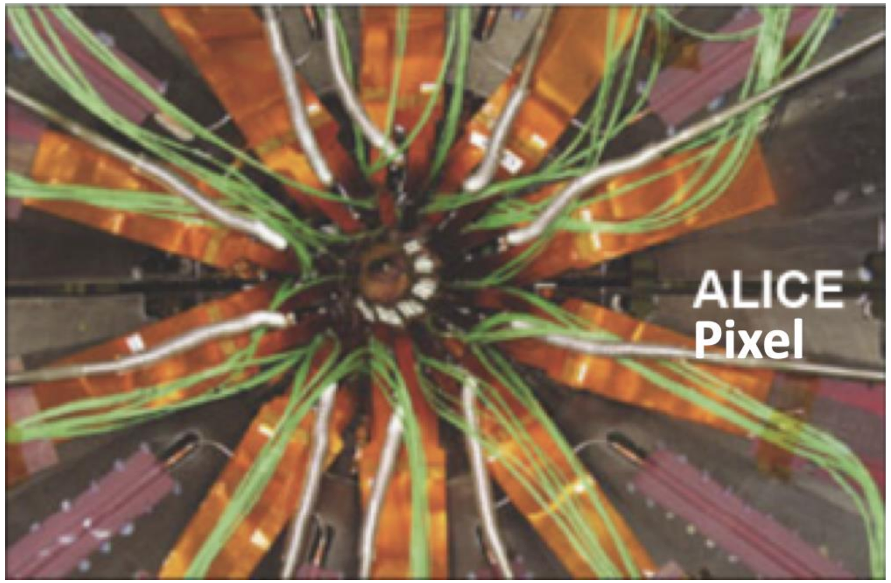
Nowadays: Silicon Everywhere

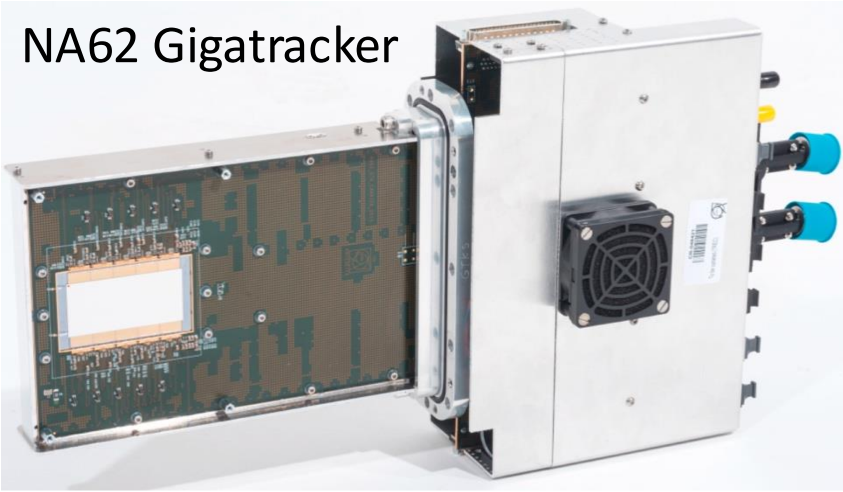




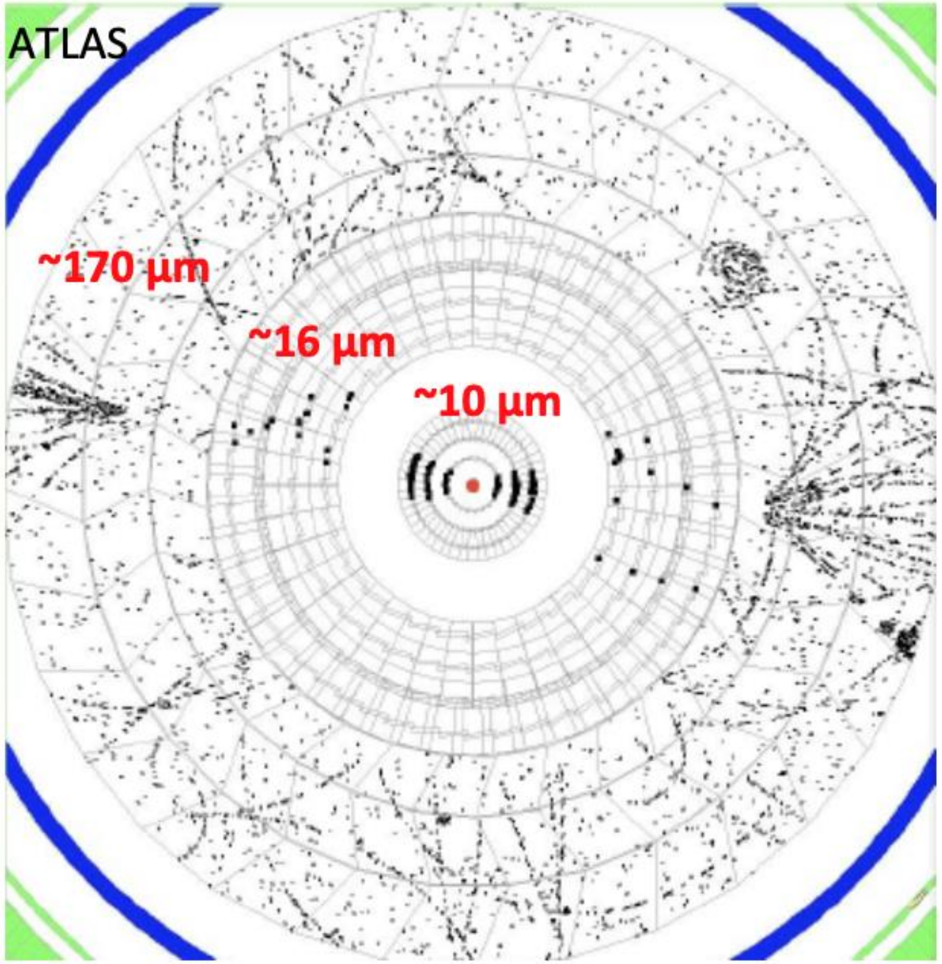


AIDA Telescope





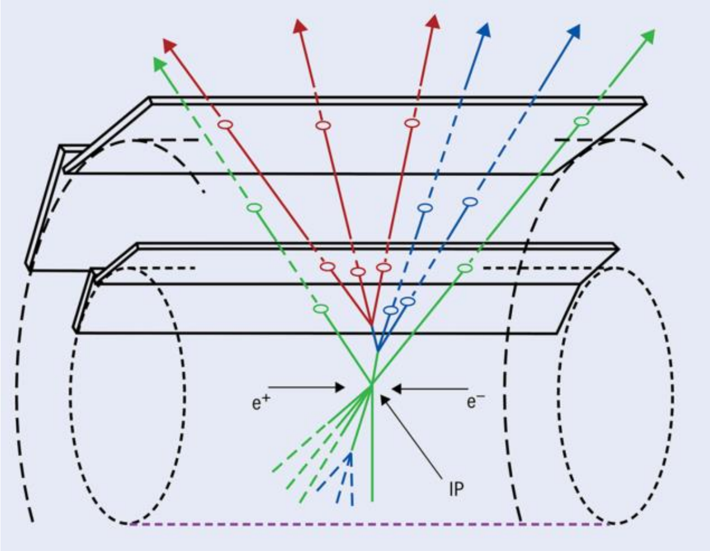
Tasks of Tracking Detectors



- Provide precise space points or space point clusters (vectors) originating from ionizing charged particles
  - Particle track finding from patterns of measured hits
  - Momentum (B-field) and angle measurement
  - Measurement of primary and secondary vertices
  - Multi-track separation and vertexing in the core of (boosted) jets
  - Measurement of the specific ionization (dE/dx)
- Keep the material influencing the paths of the particles to a minimum to avoid scattering in the material and secondary interactions

Vertex Resolution

- Concentrating here on properties for vertexing in HEP experiments

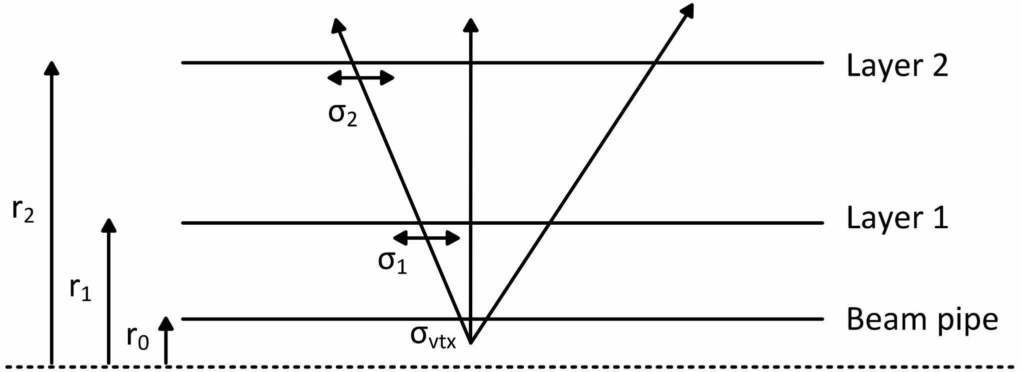


Vertex resolution

$$\sigma_{vtx} = \sqrt{\left(\frac{r_1}{\boxed{r_2 - r_1}} + 1\right)^2 \boxed{\sigma^2} + \boxed{(2r_1 - r_0)^2}(13.6\,\mathrm{MeV})^2 \boxed{\frac{x}{X_0}}\frac{1}{p^2}}$$

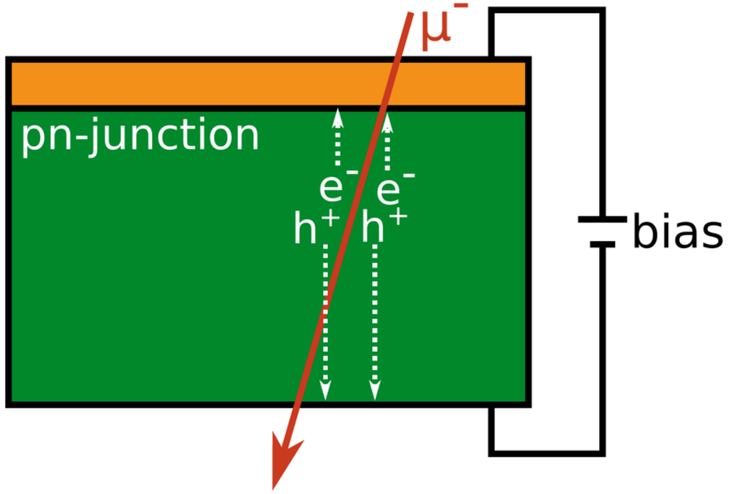
Detector requirements

- Fine segmentation
- Low material (beam pipe and detector layers)
- First layer as close as possible to the beam pipe
- Large lever arm



Silicon Detectors

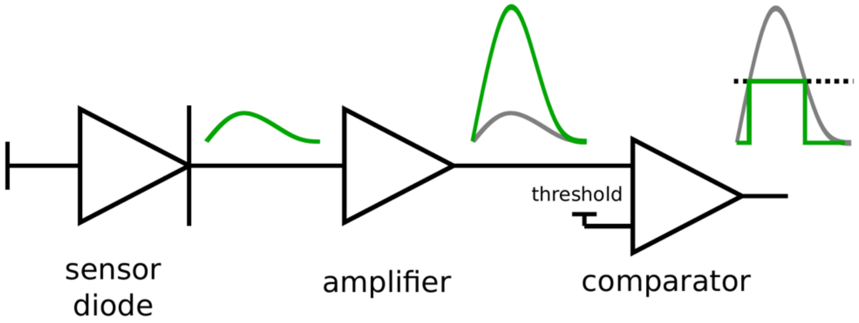
- Particles flying through the bulk produce ionization
- Ionization creates charges in the detector volume:
  - Electron-hole pairs in a semiconductor detector



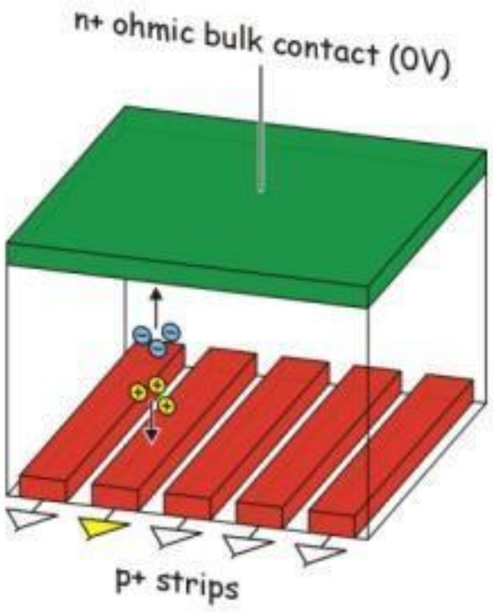
- Electric field applied to move the charges and 'induce' an electric current

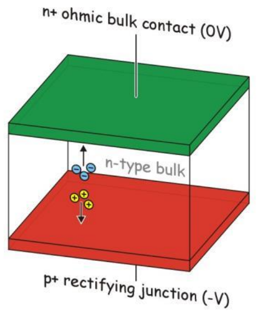
- Simplest detector: pn-junction
  - Operated in reverse bias → Depletion region
  - Traversing particle → Ionization = signal carriers in the silicon
  - Typical thickness 50 – 300 µm

- Shockley-Ramo Theorem:
  Moving charges induce signal on electrode



Increasing the Resolution: Segmentation





- **Silicon strip detectors**

A strip detector is an arrangement of strip like shaped implants acting as charge collecting electrodes (one-dimensional array of diodes).

- Double sided silicon strip detectors

Two dimensional position measurements can be achieved by applying an additional strip like doping on the wafer backside by use of a double sided technology.

- Pixel detectors

2D array of pixels. Each pixel = 1 pn-junction
True 2 dimensional information without ambiguities

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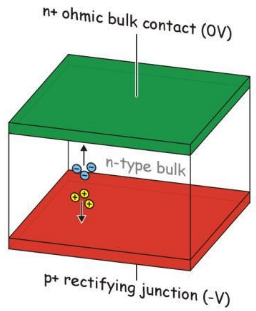

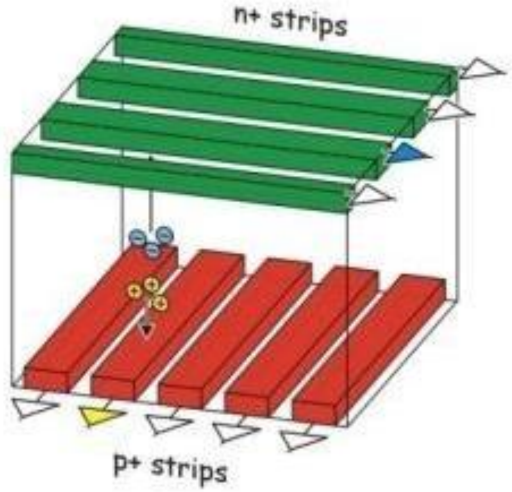

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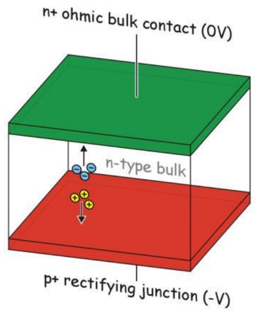

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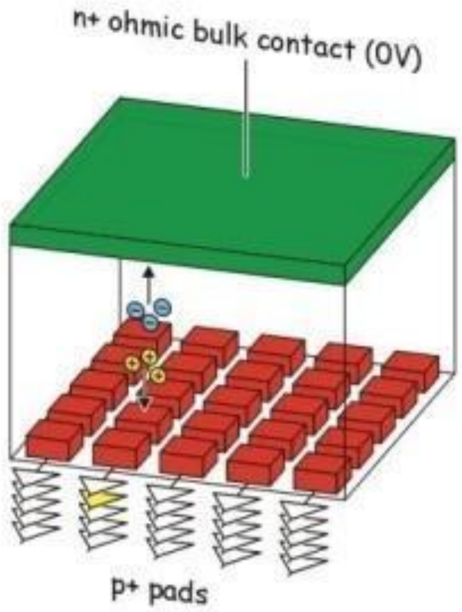
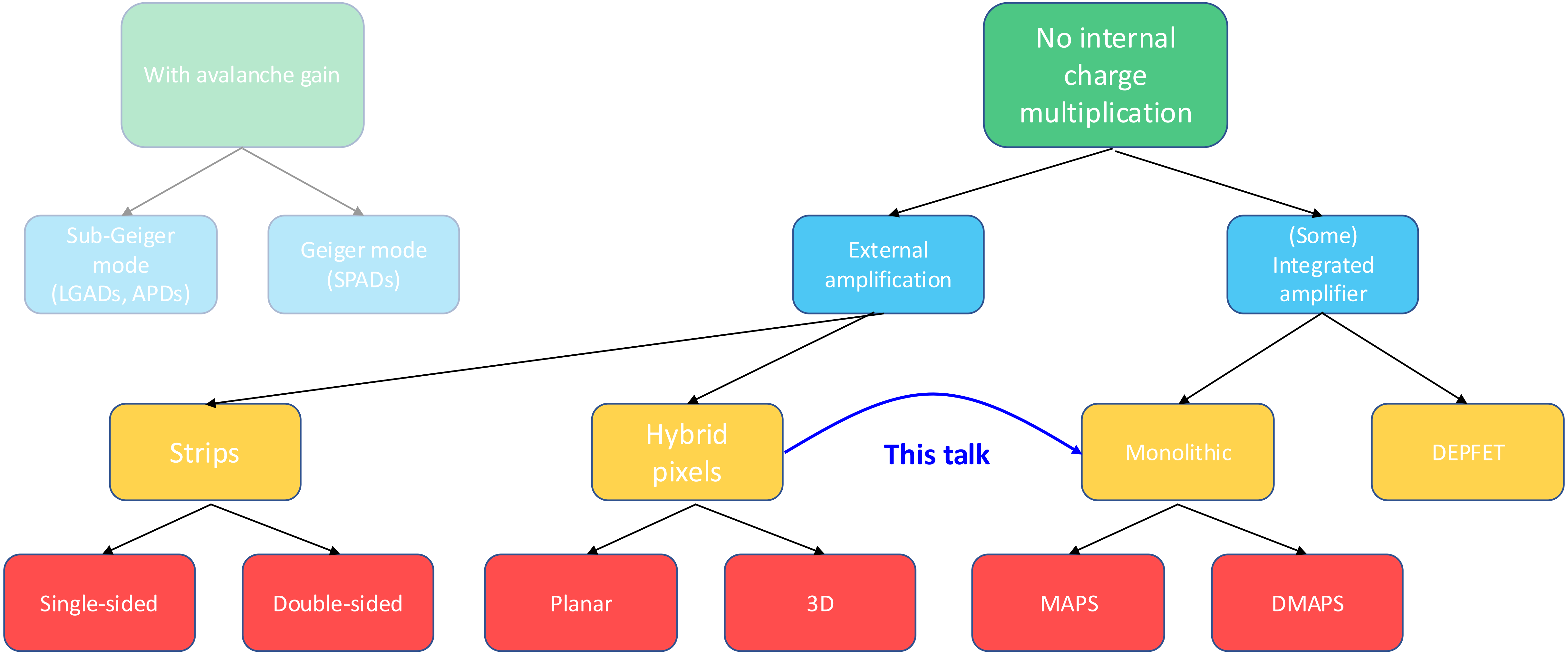
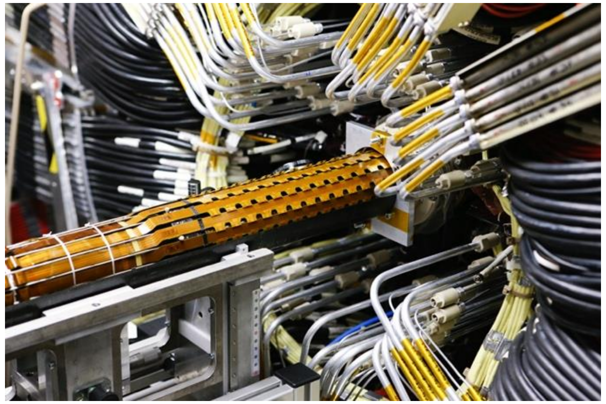


Semiconductor Detector Types

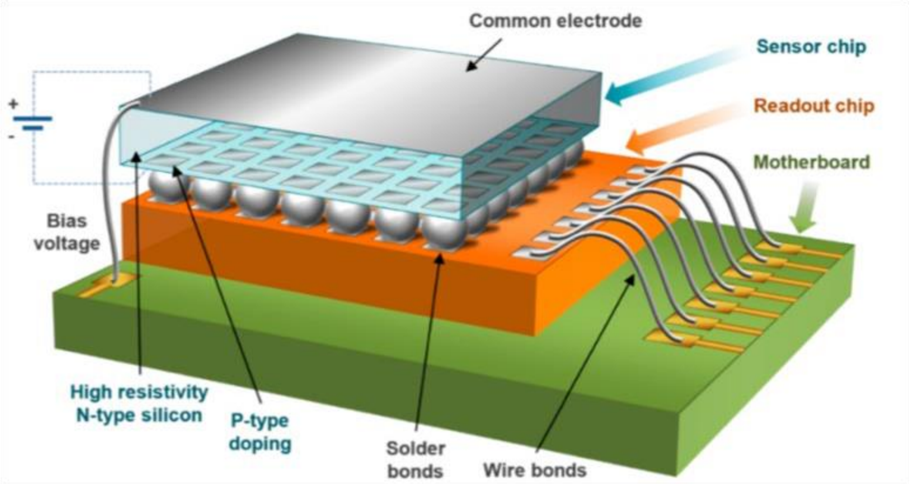


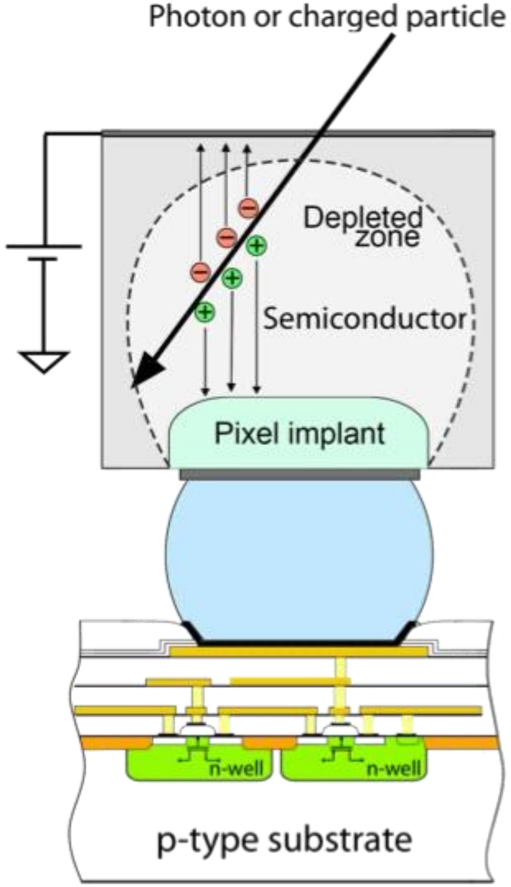
State-of-the-art of LHC Detectors

All based on **Hybrid Pixel Detectors**

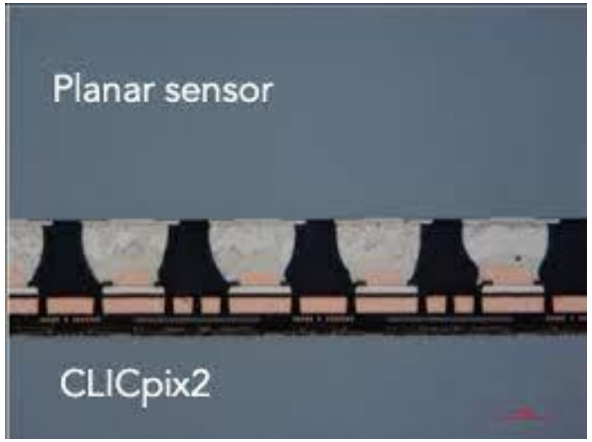


ATLAS IBL



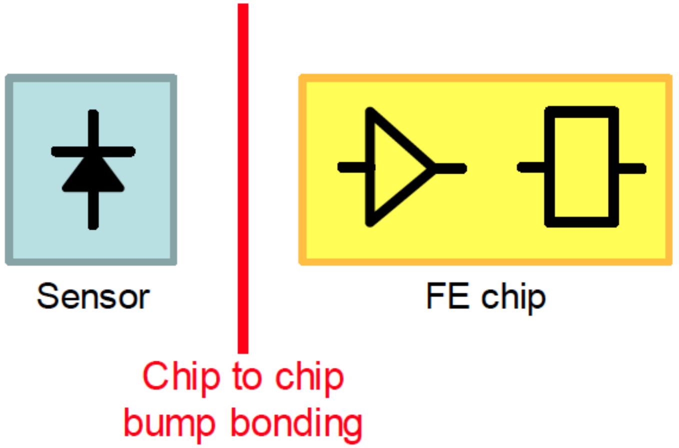


LHCb Velo



From Hybrid Pixels to Monolithic

- Standard HYBRID pixels
  - Various sensors: planar-Si, 3D-Si, diamond
  - Mixed signal R/O chip



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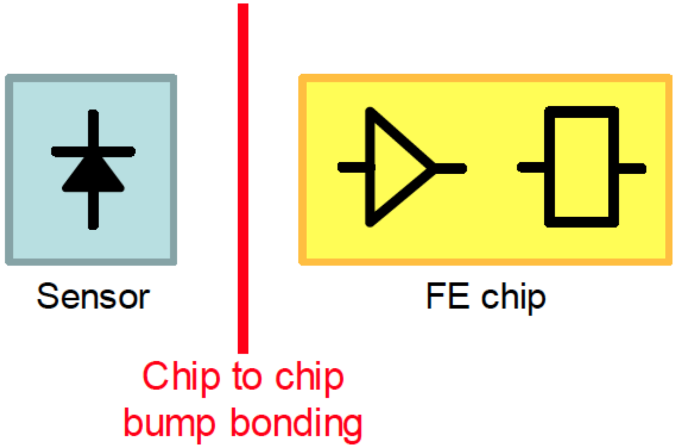
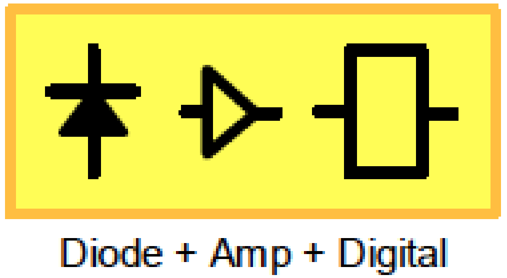


- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion)
  - Depleted DMAPS using HR substrate and/or HV process to create depletion region



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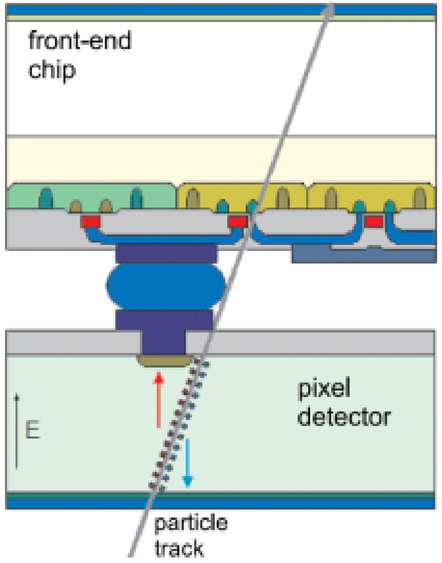
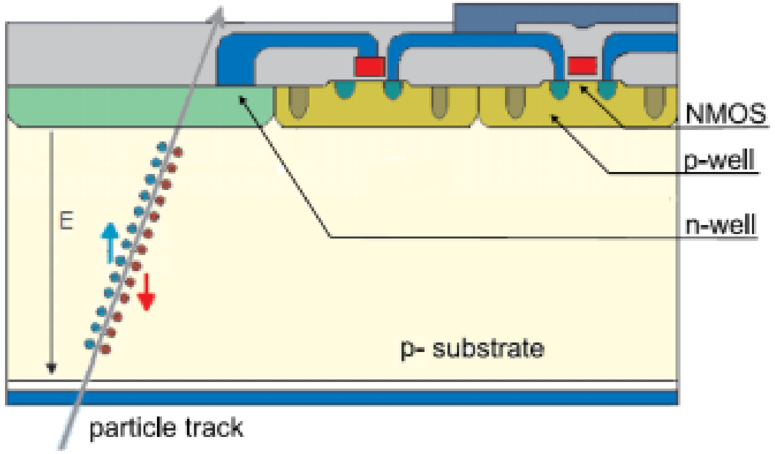


Moderate spatial resolution (10-100 µm)
High material budget (few % X_0)
High cost
Radiation hard

- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion)
  - Depleted DMAPS using HR substrate and/or HV process to create depletion region

High spatial resolution (1 µm)
Low material budget (0.1 % X_0)
Needs modifications for radiation
Simpler readout architecture



(D)MAPS

(Depleted) Monolithic Active Pixel Sensors

- Monolithic

Signal generation + readout integrated on a single unit

Low material budget

- Active

Detection and in-pixel amplification and processing

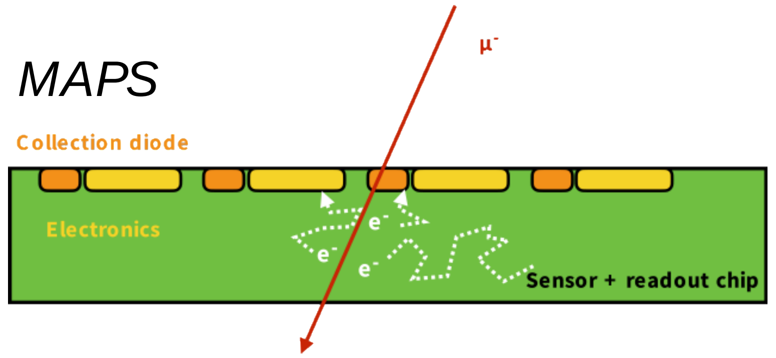
- Depleted

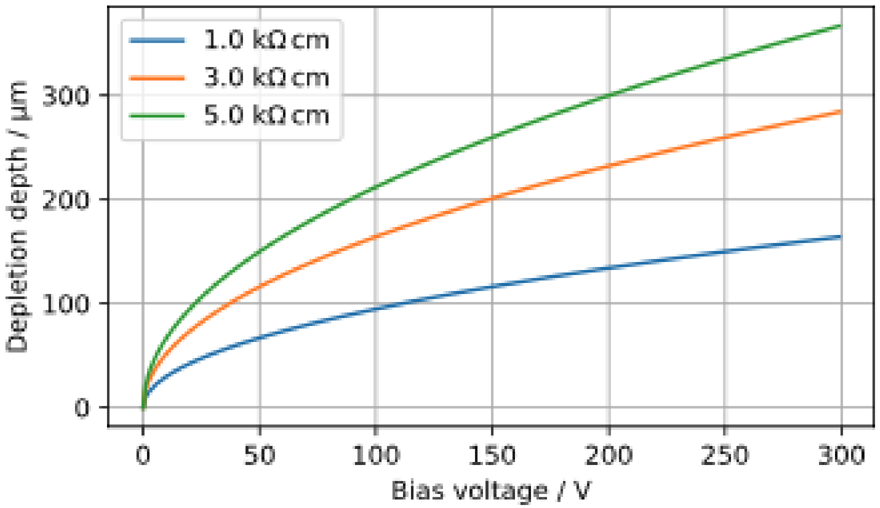
HV process or HR substrate to create depletion region

Fast charge collection via drift

Large depleted volume with large signal

$$d \sim \sqrt{\rho \cdot V}$$





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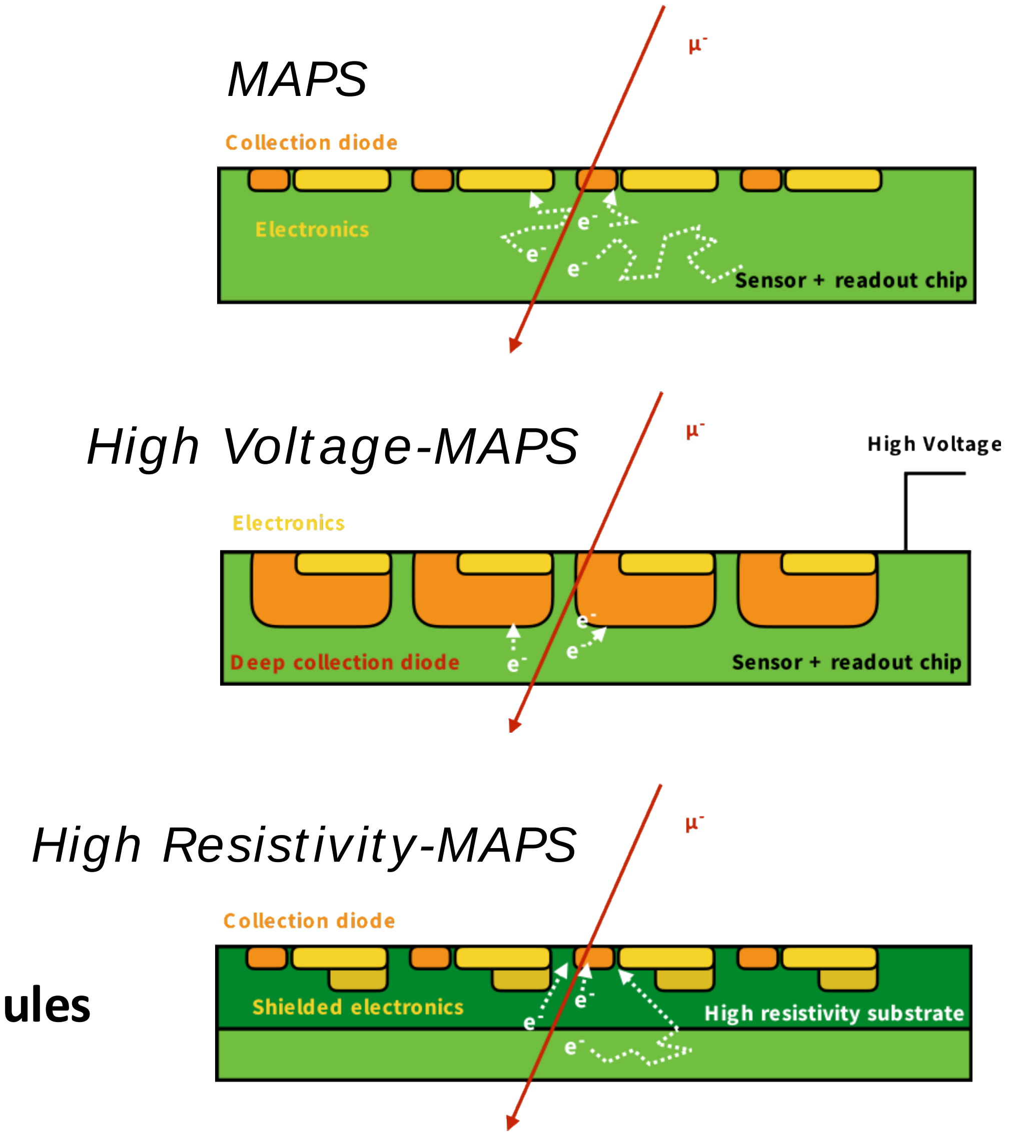
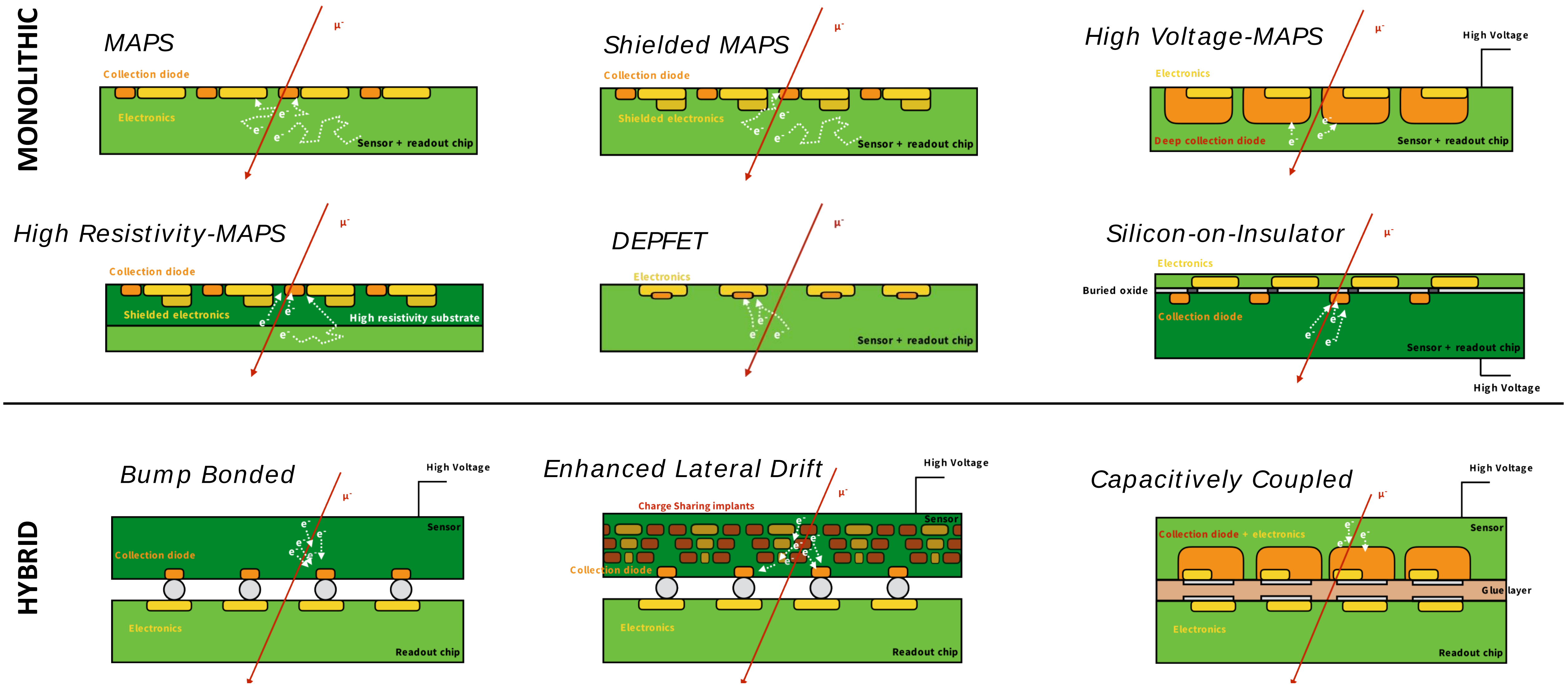
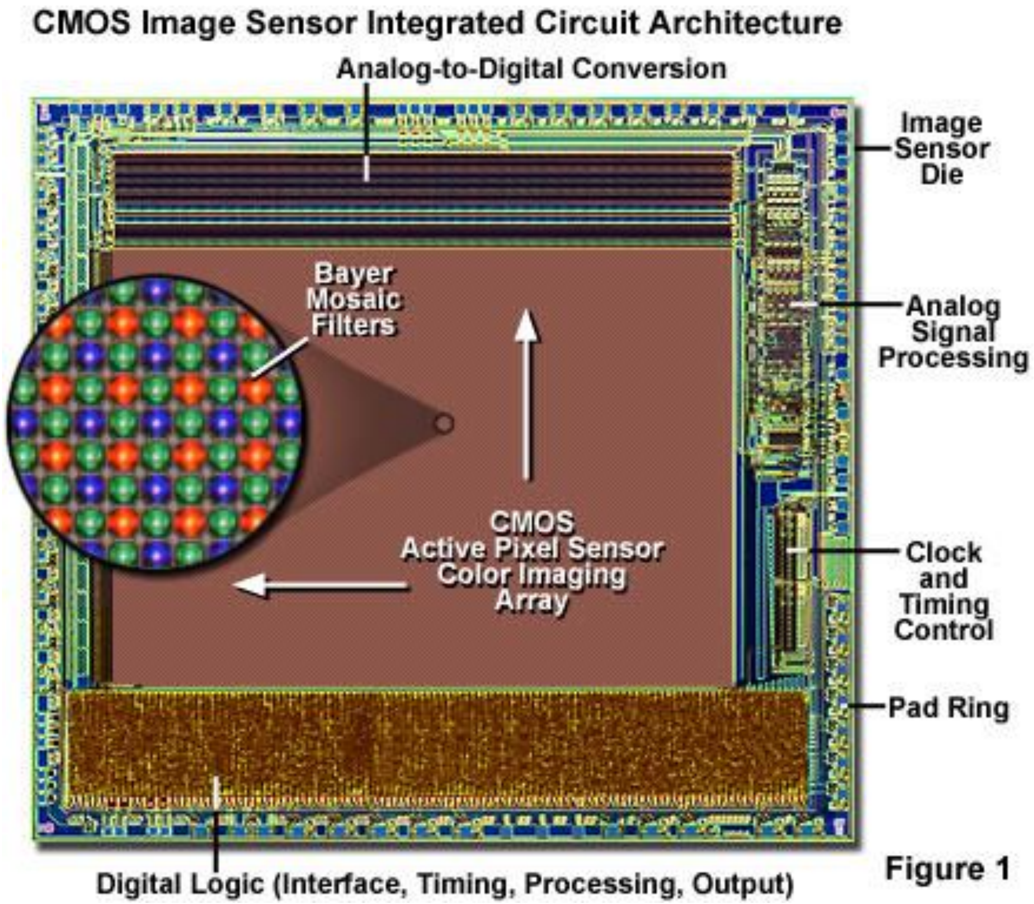
Very low mass, small pixel sizes, highly integrated modules



Many Different Implementations



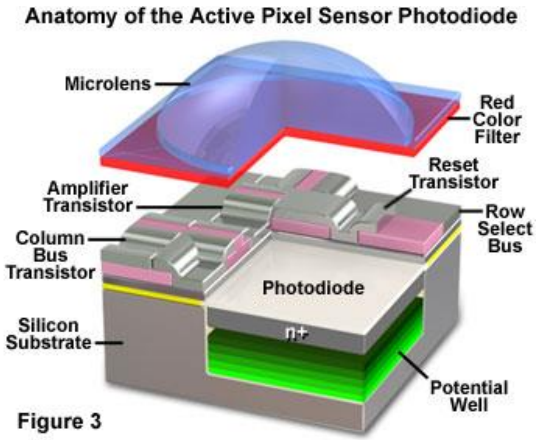
CMOS Image Sensors (CIS)



- All-in-one: Electronic Camera On Chip

- Standard CMOS technology:
  - Lower production costs
  - Simpler integration of complex functionalities

- Very small pixels (1 um, 40 M pixels)
- Single low supply and power consumption
- Increased speed (column- or pixel - parallel processing)



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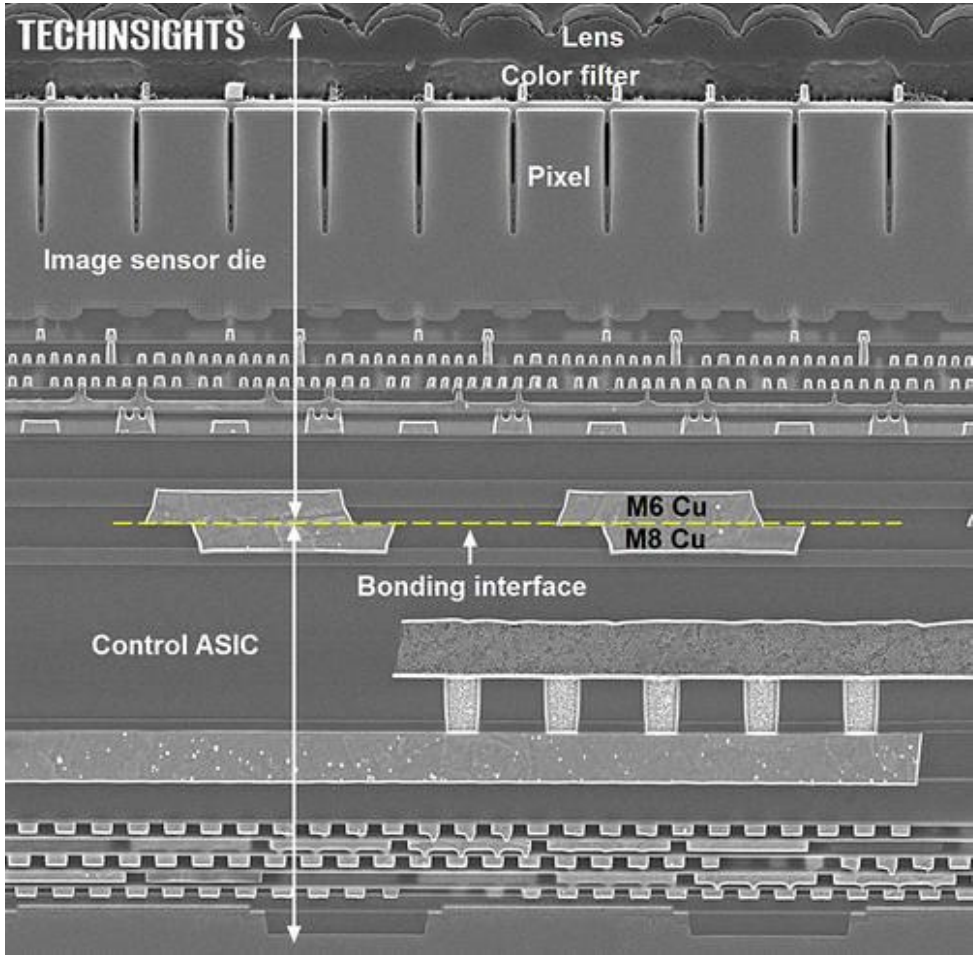

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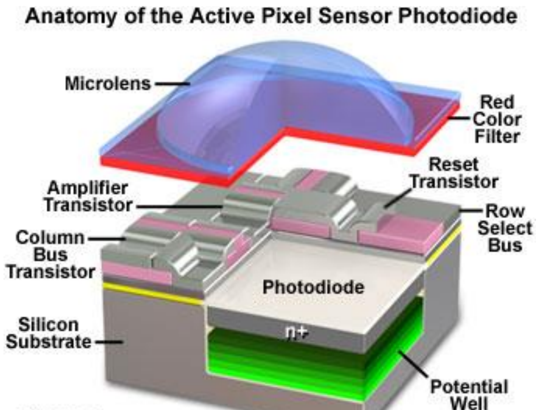
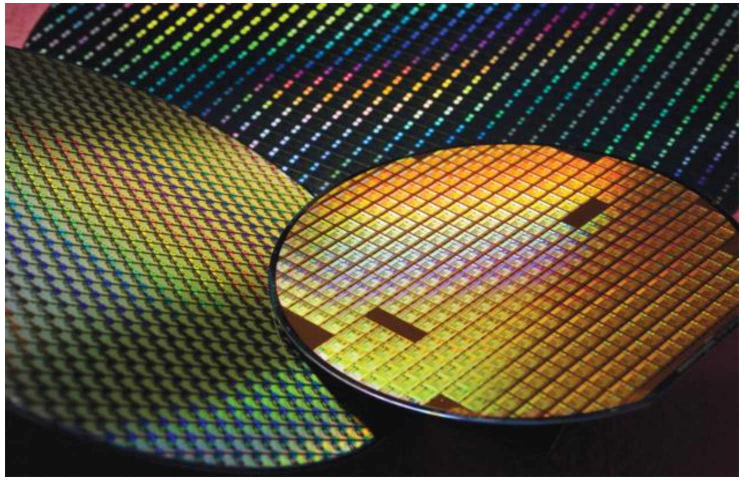


Figure 3

Commercial Vendors



Monolithic sensor technologies based on commercial processes

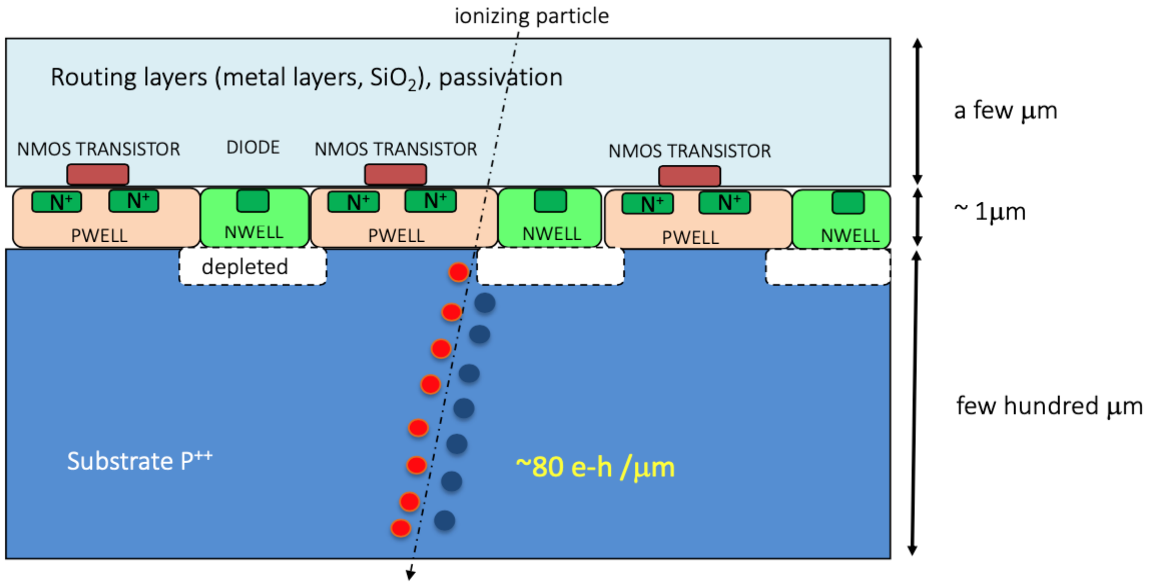
Reduced cost, large throughput, fast turnaround, large wafers

Complex layouts, limited information on processing details, long term support

Various processes in use currently in HEP:

- TowerJazz 180 nm, 65 nm
- TSI 180 nm
- L-Foundry 150, 110 nm
- Globalfoundries 130 nm …

Particle Detection in CMOS APS



In standard CMOS image sensors, the photodiode is implanted in low-resistivity silicon.

Depletion is shallow
Charge collection efficiency is low
The detector element covers a small fraction of the pixel area

-> Not suitable for measurement of charged particles

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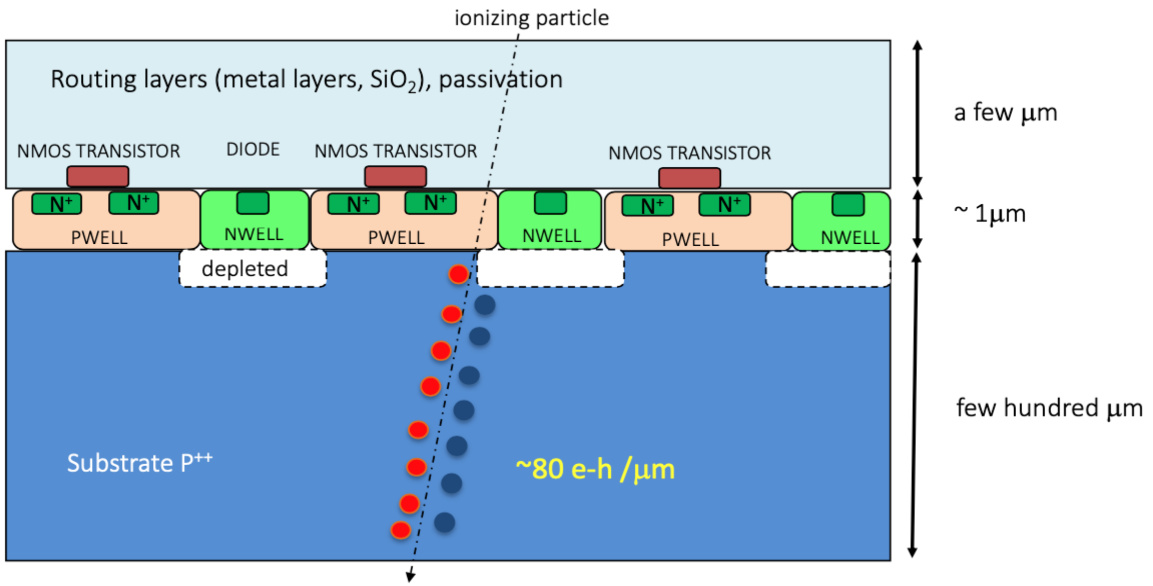

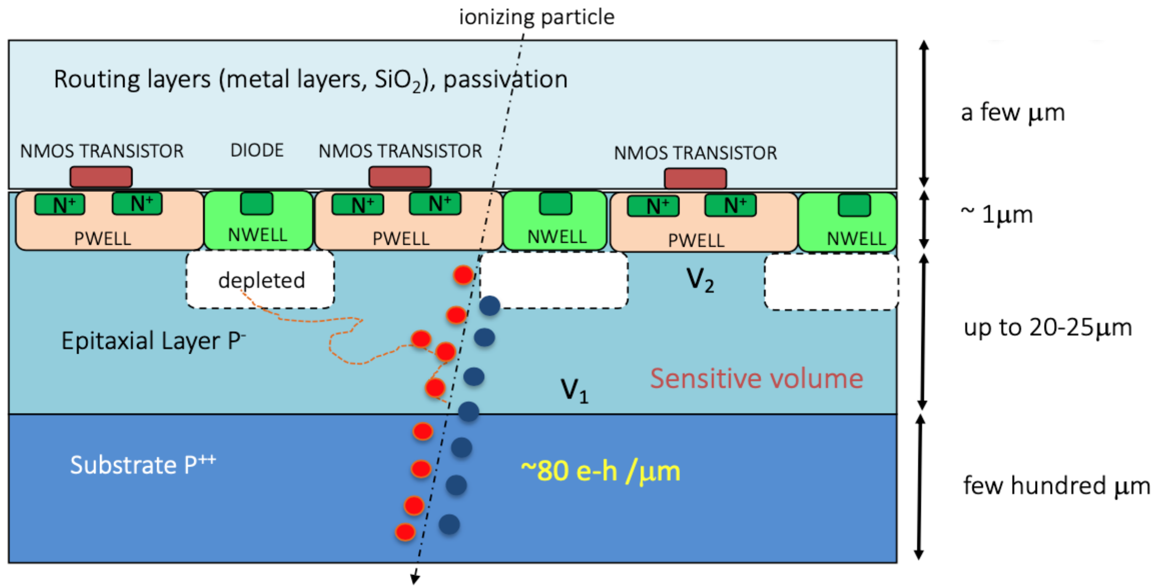

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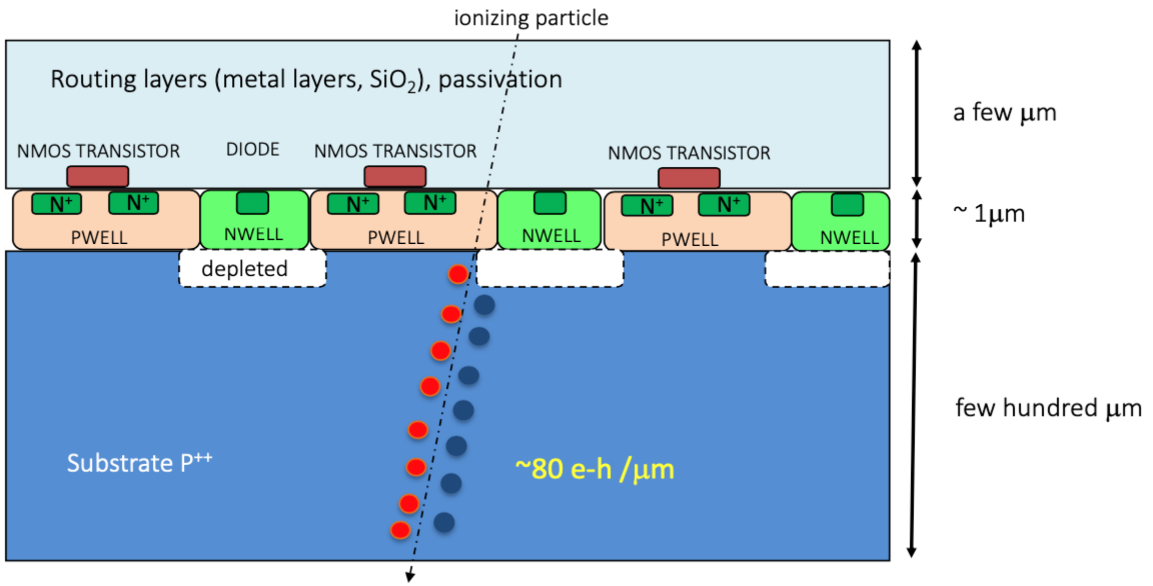
Use of an epitaxial layer with doping few orders of magnitude smaller than the one on the p++ substrate

Potential barriers at boundaries:

$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}} \qquad V_2 = \frac{kT}{q} ln \frac{N_{PWELL}}{N_{epi}}$$

Which keep minority carriers confined in the epi-layer until they reach the depleted region under nwell

Particle Detection in (Thinned) CMOS APS



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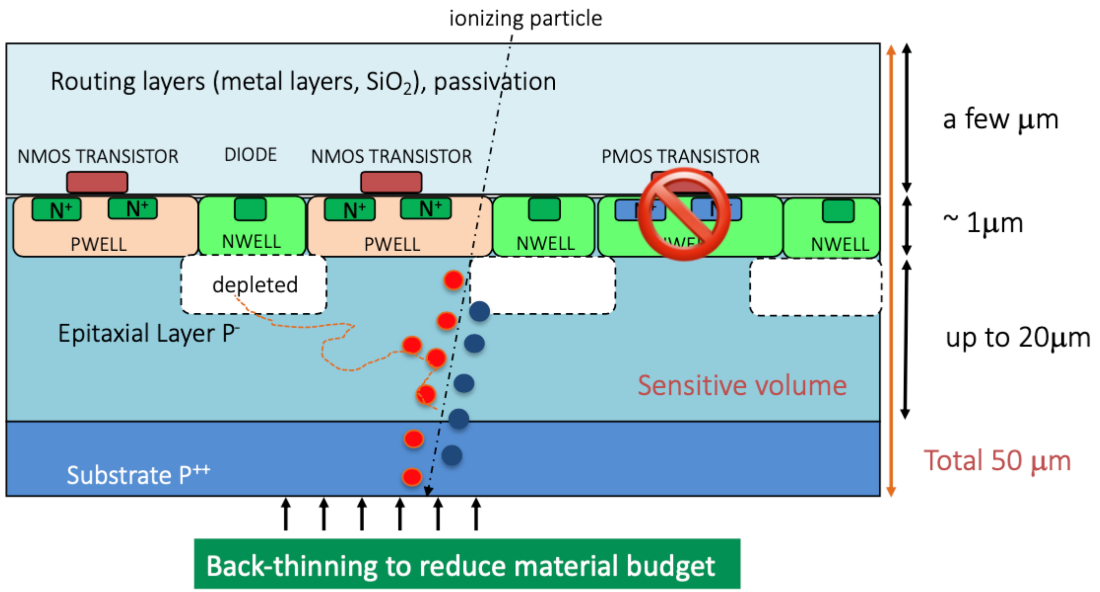

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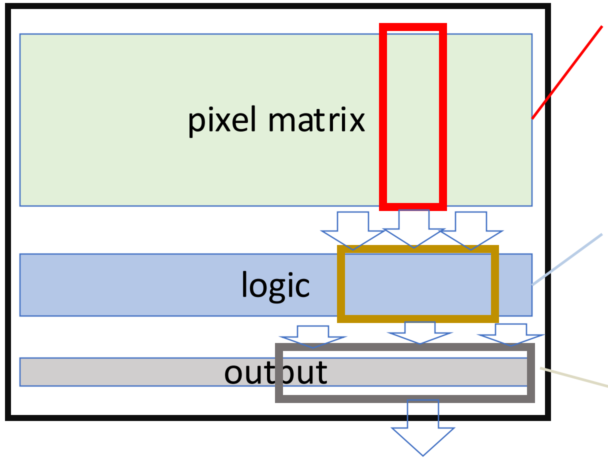
Readout Architectures

- Generalities



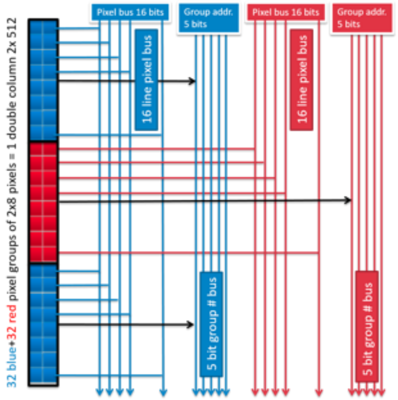
Assume digitisation
Need to absorb the max hit rate
Power connected to clock-speed

- Multiplexing toward output (! bottleneck)
- Potential trigger logic
- Power depends on memory management

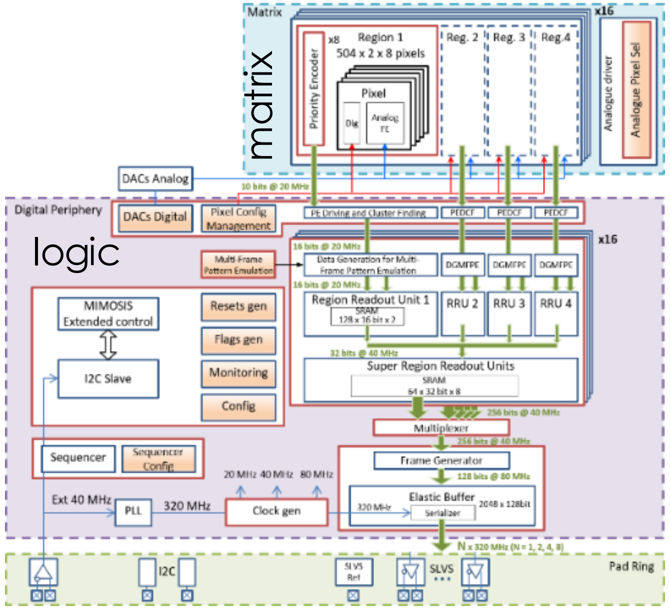
- Power depends on read-out rate (#outputs and clock)

- Synchronous
  - Priority encoder: ALPIDE, MIMOSIS
    => adapted for stitching: MOSS
  - Column-drain architecture: MONOPIX
  - Data driven,
    fired pixel adress within 20 ns over 2cm

- Asynchronous
  - no in-matrix clock → lower power
    - Still data-driven
  - MALTA with pulses through
  - Adapted to stitching: MOST



- Complex logic
  - MIMOSIS case
  - Required by fluctuating rate



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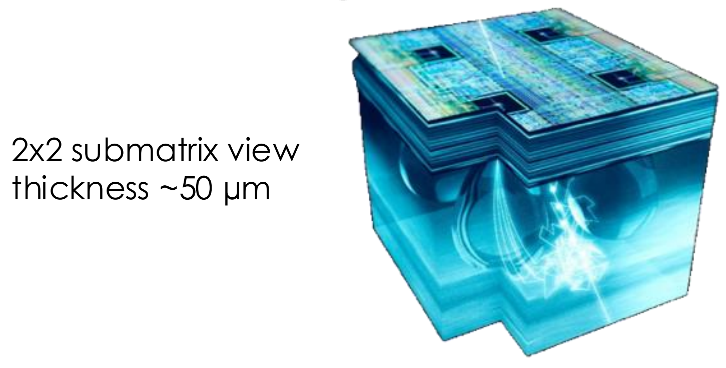
CMOS-MAPS R&D in a Nutshell

- **General concepts**



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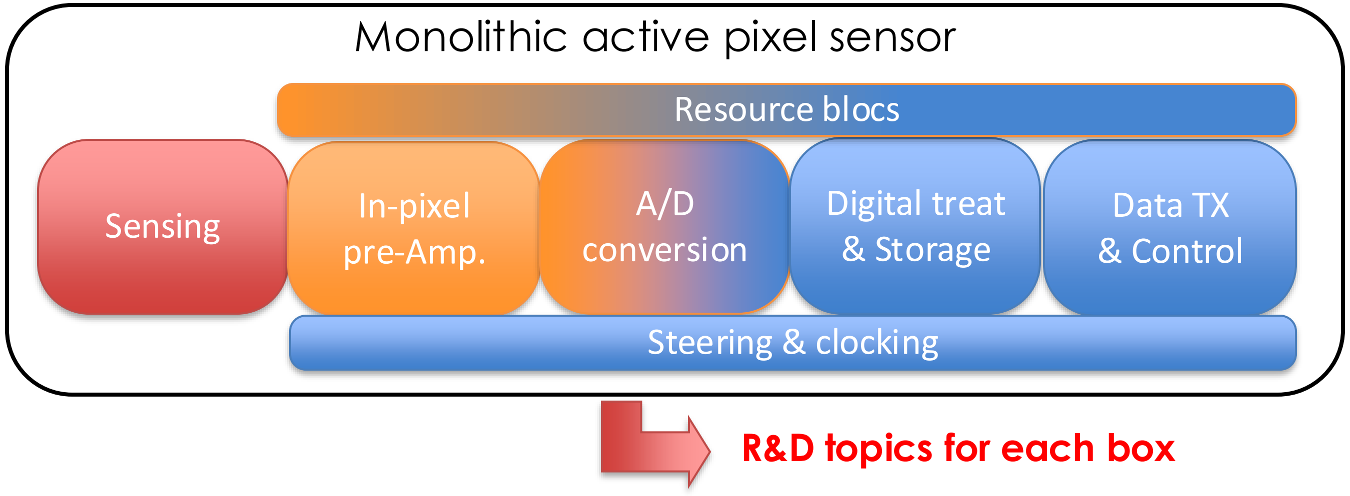
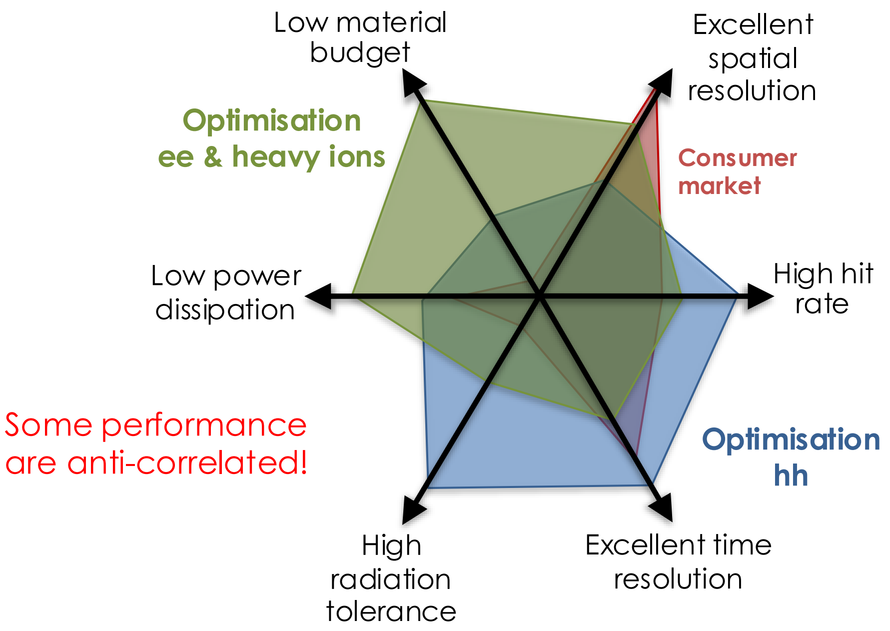
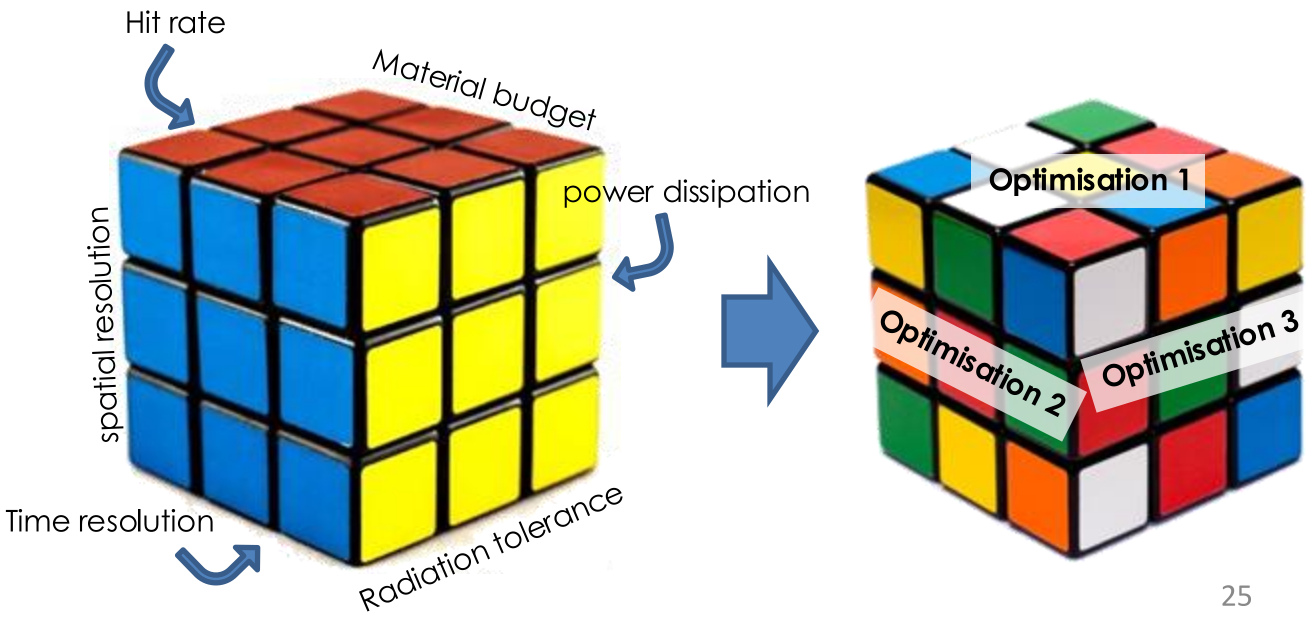


- **Performance is a matter of optimisation**

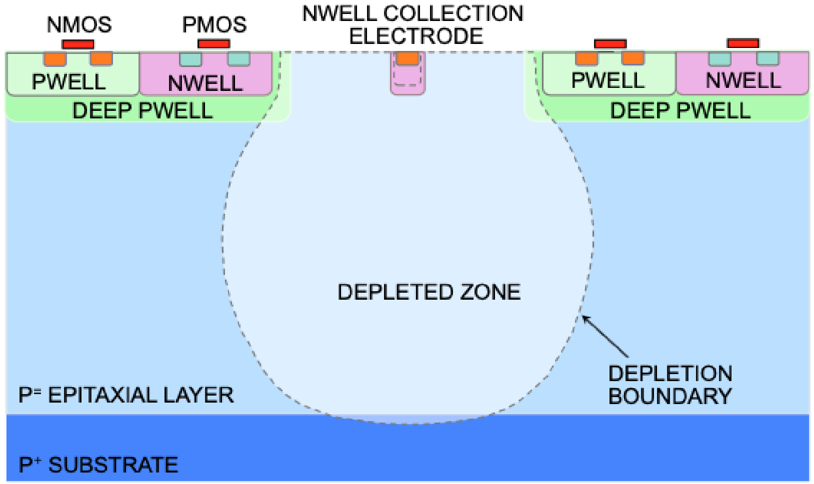


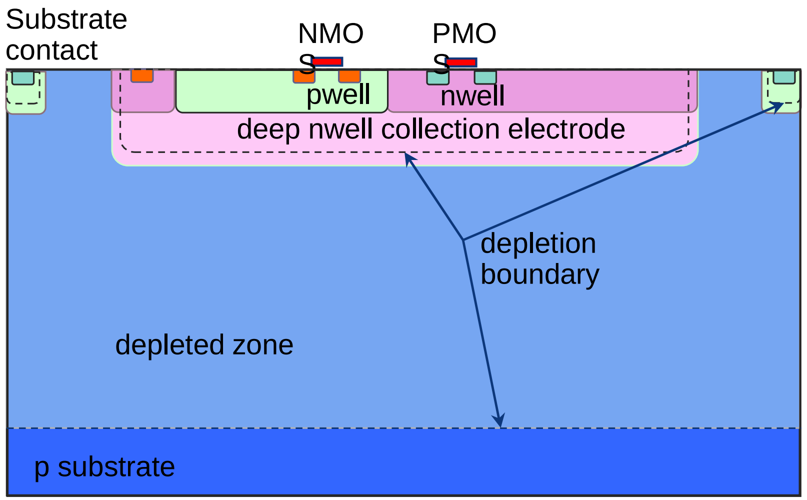
or



Towards Better Radiation Tolerance - I

- **Electrode design**





Electronics outside the charge collection well

Small collection electrode

Very small sensor capacitance (<5fF)
→ Low noise, low power, high speed

Longer drift distances and low field regions
→ Radiation hardness needs improvements

Electronics inside the charge collection well

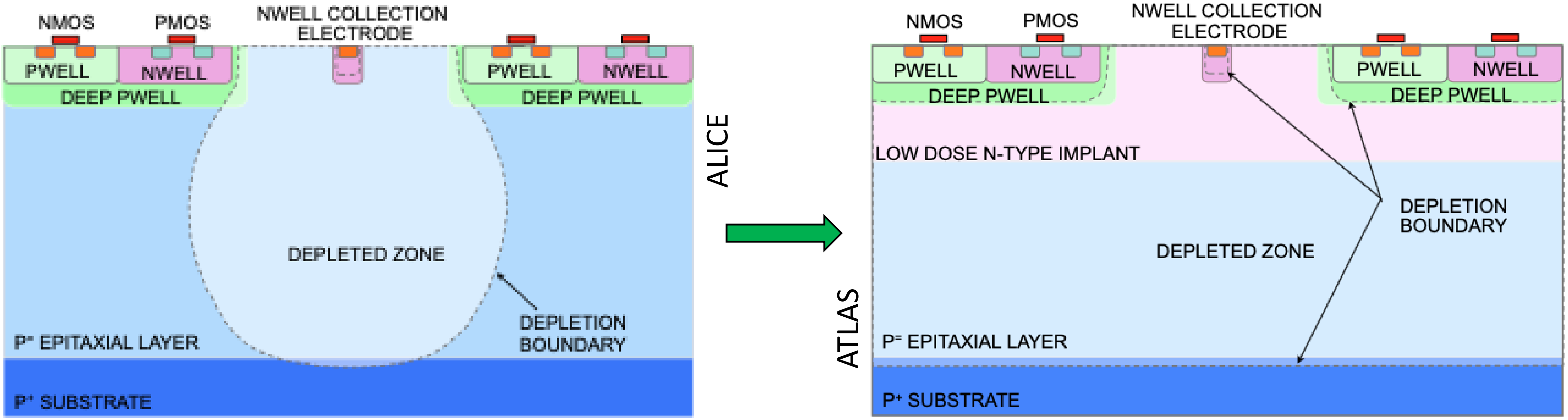
Large collection electrode

No low field regions
Shorter drift distances
Less trapping → More radiation hard

Larger sensor/well-well capacitance (>100 fF)
→ Penalties in noise/power/speed

Towards Better Radiation Tolerance - II

- **Process modification**



- Partially depleted epitaxial layer
  - Charge collection time < 30 ns
  - Operational up to 10^{14} 1 MeV n_{eq}/cm^2

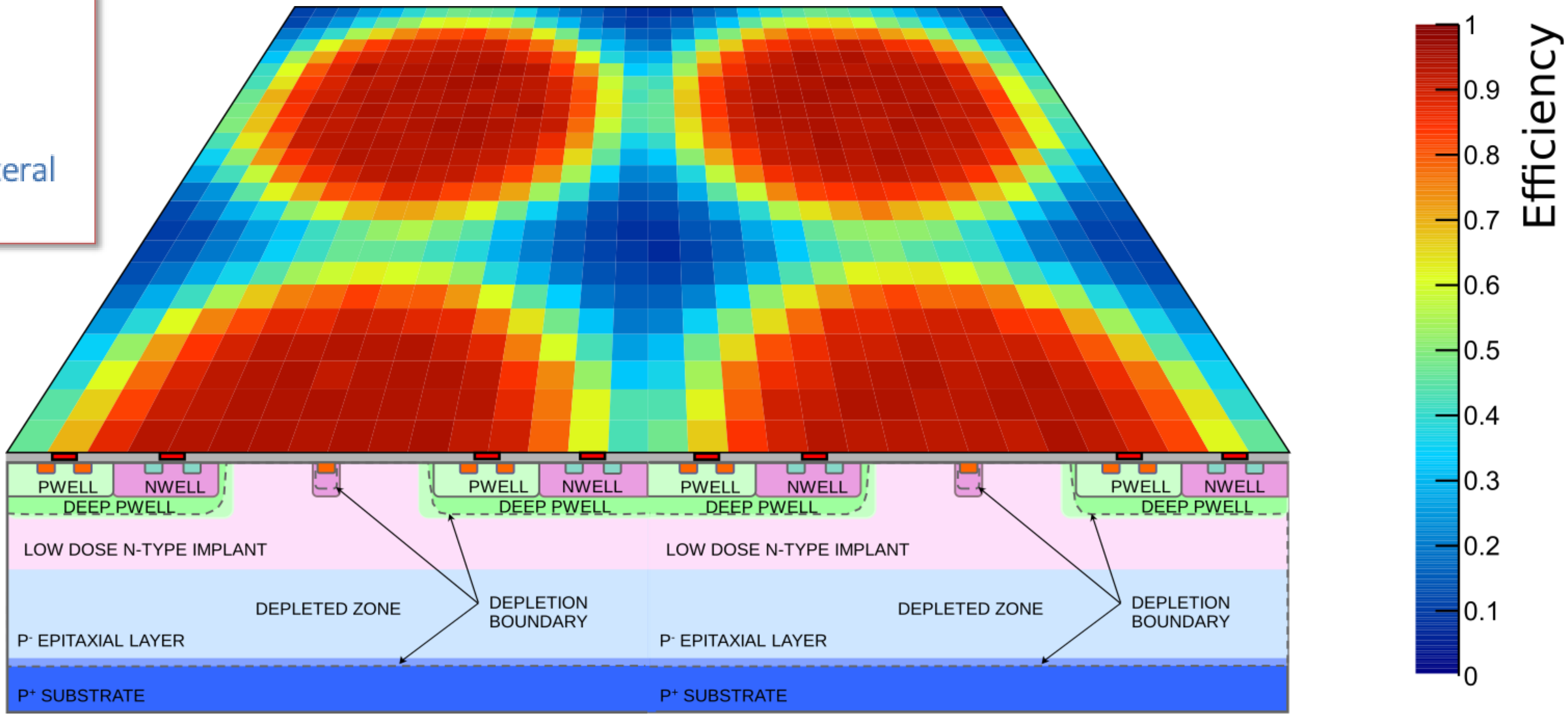
- Modified process: Additional planar n-type implant
  - Full depleted epi layer (up to 40 um deep)
  - Fast charge collection < 1 ns
- 3 nm gate oxide for good TID

→ Order of magnitude improvement in rad. hardness

TJ-Monopix Pixel Design Issues

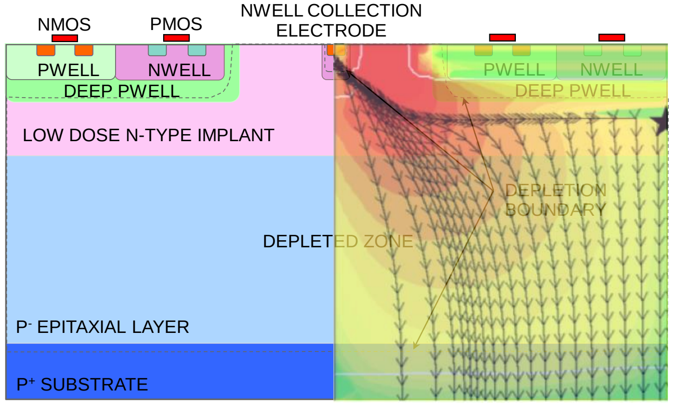
Neutron irradiated
$5x\ 10^{14}\ n_{eq}/cm^2$

Inefficiency at pixel edges due to low lateral electric field

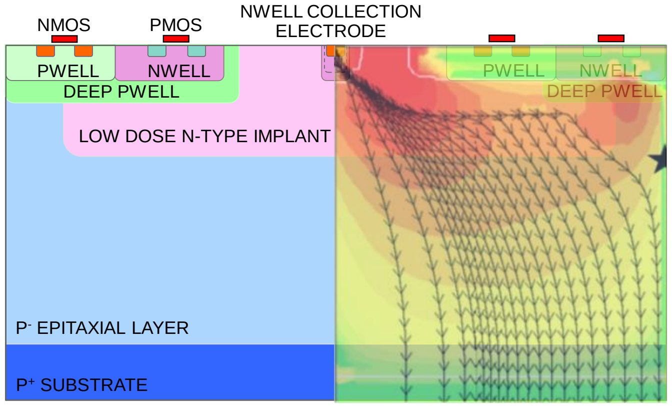


TJ-Monopix/MALTA Modifications

STD

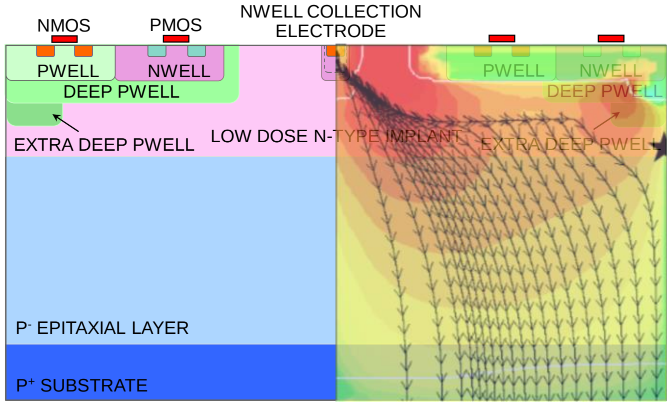


NGAP



Gap in the low dose N-type implant

XDPW

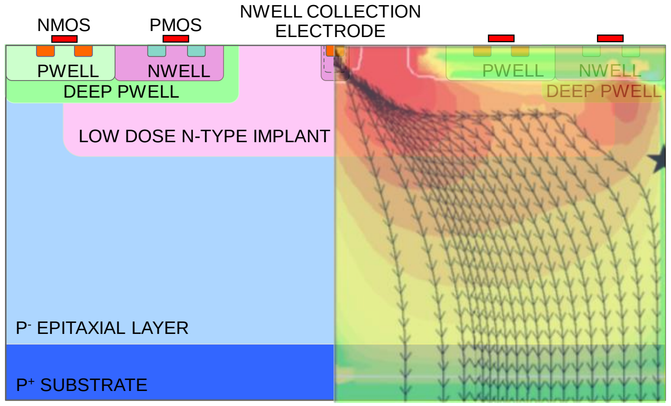


Extra Deep P-Well

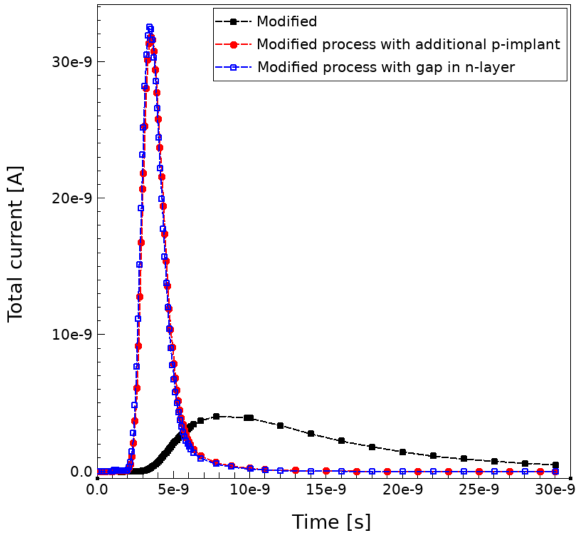
Goal:

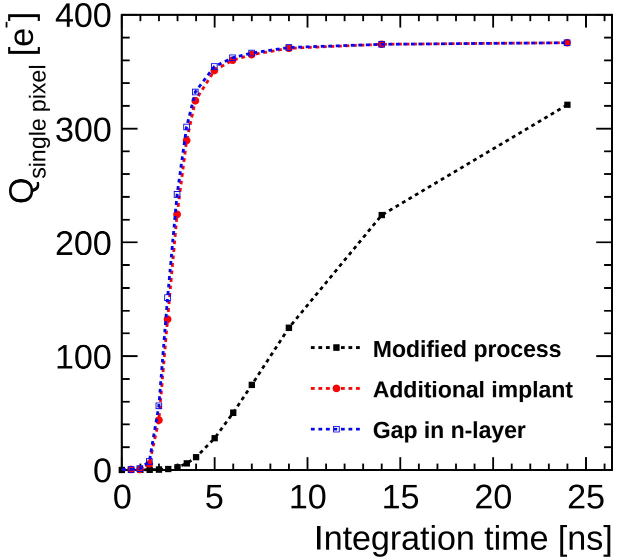
- Bend the field lines towards the collection electrode
- Shorten the drift path
- Increase charge collection speed, specially at pixel borders

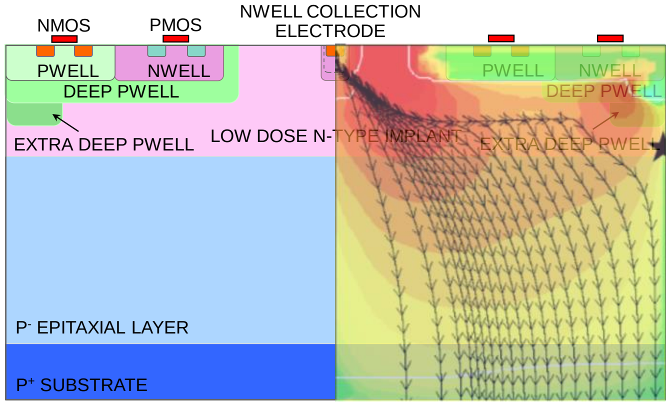
TJ-Monopix/MALTA Modifications



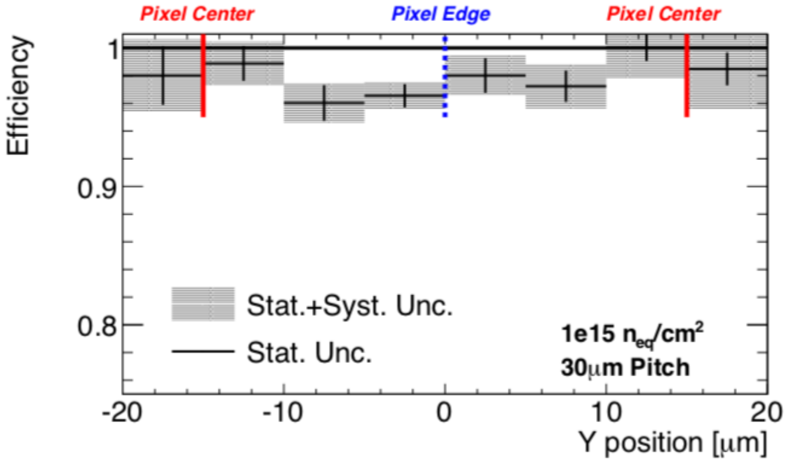
Gap in the low dose N-type implant

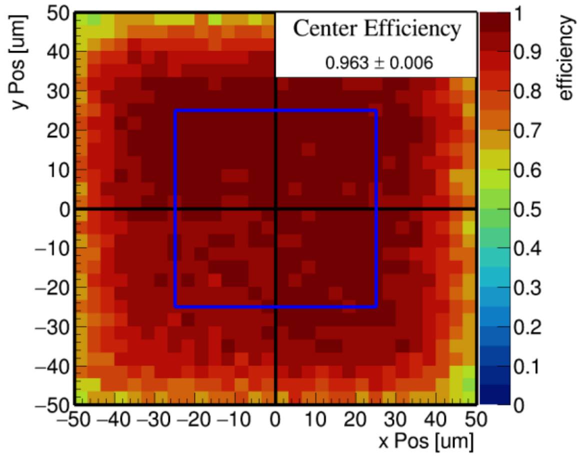






Extra Deep P-Well





→ Result: Faster charge collection, larger signal, high efficiency

Conclusions

- CMOS vertex and trackers in HEP are a mainstream technology:
  - Construction of large trackers for LHC
  - Possibilities for future upgrades (Belle II, LHCb, NA64) and new machines (Higgs factories)

- Strong interest for R&D to fully exploit potential of DMAPS
  - High granularity
  - Low material budget
  - Large area (vertexing, tracking, calorimetry, TOF) at reduced cost
  - Utilize industry postprocessing
  - Build compact, highly integrated modules

- Semiconductor trackers, and CMOS in particular, are here to stay…

  - **The devil is in the details**

The Belle II VXD Upgrade

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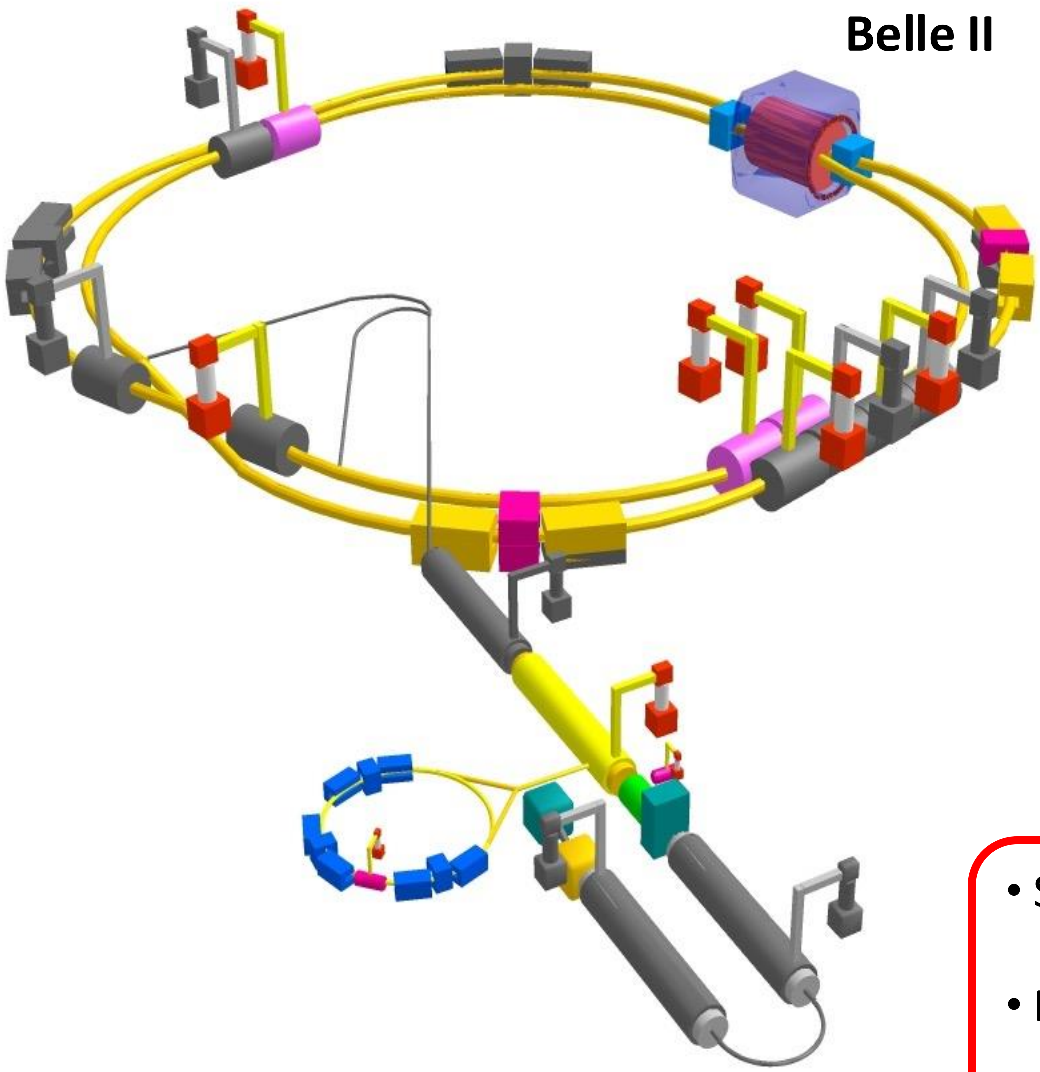
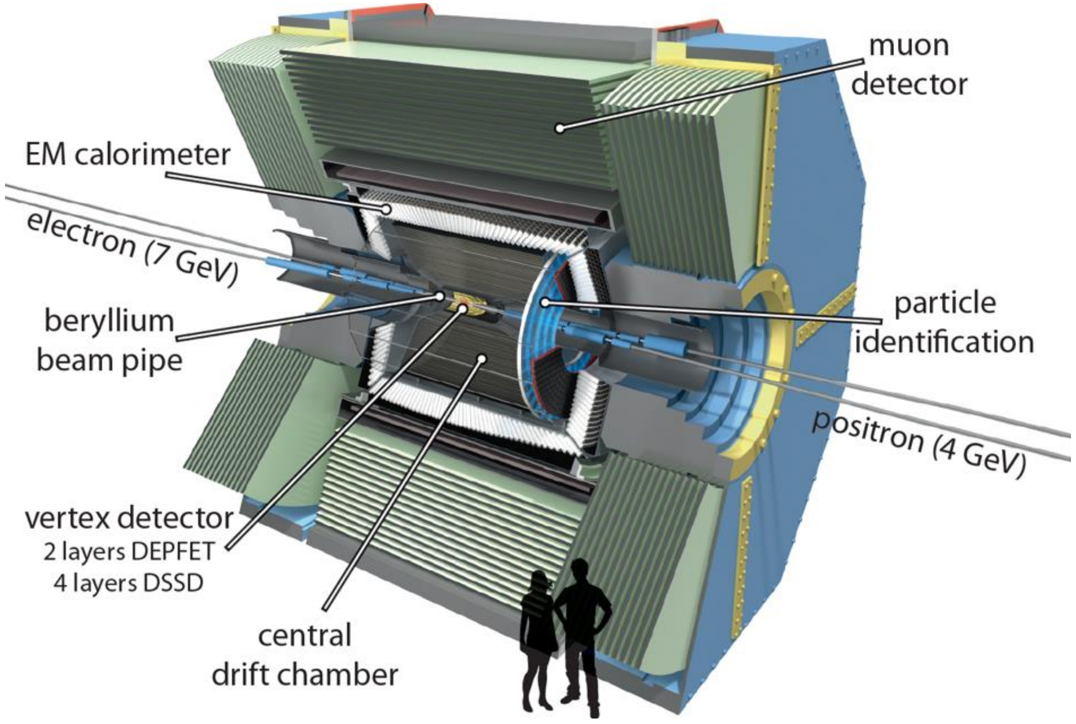
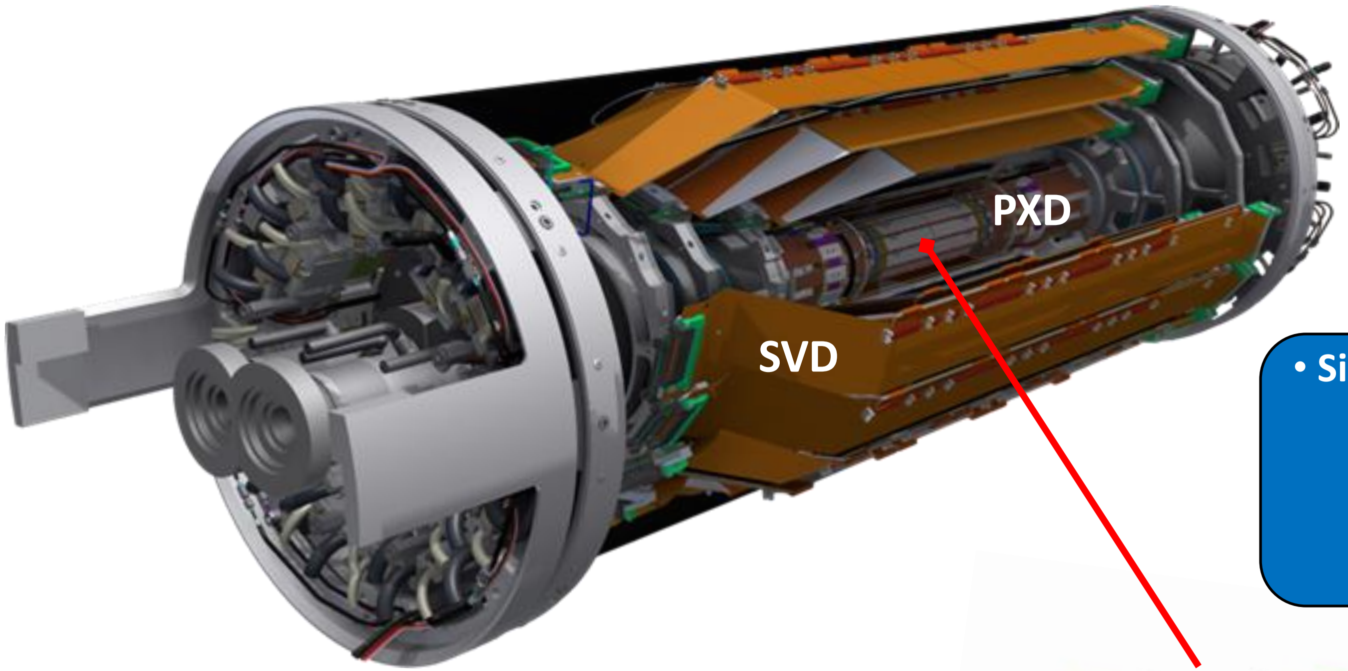
SuperKEKB and the Belle II Experiment



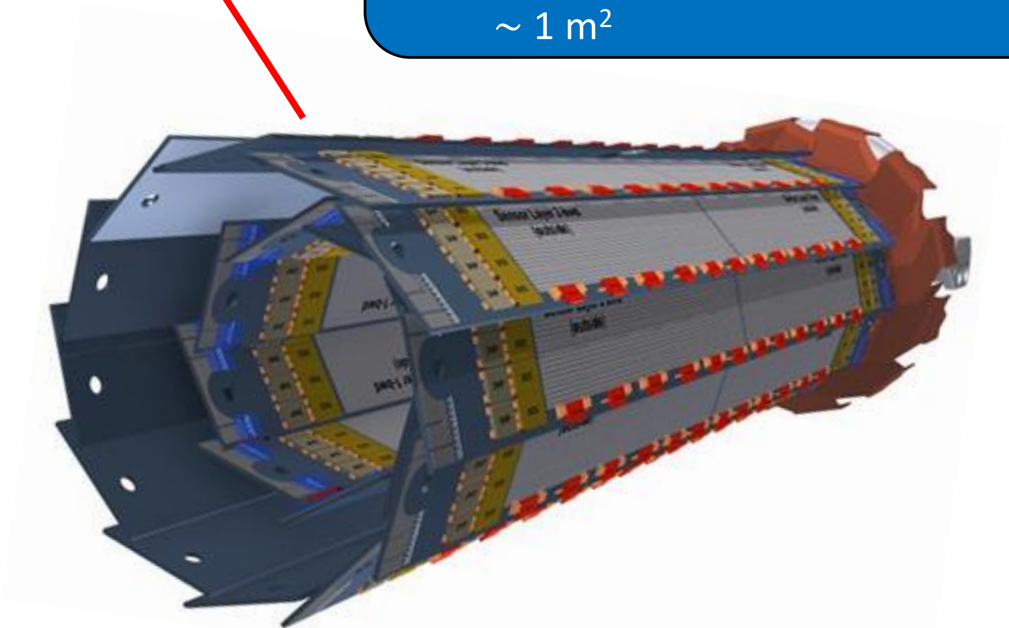


- SuperKEKB: Asymmetric energy e^+e^- collider
  $E_{cm} = m(\Upsilon(4S)) = 10.58$ GeV
- Peak luminosity: $\mathscr{L} = 6 \cdot 10^{35}$ cm^{-2} s^{-1} (x30 than KEKB)
  Beam size reduction. Higher current (x2 higher).

Belle II Vertex Detector

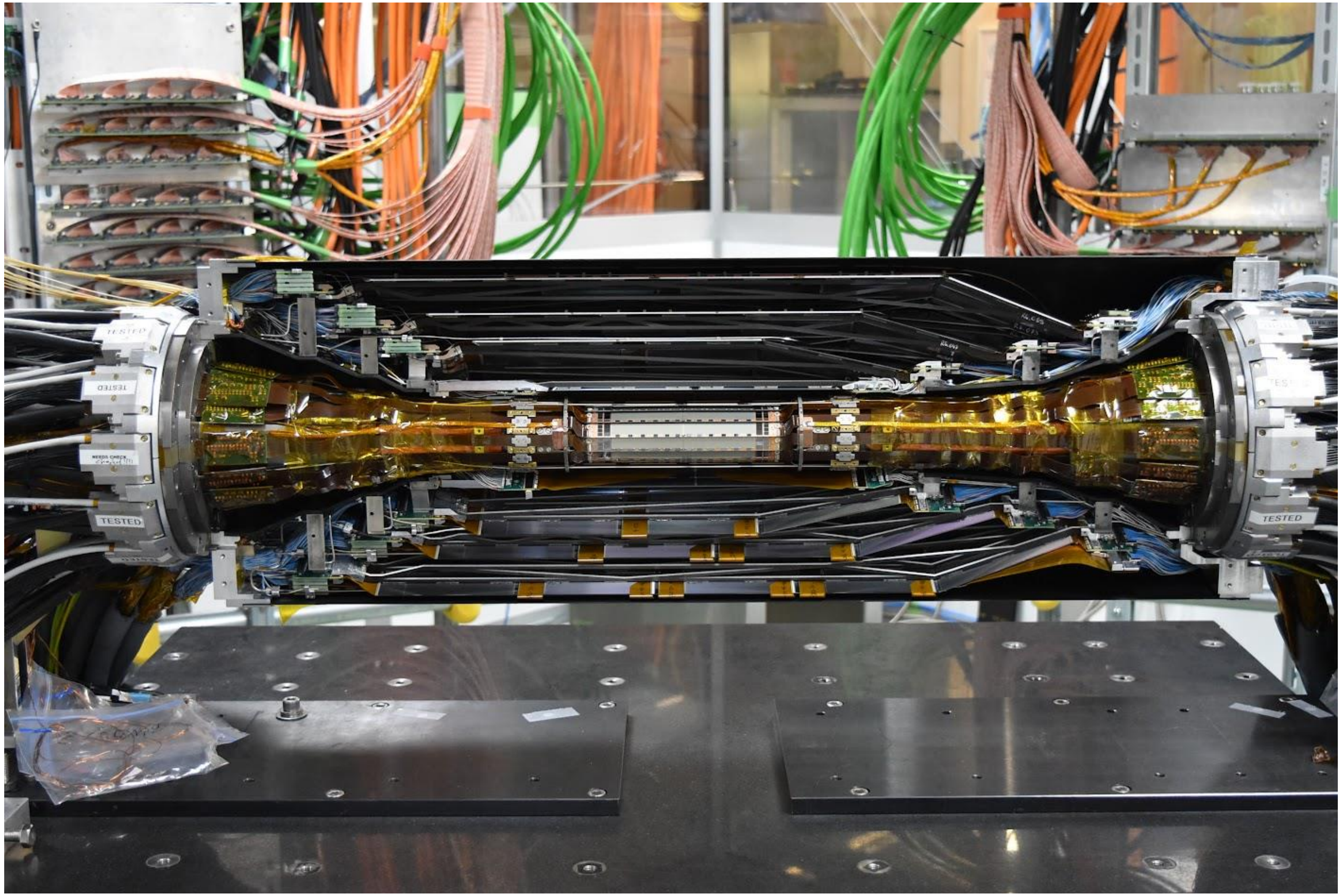


- **Silicon Vertex Detector (SVD)**
  4 layers of DSSD
  r = 3.9 cm, 8.0 cm, 10.5 cm, 13.5 cm
  L = 60 cm
  ~ 1 m^2

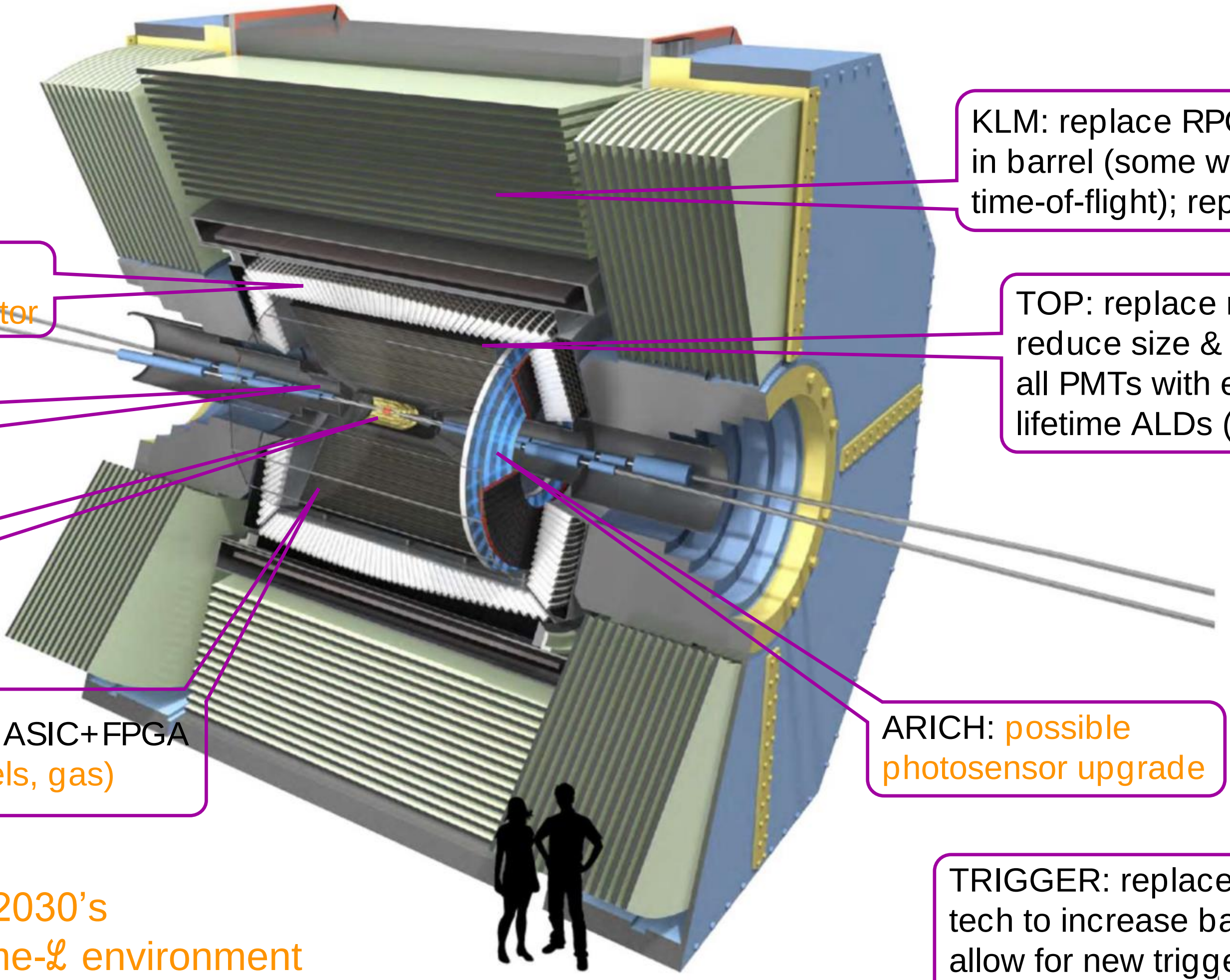


- **Pixel Detector (PXD)**
  2 layers of DEPFET pixels
  r = 1.4 cm, 2.2 cm
  L = 12 cm
  ~ 0.027 m^2

Belle II VXD



Belle II Upgrades



KLM: replace RPCs with scintillators in barrel (some with fast timing for K_L time-of-flight); replace readout

ECL: replace crystals with pure CsI; APD readout; add pre-shower detector

TOP: replace readout to reduce size & power; replace all PMTs with extended-lifetime ALDs (or SiPMs?)

IR: accommodate QCS replacement and repositioning

VXD: all pixels DMAPS

CDC: replace r/o ASIC+FPGA
New tracker (pixels, gas)

ARICH: possible photosensor upgrade

TRIGGER: replace with latest tech to increase bandwidth, allow for new trigger primitives

More distant future: ~mid-2030's
✓ Detector R&D for extreme-$\mathcal{L}$ environment

Requirements for VXD Upgrade

Upgrade motivation:

- Cope with larger background activity
- Improve momentum and impact parameter resolution in low p_T region
- Simplify tracking chain with all layers involved
- Operation without special modes nor data reduction

Key sensor specifications:

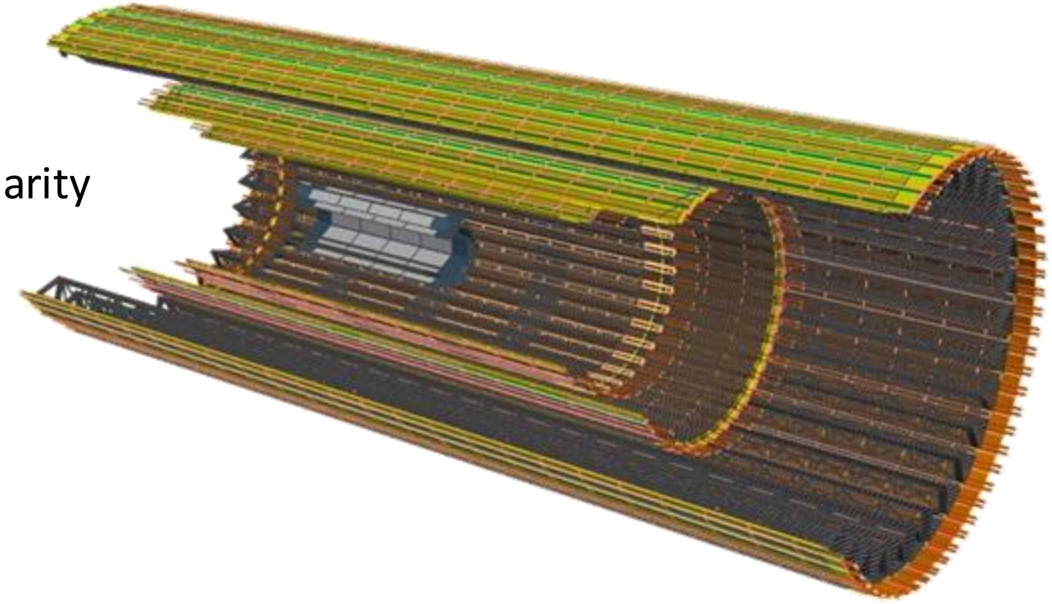
- Pixel pitch 30-40 µm
- Integration time $\lesssim$100 ns
- Power dissipation $\lesssim 200\ \mathrm{mW/cm^2}$

Improve physics reach per ab^{-1}

Radius range	14 – 135 mm
Tracking & Vertexing performance	
Single point resolution	< 15 µm
Material budget	0.2% X_0 / 0.7% X_0 inner- / outer- layer
Robustness against high radiation environment (innermost layer)	
Hit rate	~ 120 MHz/cm²
Total ionizing dose	~ 10 Mrad/year
NIEL fluence	~ 5e13 n_{eq}/cm²/year

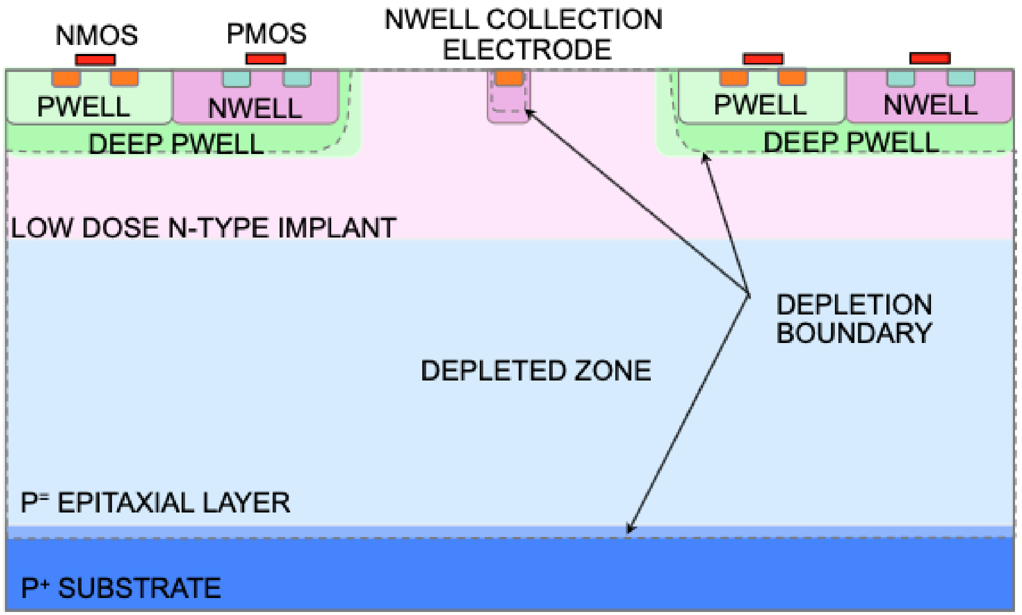
Belle II Upgrade: VTX - DMAPS

- 5 straight layers barrel, using CMOS pixel sensors
- Low material : 0.2% X_0 (L1+L2) - 0.5% (L3) - 0.8% X_0 (L4+L5)
- Moderate pixel pitch ~ 30 μm^2
- Time precision 50-100 ns
  - Option for track-triggering with a fast low-space-granularity
- iVTX: innermost 2 layers, self-supported, air cooled
- oVTX: 3 outer layers, CF structure, water cooled
- Overall service reduction and operation simplification



Small Electrode Sensor Design DMAPS

Monolithic detector: Combine sensor and readout on the same wafer



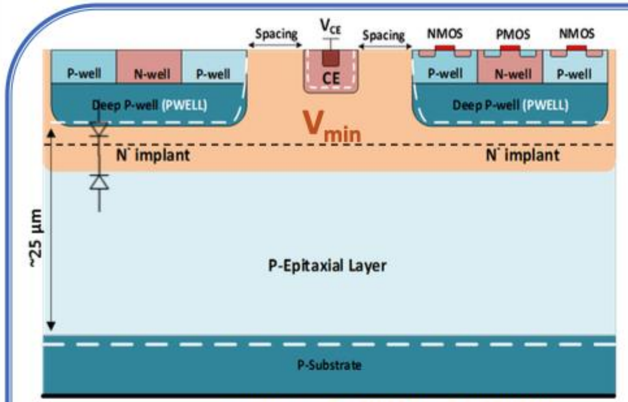
Electronics outside the collection well
Small fill factor

- Very small sensor capacitance
- Low noise and power

TowerJazz 180 nm CIS

- Deep pwell allows for full CMOS in pixel
- High resistivity epi-layer 1-8 kOhm.cm
  Epi thickness 18-40 µm
- 3 nm gate oxide for good TID
- Modified process: Additional planar n-type implant
  Full depleted volume
  Fast charge collection
- Derived from LHC developments

TJ-Monopix Family



W. Snoeys et al. https://doi.org/10.1016/j.nima.2017.07.046

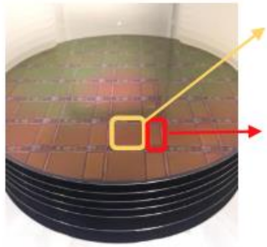
$C_d \leq 3fF$

$P \approx \frac{S}{N} \approx \frac{Q}{C_d}$

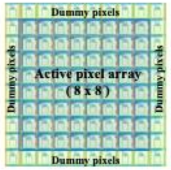
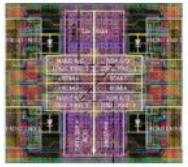
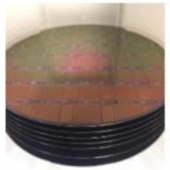
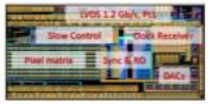
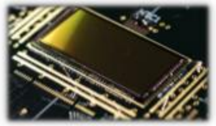
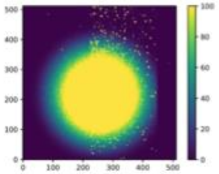
DMAPS in TJ 180 nm: Concept

- Small sensor capacitance (Cd)
  - Key for low power/low noise
- Radiation tolerance challenges
  - Modified process
  - Small pixel size
- Design challenges
  - Compact, low power FE
  - Compact, efficient R/O

Large scale demonstrator chip development

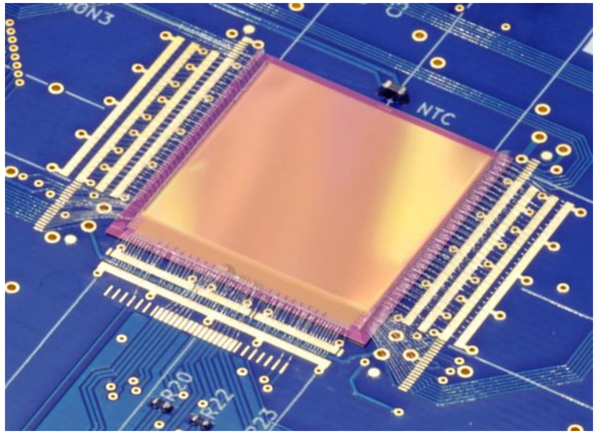


- MALTA
  - Asynchronous readout
- TJ-Monopix1
  - Synchronous column-drain R/O
- Process modification enhancements, Cz substrate ⟹ improved efficiency
- TJ-Monopix2: Improved full-scale DMAPS

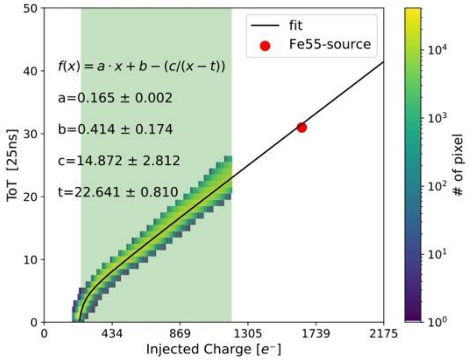
TJ-Investigator characterization	*TJ-Monopix1* & MALTA Design	*TJ-Monopix1* & MALTA Submission	Mini-MALTA sub. with process fixes	*TJ-Monopix1* resub. process fixes & Cz	*TJ-Monopix2* & MALTA2 Design	*TJ-Monopix2* & MALTA2 Submission	*TJ-Monopix2* Characteriza tion	*"OBELIX"* Design
								Full scale System-ready: LDO, CDR, memory etc.
Q2 2016	Q4/2016	Q3/2017	Q3/2018	Q2/2019	Q2/2019	Q3/2020	Present	~~Future plans~~ Present

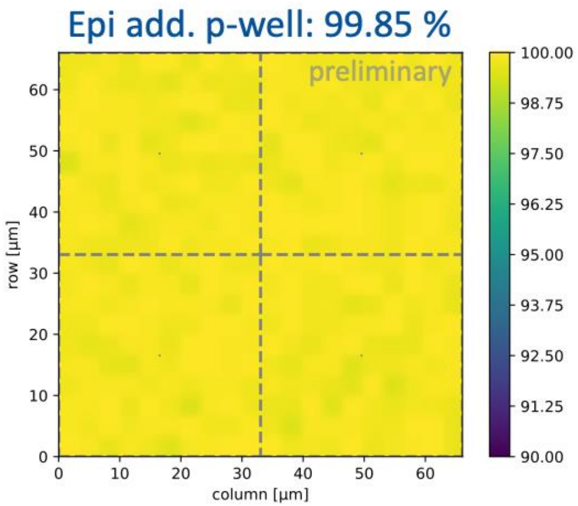
TJ-Monopix2 Characterization

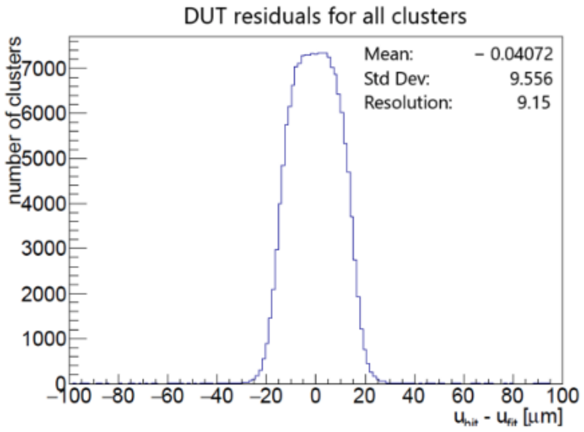
- TJ-Monopix2 as forerunner of OBELIX
  - 33x33 μm^2 pitch, 25 ns integration, 2x2 cm^2 matrix
  - 7 bit ToT information, 3 bit in-pixel threshold tuning
  - Various sensing volume thickness (CZ-bulk, epi-30 μm)



- Detailed characterisation
  - In-laboratory
    - Threshold / noise
    - ToT calibration
  - In-beam (DESY, 5 GeV electrons)
    - Efficiency ~99%
    - Position resolution ~9 μm







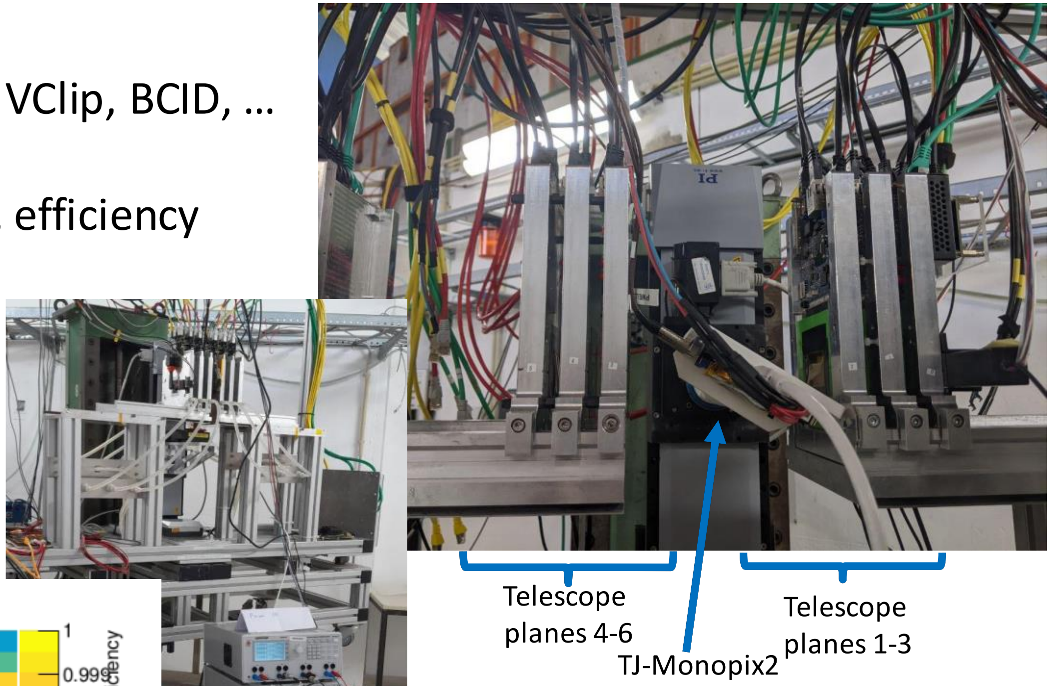
Irradiated TJ-Monopix2 Test Beam

Serial	Irradiation	Substrate
W02R05	None	30 µm EPI
W02R09	Neutrons 1 × [illegible]	30 µm EPI
W05R16	Protons 5 × [illegible]	30 µm EPI
W08R19	None	30 µm EPI
W14R12	None	Cz

Parameter scans:

HV, IBias, PSub, VClip, BCID, …

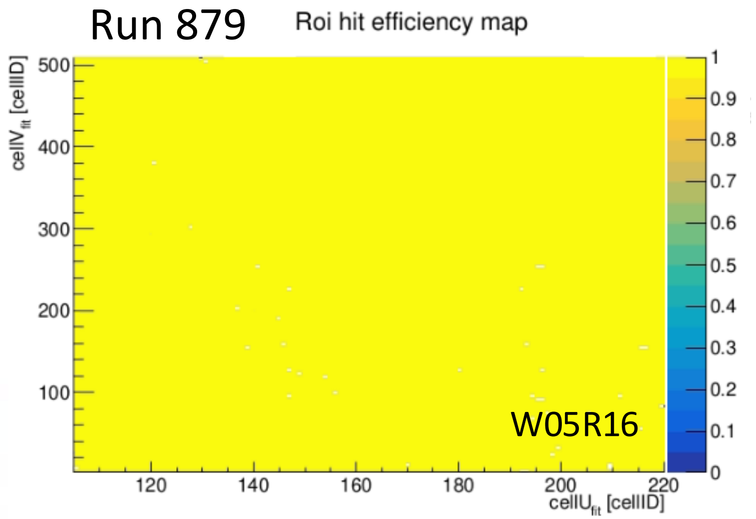
Angular scans, resolution, efficiency

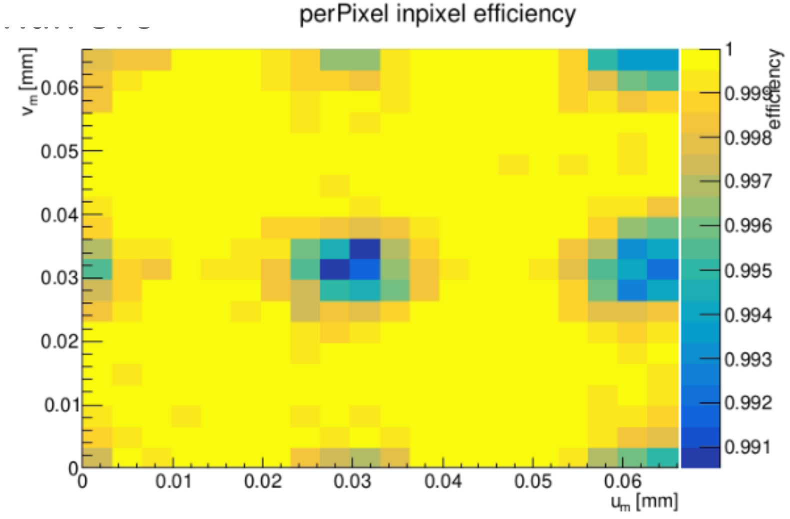


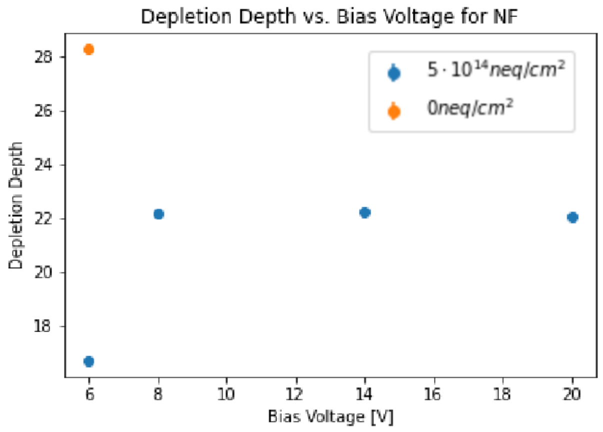
Efficiency >99% for 5×10^{14} n_{eq}/cm^2 (310 e^- threshold)

Cluster position residuals ~9.5 µm

Run 879







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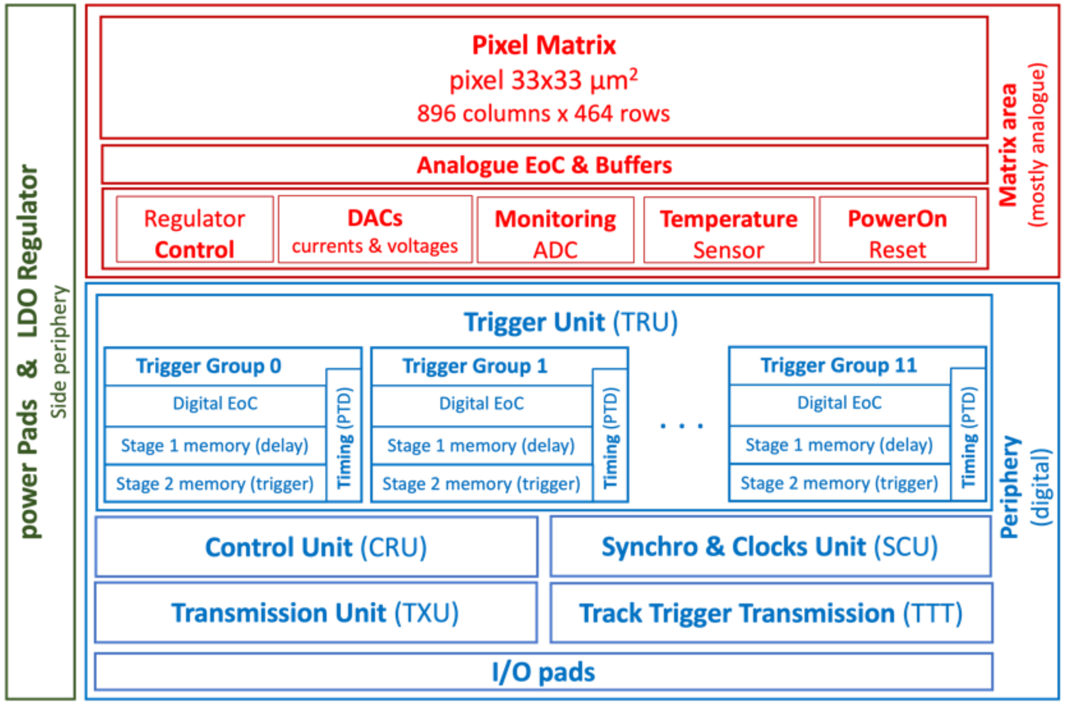
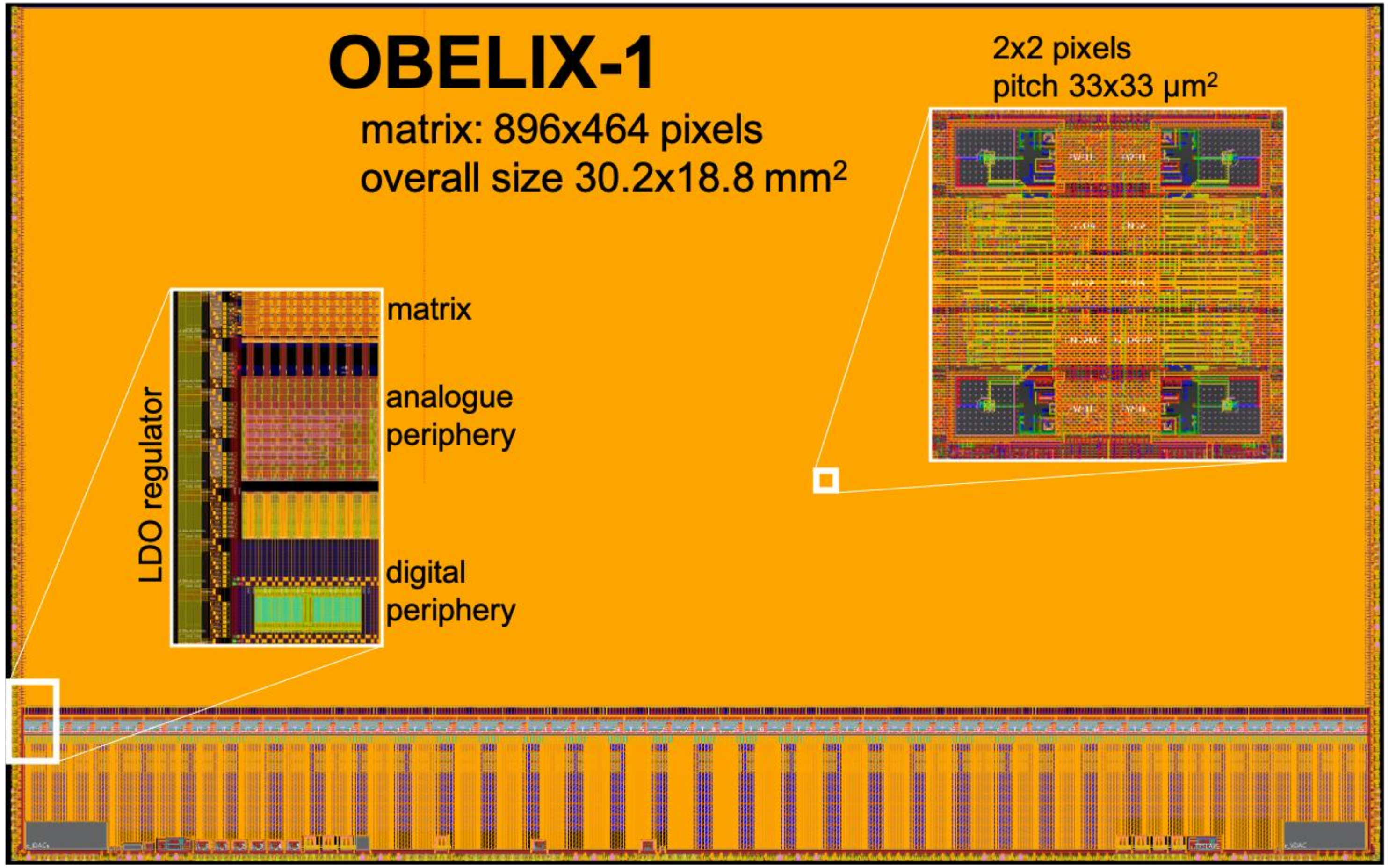
OBELIX Design

- Matrix design
  - Extended copy of TJ-Monopix2
  - 2 front-end flavours: **DC- and AC- cascode amplifier**
  - Clock for time-binning slowed down: 100ns
- Powering
  - LDO regulator for easier voltage distribution
  - Overall power depends on hit rate: 200-300 mW/cm^2
- Trigger Unit
  - Simulated with realistic inputs: 120 MHz/cm^2
  - Can sustain 600 MHz/cm^2 for 0.5 µs
- Fine time stamping
  - 6 ns achievable with end-of-column fast clock
    - Limited to hit rate $\lesssim$ 10 MHz/cm^2
- Track trigger
  - Reduced granularity to 8 strixels (~4 x18 mm^2)
  - Increased transmission rate: 33 MHz



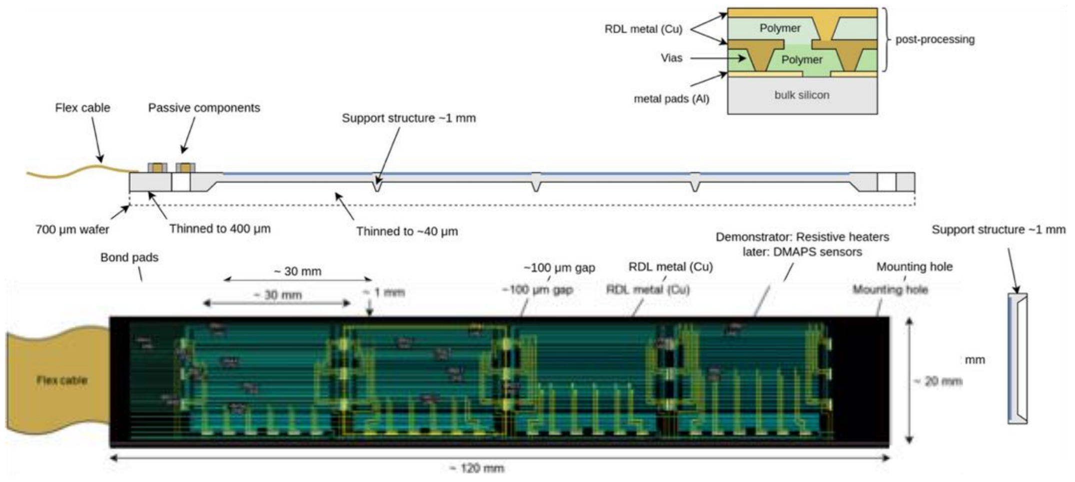
OBELIX Layout

Pitch	33 µm
Signal ToT	7 bits
Integration time	50 To 100 ns
Time stamping	~5 ns for hit rate < 10 MHz/cm^2
Hit rate max for 100% eff.	120 MHz/cm^2
Trigger handling	30 KHz with 10 µs delay
Trigger output	~30 ns resolution with low granularity
Power (with hit rate)	120 to 200 mW/cm^2 (1 to 120 MHz/cm2)
Bandwidth	1 output 320 MHz



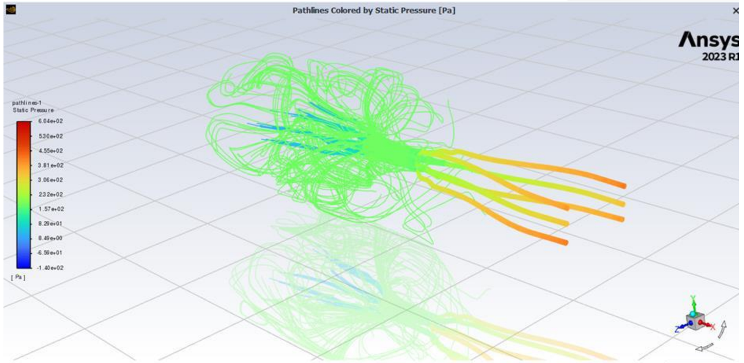
iVTX Inner Layer Concept

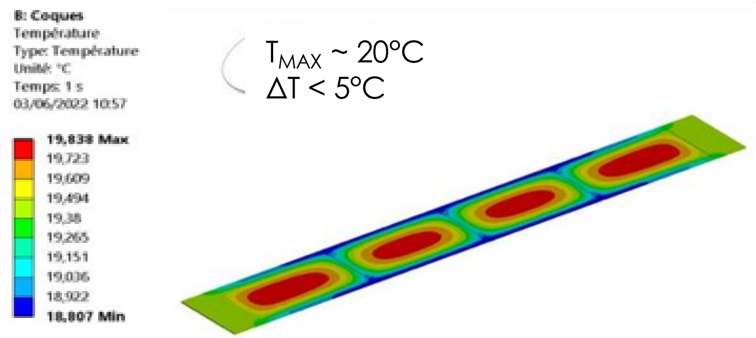
- All-silicon module < 0.15 % X_0
  - 4 contiguous sensors diced as a block from the wafer
  - Redistribution layer for interconnection
  - Heterogeneous thinning for thinness & stiffness



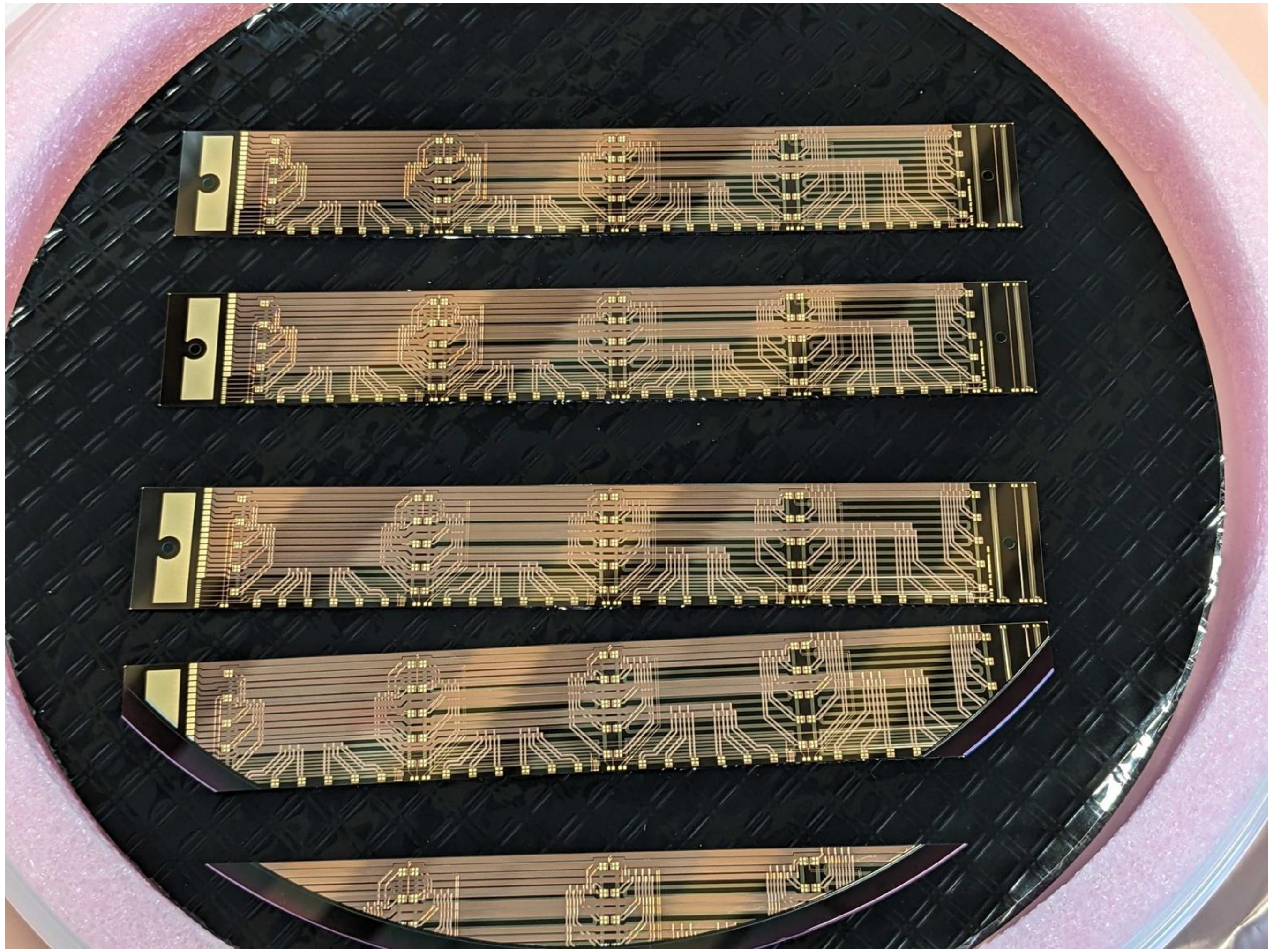
- Prototyping
  - First real-size ladders at IZM-Berlin with dummy Si
    - True iVTX geometry available

- Simulation on cooling
  - Dry air cooling 15^{o}C
  - Assume 200 mW/cm^2





iVTX Ladder Demonstrator



- Production finished smoothly:

  FE-I3 and heaters
  300 – 700 um thick

- Characterization started:

  First quality inspection with needles shows resistivity is on the expected range.

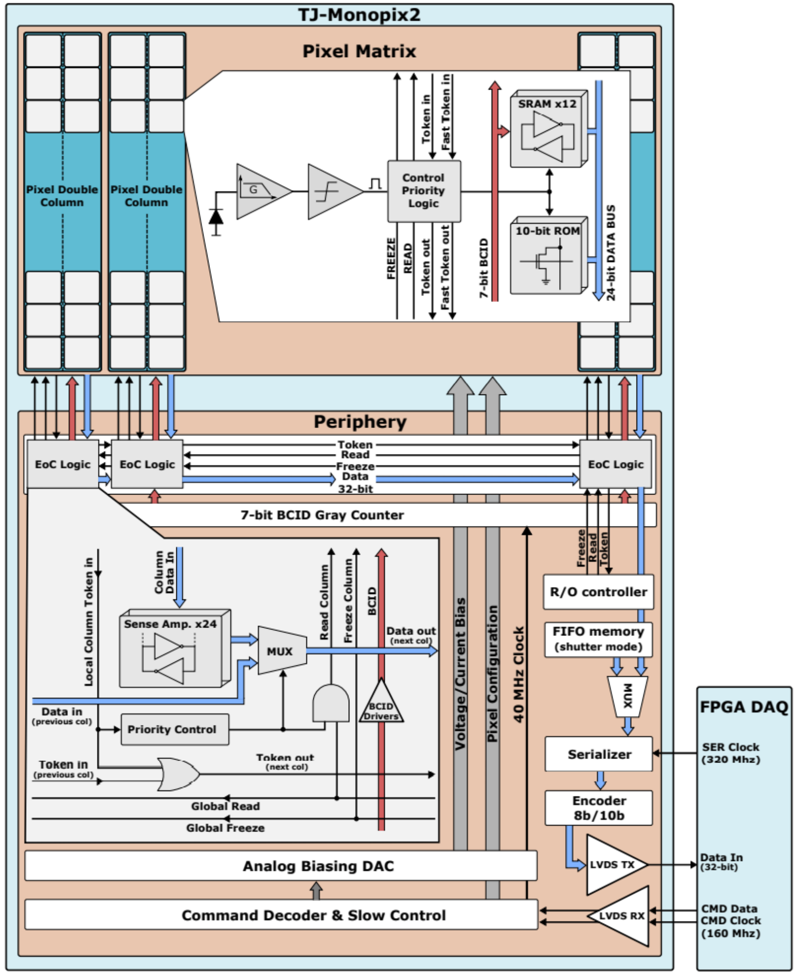
  Integrity of data lanes will follow

Summary: Belle II VXD Upgrade Plans

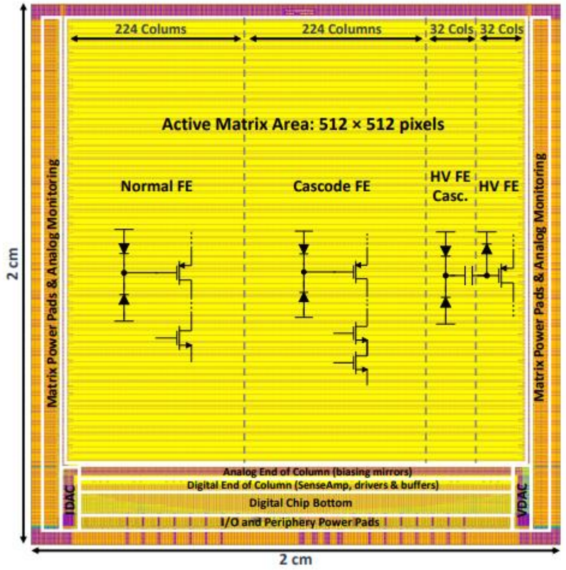
- *Vertex detector*: Plans to replace VXD with a fully pixelated CMOS detector (VTX)
  - TJ-Monopix2 performance, including irradiated devices, matches expectations
    → Solid steppingstone towards OBELIX, to be submitted in 2025
  - Complete ladder demonstrators available, including its test stands
  - Preparing the next big step: **TDR**

THANK YOU

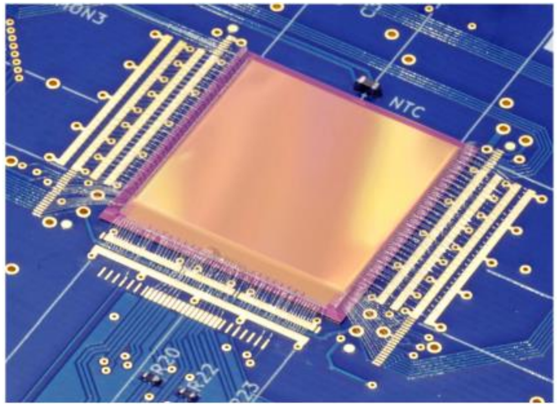
TJ-Monopix2 as Prototype



Chip architecture of TJMP2



Layout of TJMP2 sensor: divided in 4 regions with different FE



TJM2 sensor bonded on a test board

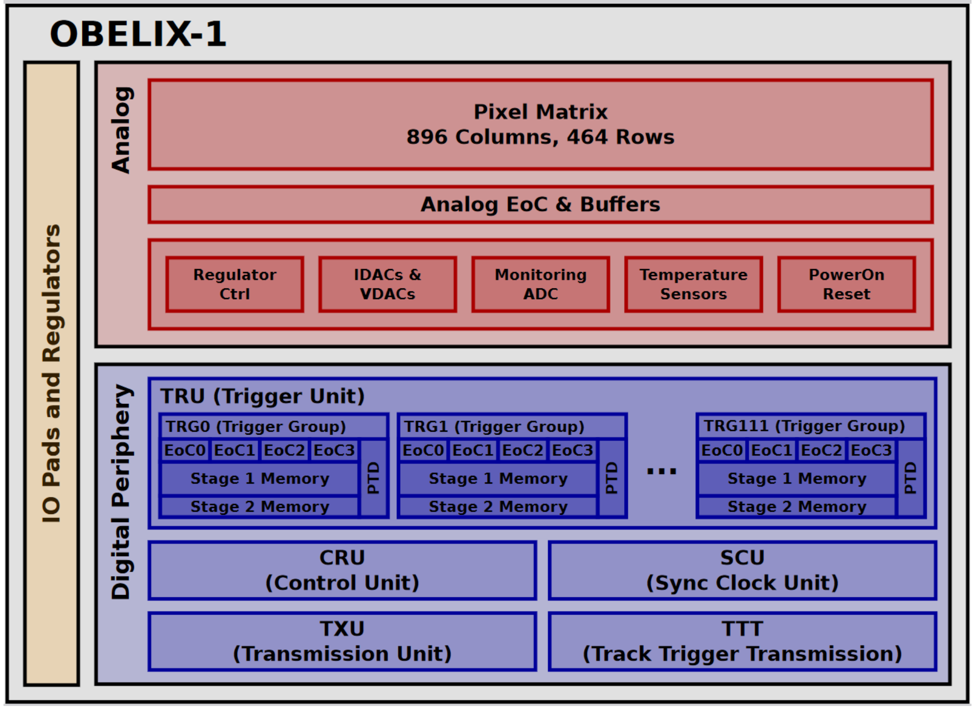
- Developed for ATLAS experiment
  - FE derived from ALPIDE
  - 4 FE flavors with differences in the amplifier and detector input coupling (AC or DC)
  - Column-drain R/O architecture

- DMAPS **Tower Semiconductor 180 nm CMOS**
- 2×2 cm² chip: 512×512 pixels
- Pixel pitch: 33.04×33.04 µm²

- Expected from design (simulations):
  - ~ 100 e− min threshold
  - 5-10 e− threshold dispersion (tuned)
  - >97% efficiency at $10^{15}\ n_{eq}$/cm²
  - ~ 5 e− noise
  - Fully efficient with hit rate 120 MHz/cm²
  - Power: ~ 1 µW/pixel

Base-line option for OBELIX design

OBELIX Block Diagram



Digital Periphery

- Main clk-in: 170MHz
- New end-of-column adapted to Belle II trigger
- Timestamped hits stored in memories
- Read-out when timestamp matched with trigger
- Single output at 340 MHz average bandwidth
- RD53 control/readout protocol

Power pads

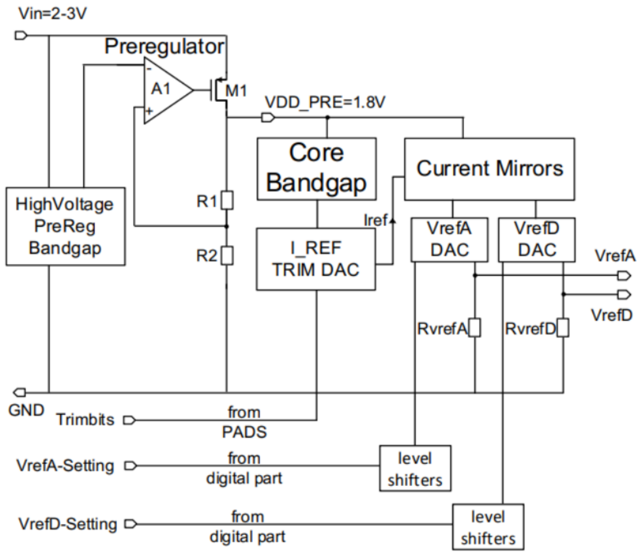
- Power regulators
- Simplified system integration

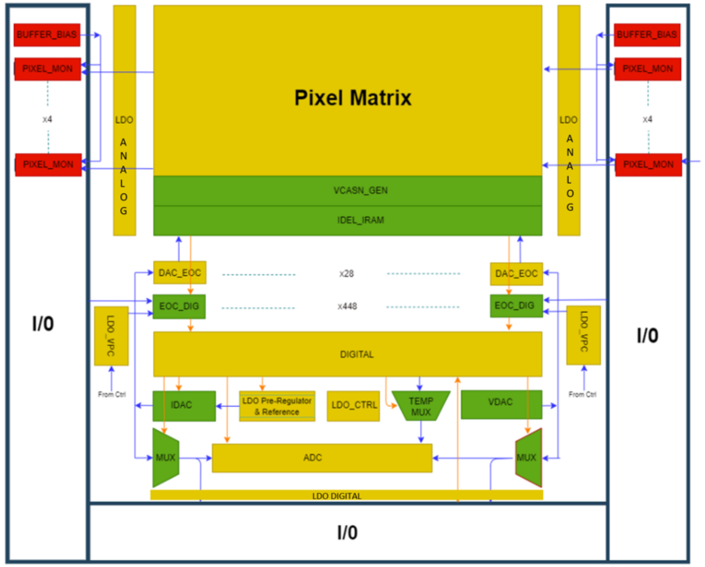
Analog

- Pixel matrix adapted from **TJMP2**
- Column drain architecture
- Monitoring ADC
- Temperature sensors

- **Based on current characterisation and simulation results, 2 FE flavors are chosen for OBELIX on equal area:**
  - **Cascode FE (DC)**
  - **HV Cascode FE (AC)**

OBELIX Power Management

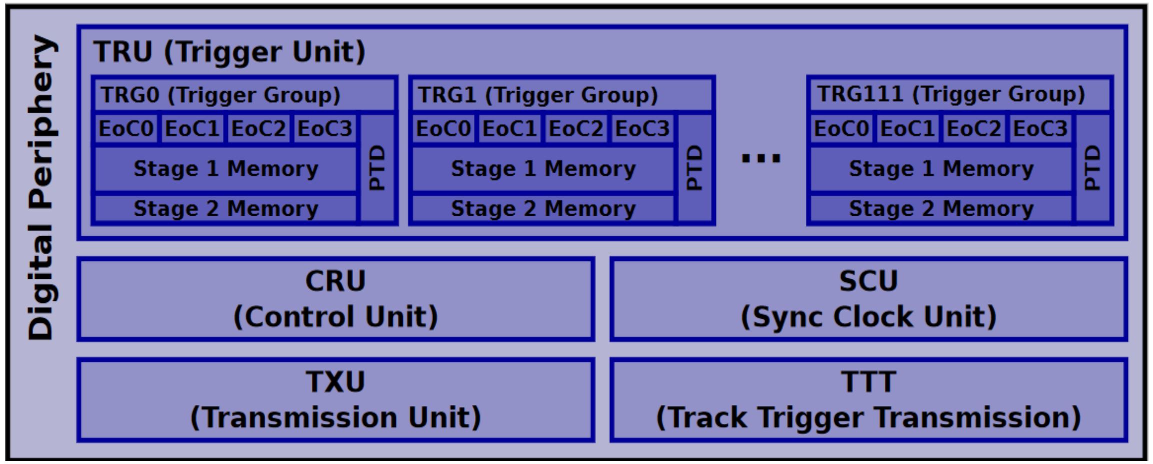


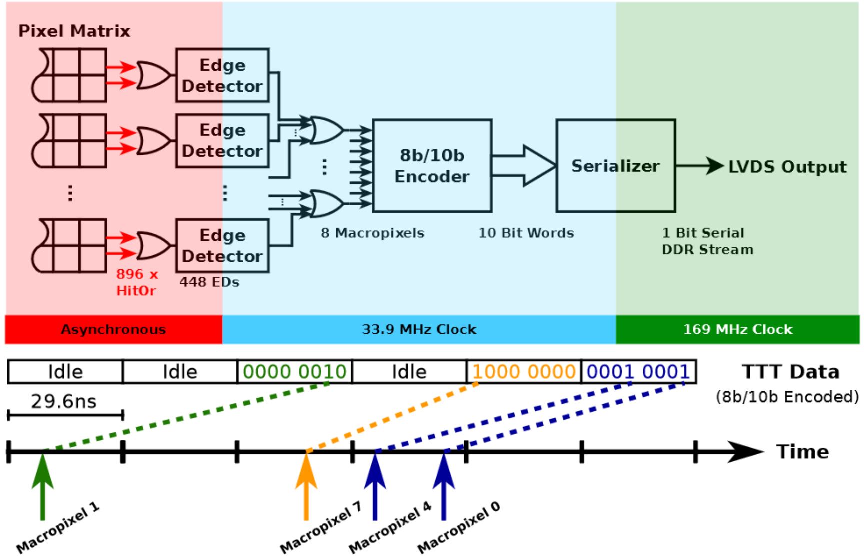


- Power distribution is a major concern as OBELIX is larger than TJMP2, leading to performance degradation
- Long linear ladders voltage drop across ladder
- On chip regulators are developed to compensate the voltage drop and simplify the power distribution
  - Two analog **LDO (Low Dropout)** regulators to supply the matrix from both sides
  - A digital LDO in the bottom of the chip to supply the digital blocs
  - A preregulator to supply LDO references generator
  - A VPC (Voltage pre-charge) LDO to reset and recharge bit-lines between each read cycle
- The LDO generates the output voltage of 1.8 V (+ 10%, -20%) necessary for the technology to power the chip
- Wide input supply voltage range of 2-3 V

OBELIX Digital Periphery

- Module division: 5 main parts with new modules related to the Belle II trigger
  - **TRU - Trigger Unit:** Manage pixel data from the matrix-EOC and wait for the trigger to pick them for output
    - PTD - Periphery Time to Digital : Precision timing feature → 5ns for hit rate < 10 MHz/cm^2 (enabled via configuration)
  - **CRU - Control Unit:** Implement RD53B interface, command decoder and global configuration
  - **SCU - Sync Clock Unit:** Synchronize circuit and clk divider , Rx_data SIPO synchronization
  - **TXU - Transmission Unit:** Generate output data and sequential output, data framing, serializer
  - **TTT - The Track Trigger Transmission:** Provide coarse and rapid information to the Belle II trigger system





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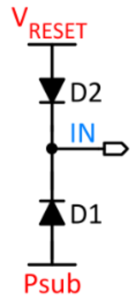
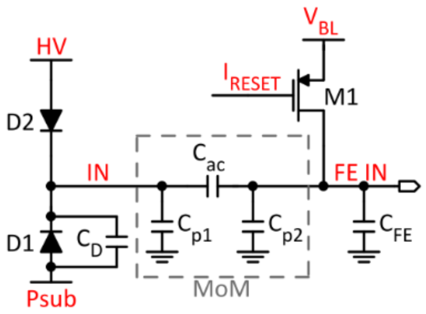
Analog FrontEnd Design

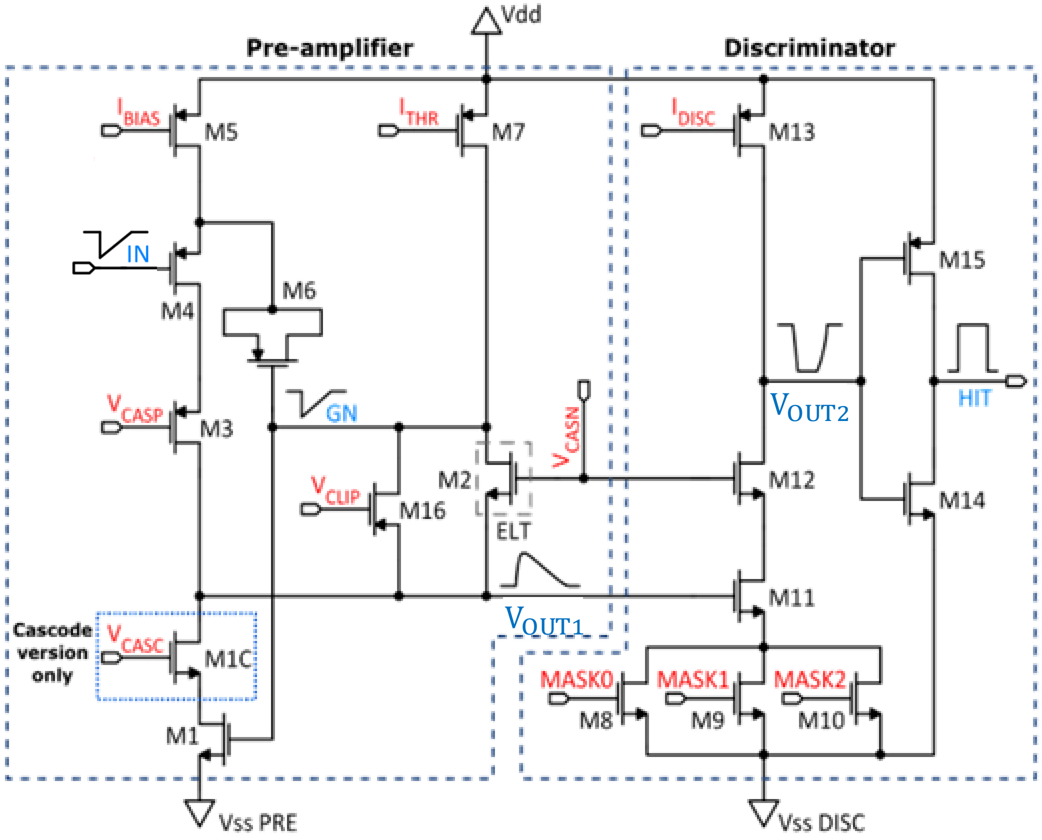
- Two flavors with a cascode pre-amplifier :
  - With an input **DC-coupling** using a forward biased diode **(Cascode FE)**
  - With an input **AC-coupling** allowing higher bias voltage above 30V (**HV Cascode FE)**



Input DC-coupling

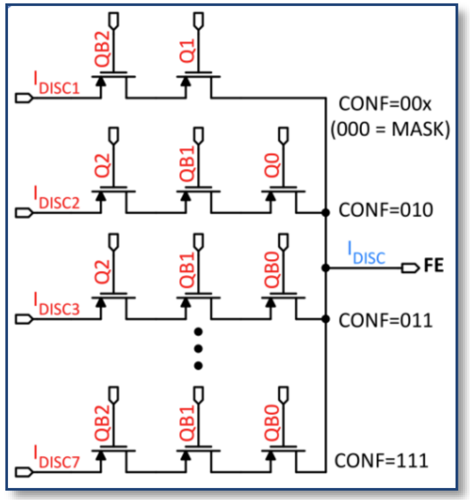


Input AC-coupling



Individual pixel masking

3-bit Threshold Tuning DAC



- A 3 bit threshold tuning is available at the pixel level to reduce the threshold dispersion

OBELIX – Layout

- Matrix inherited from TJ-Monopix2 developed for ATLAS (Tower 180 nm CIS)
- Dimensions adjusted to VTX geometry
  464 rows and 896 columns, 29.60 x 15.33 mm^2 active area
- Low dropout regulators (LDOs) to allow a wide input supply voltage range 2-3 V
- Clock frequency for the timestamp and trigger unit is 21.2 MHz (timestamp length 47.2 ns)
- Trigger unit with 2-stage trigger memory (data loss < 0.02% at design trigger latency of 10 µs and hit rate of 120 MHz/cm^2
- 320 Mbit/s output