Novel Timing and Synchronization Trends for Particle Detectors

Experience with White Rabbit IEEE1588-2019 Spanning from Accelerators to Future Detectors

Javier Galindo on behalf of IFCA, IMB-CNM and ITA Teams

XVI CPAN Days, Madrid, Nov. 19th 2024

-High-lum colliders, tomography…

-Tracker, Timing detectors…

-Picosecond-level accuracy

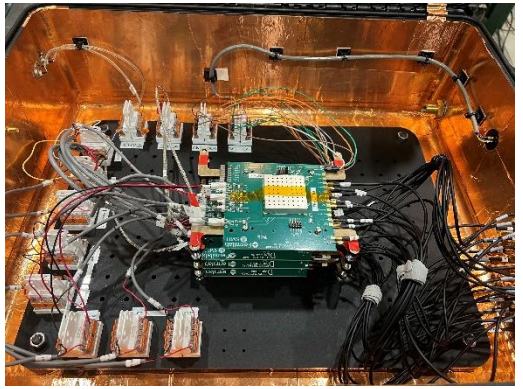
-Reference/detection planes

-Synchro. measurements

-Stable absolute notion of time

Projects; CMS-ETL, DRD7, TOMULGAD-4D, PROTECT..

4D Detector Prototype based on LGAD sensors and ETROC2



Instrumentation: Timing and Synchronization

-Scalable timing/clocking distribution system

-Self calibrating and mitigating perturbations

-Using as Commercial Off-The-Shelf (COTS)

White Rabbit COLLABORATION

High Accuracy Default PTP Profile of IEEE1588-2019

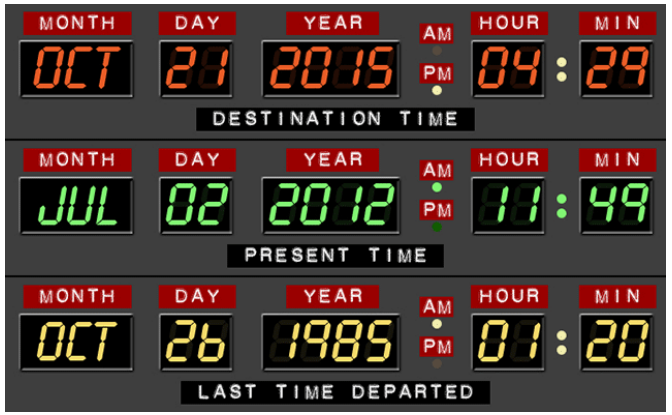
Experience And Efforts With WR Technology

Preliminary Results Performance And Usability

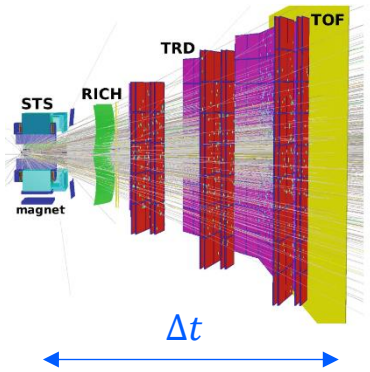
IFCA cnm ita

Timing: The need for a Reference

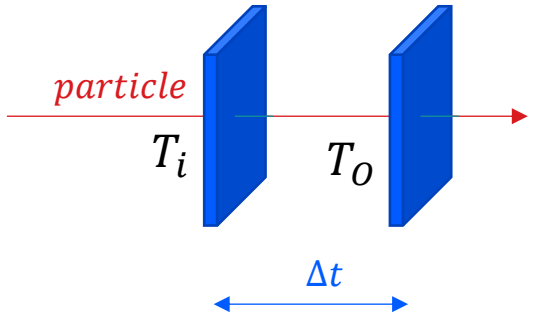
When talking about time
we usually refer to a
Time Difference
$\Delta t = T_o - T_i$



Colliders



Multiple plane detectors

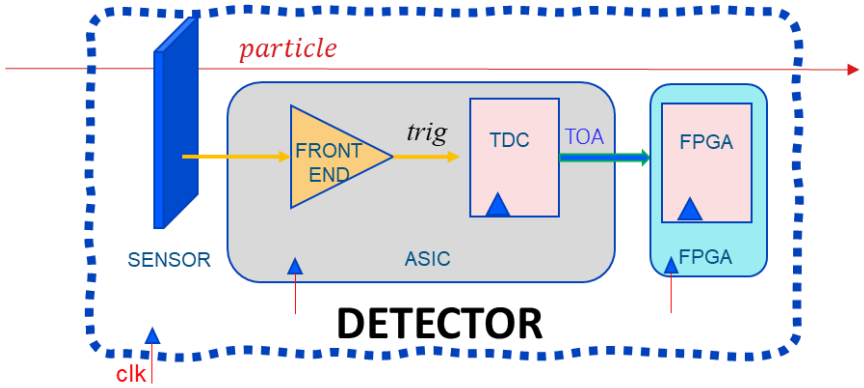


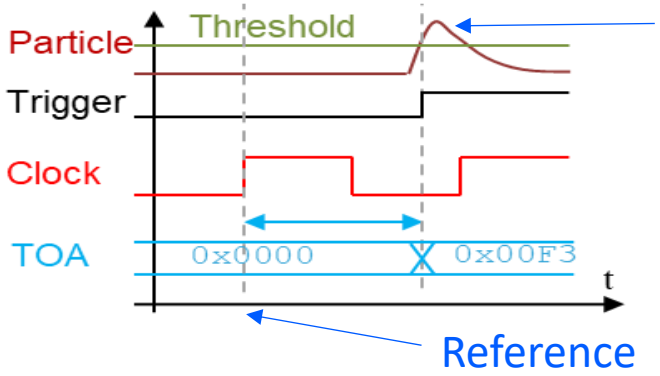
Absolute notion of time

Both times T_o and T_i
need a common
REFERENCE

A bit of background on 4D timing detectors

The Reference; the Synchronization problem



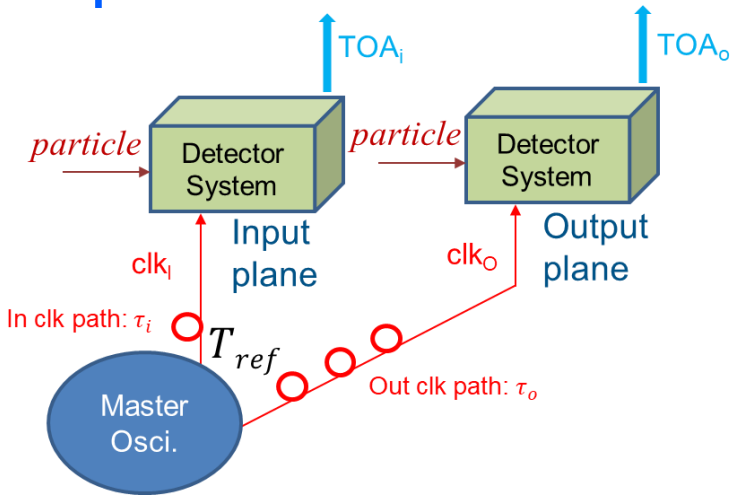


Particle crossing detector

T_{ref} needs to be a common synchronized reference among all nodes

$T_x = T_{ref\,x} + TOA_x$

Multiple Planes

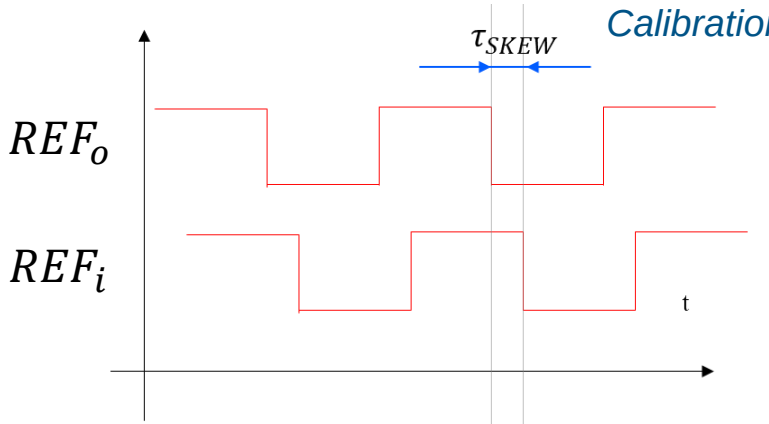


Absolute time concept: T_{ref} / clock phase identical across the entire system

Reality….

SKEW

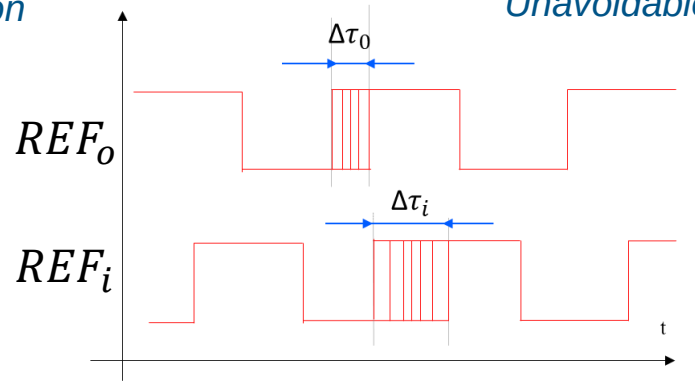
Calibration



$$\tau_{SKEW} = (T_{refo} - T_{refi})$$

JITTER

Unavoidable



$$\Delta\tau_{jitter} = (\Delta\tau_0 - \Delta\tau_i)$$

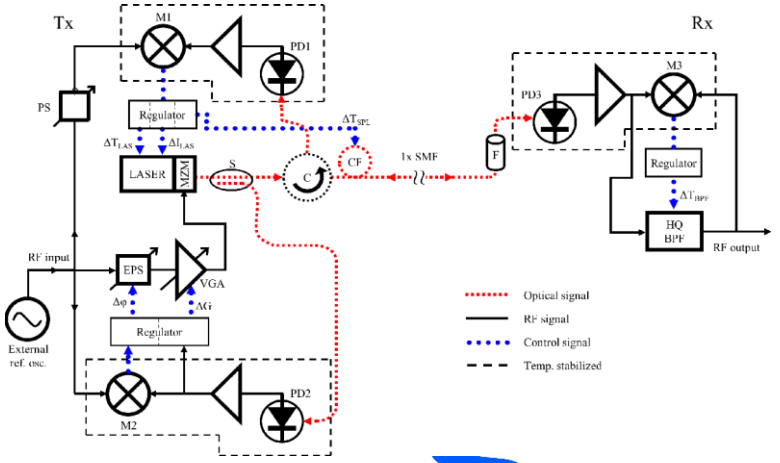
A bit of background on 4D timing detectors

The Local Oscillator and Distribution Network

Master Oscillator

Perturbation Compensated Network: fiber, coax…

Initially “Open loop” idea that turned
a complex “Closed Loop” system



High Accuracy Default PTP Profile of IEEE1588-2019

White Rabbit

CERN

Based on

- Gigabit Ethernet over fibre
- IEEE 1588 Precision Time Protocol

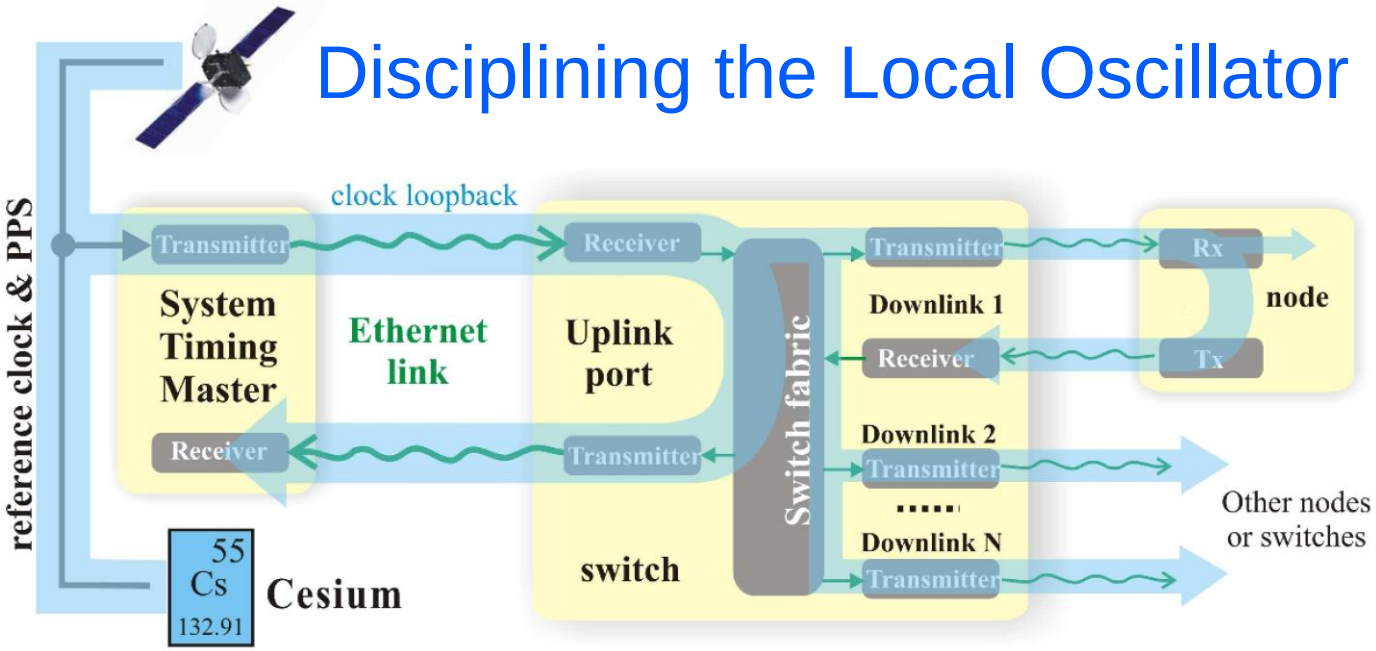
Enhanced with

- Layer 1 syntonisation
- Digital Dual Mixer Time Difference (DDMTD)
- Link delay model

“Closed Loop” system dealing with timing and synchronization from the beginning

White Rabbit Principles

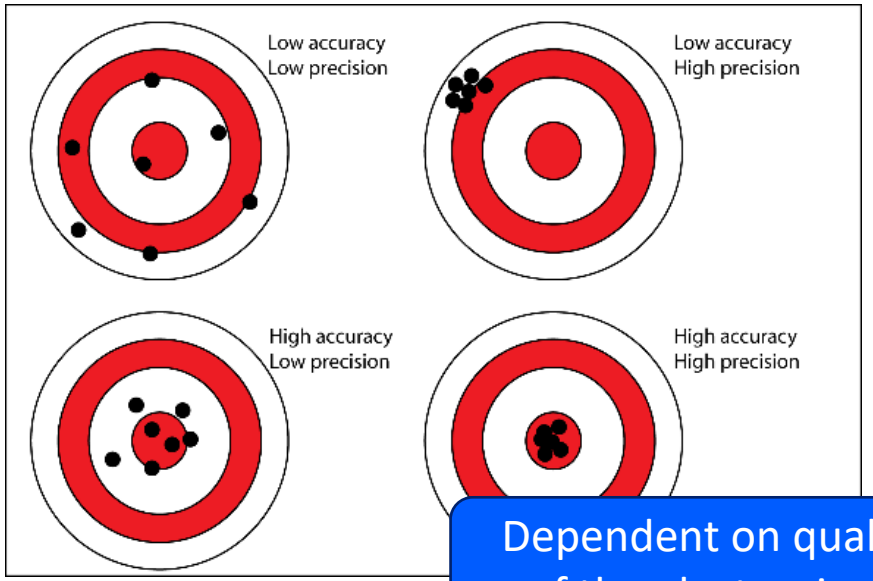
Disciplining the Local Oscillator



Clocking Performance

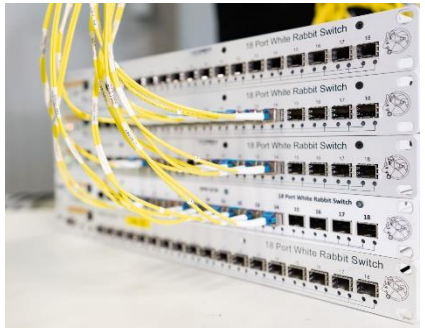
Accuracy: repeatability of the reference edge in the slaves with respect to an ideal master (skew)

Precision: dispersion of reference edge (jitter)

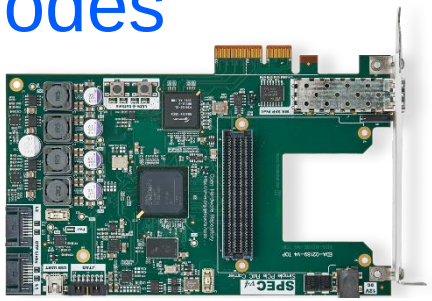


Dependent on quality of the electronics…

WR Switches



Nodes



Hardware; Carrier, FMC

Gateware; WR PTP Core

Firmware; Controls C code

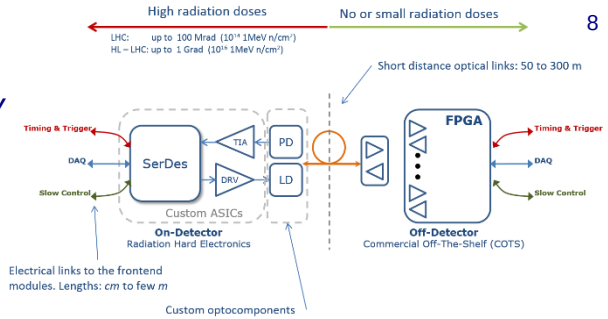
And now…
Our 4D Detector

Base on ETROC2 and…

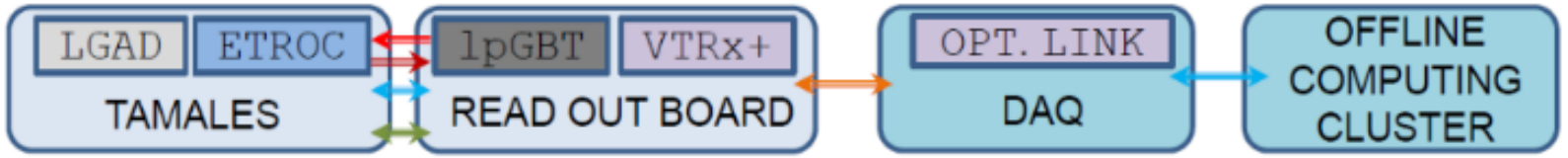
White Rabbit

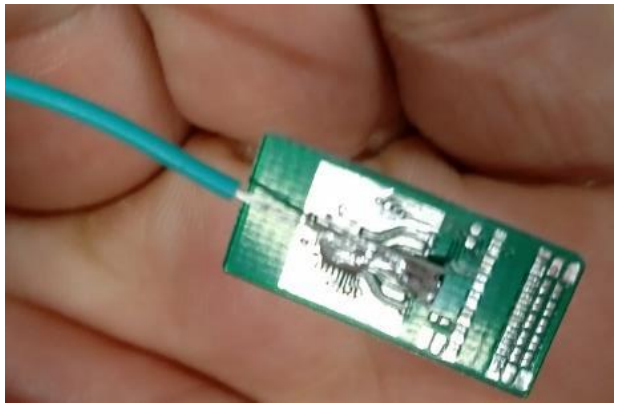
The ETROC2 Based Electronics…

CERN GBT and VTR ASIC Family



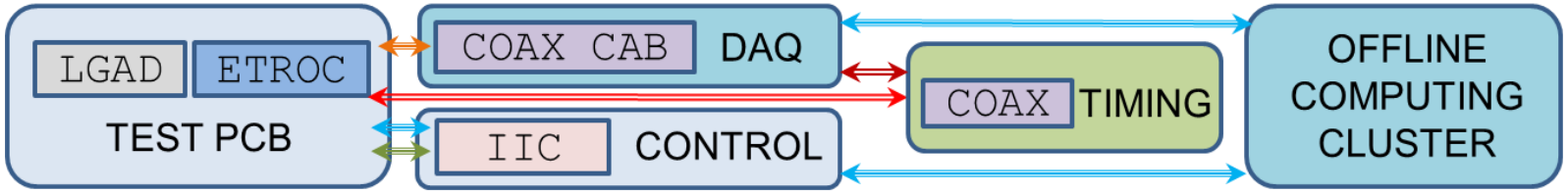
CMS – ETL Electronics

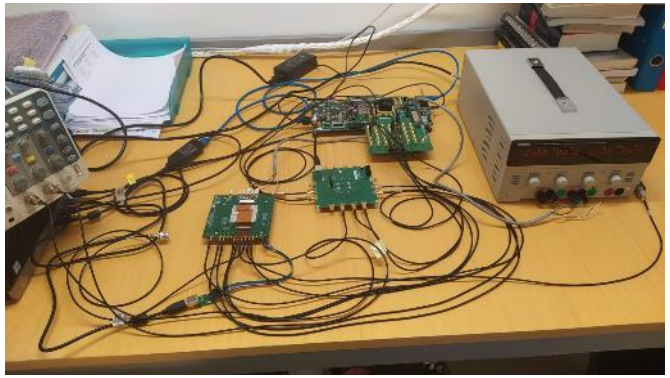




Based on CERN GBT ASICs (optical data/clock link)

TOMULGAD-4D Electronics

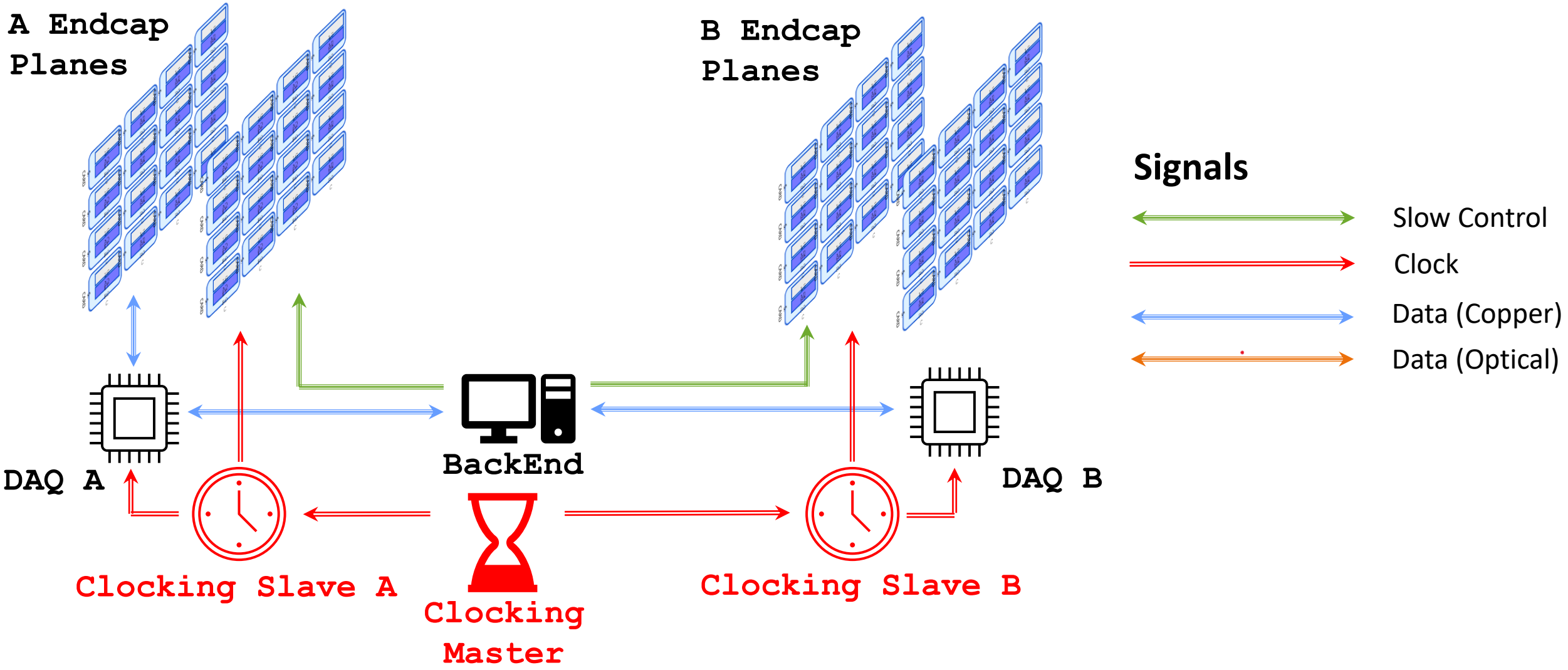




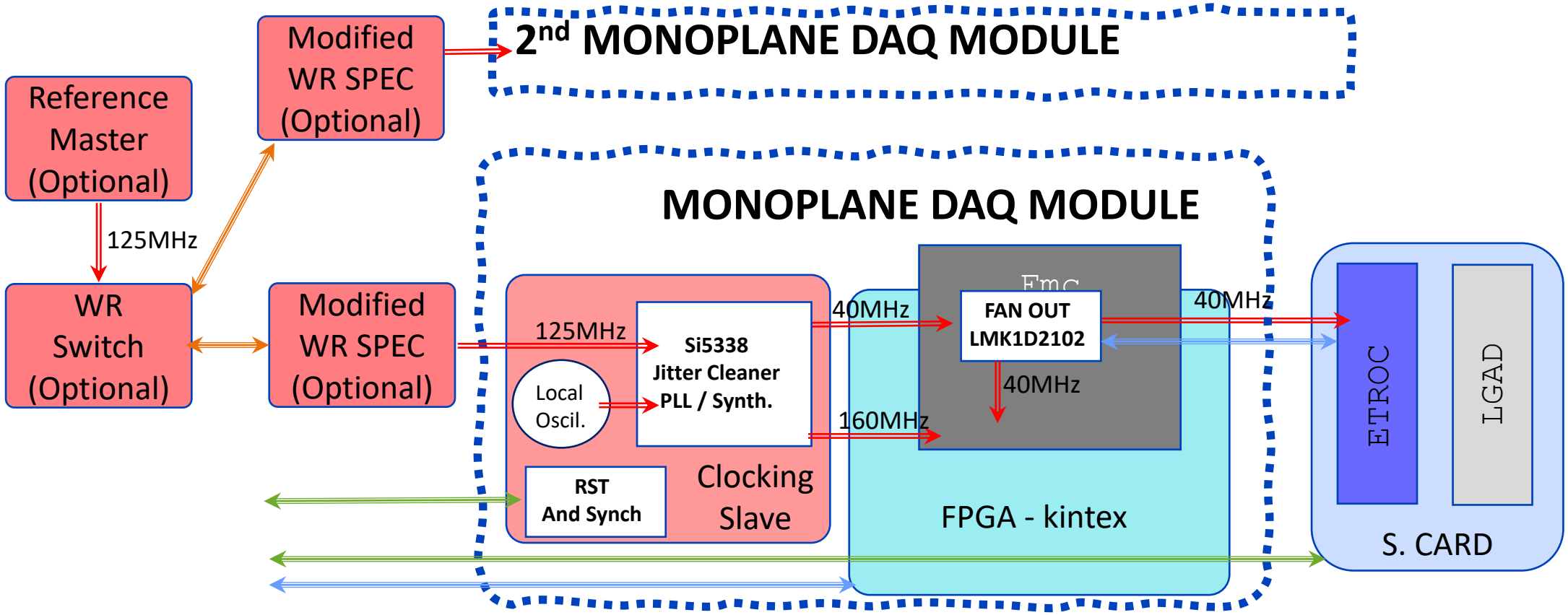
No access to GBTs… we decouple data, clocking, controls

↔ clocking ↔ controls ⇄ data

The Multiplane Detector Architecture



The WR based Planes



Signals

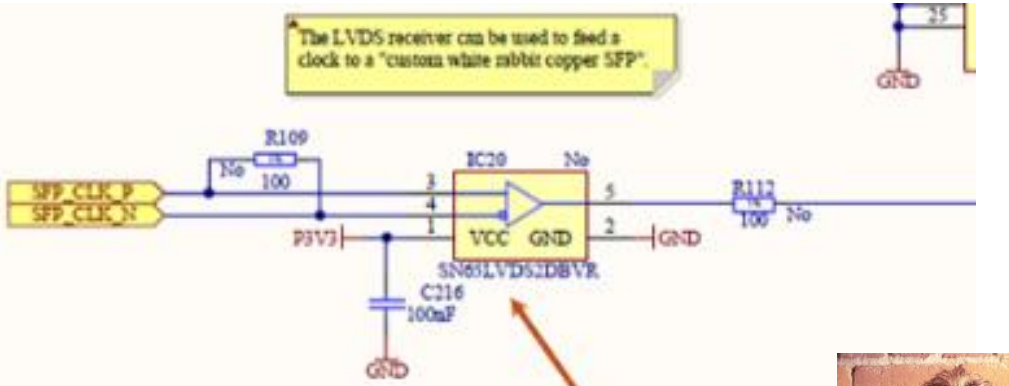
Slow Control

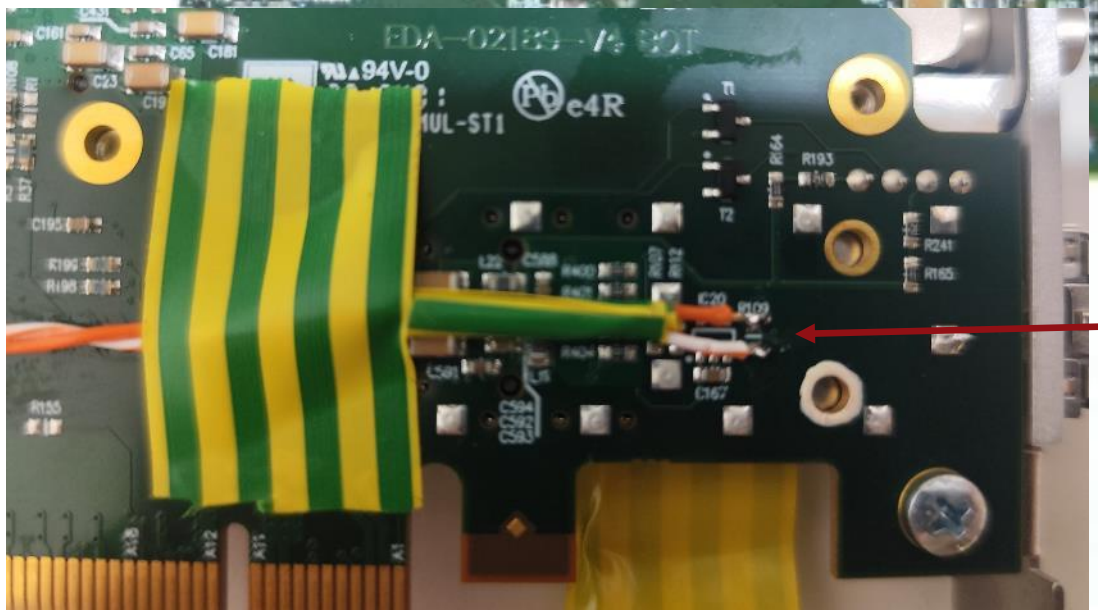
Clock

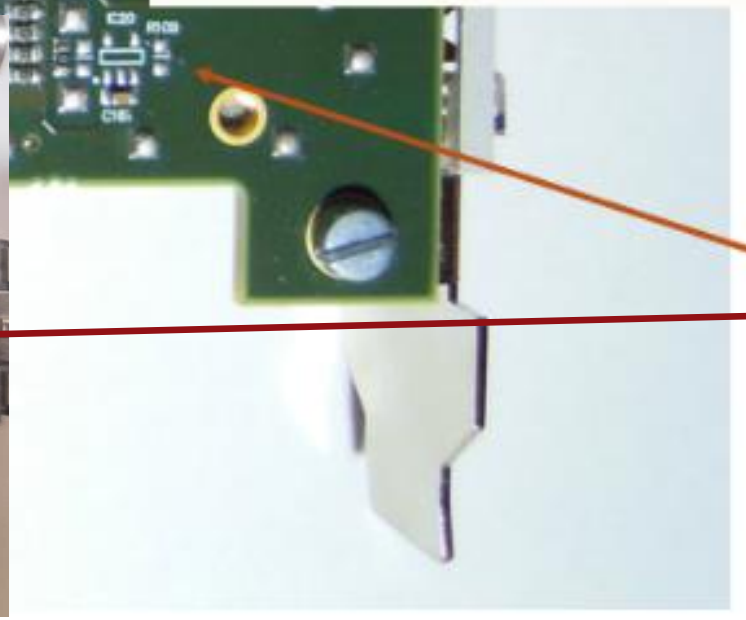
Data (Copper)

Data (Optical)

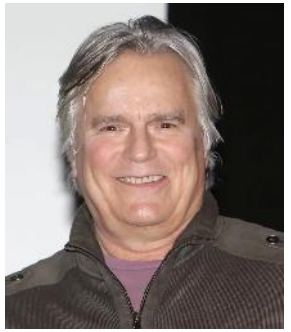
The MacGyver Hack to the Electronics…



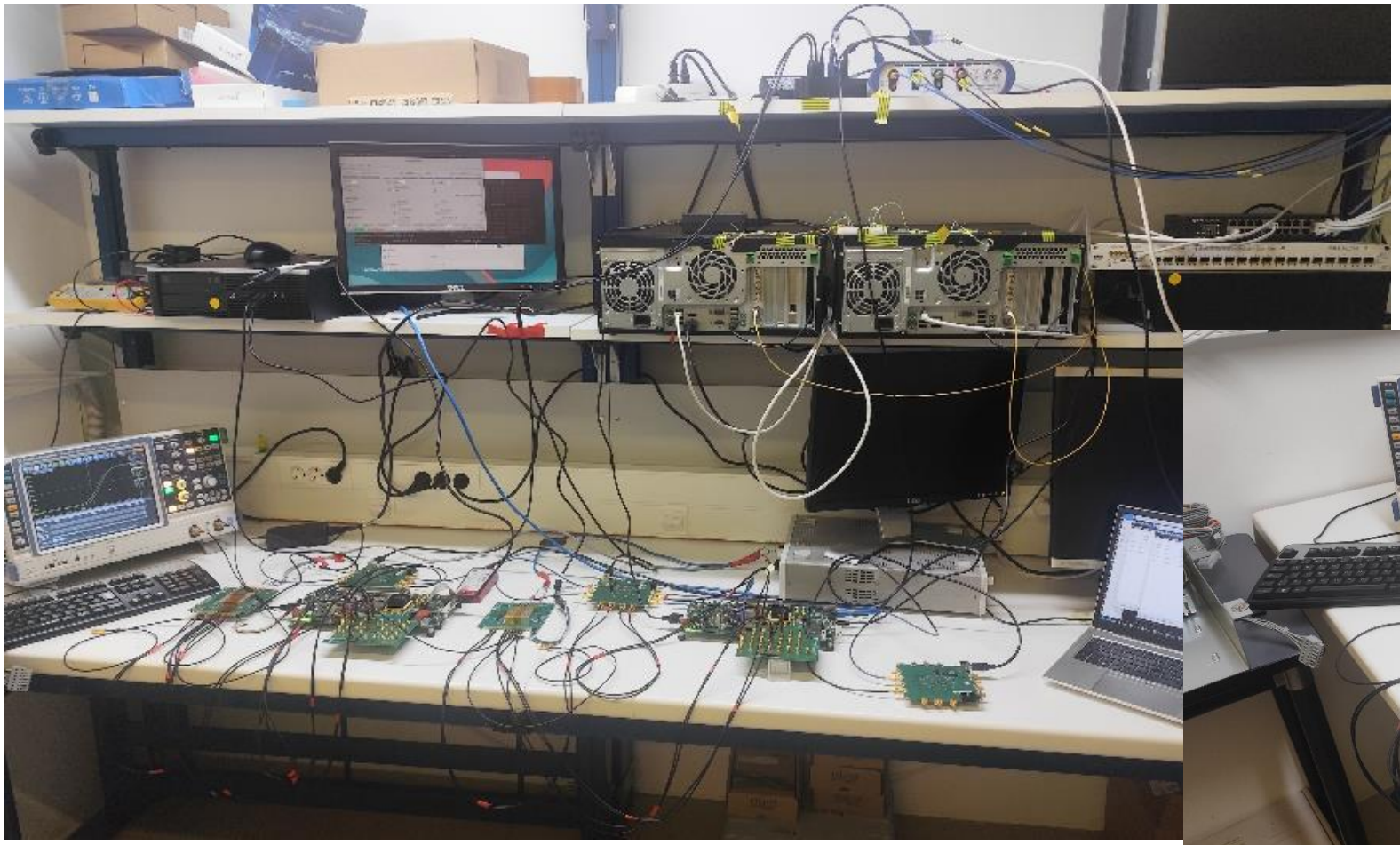


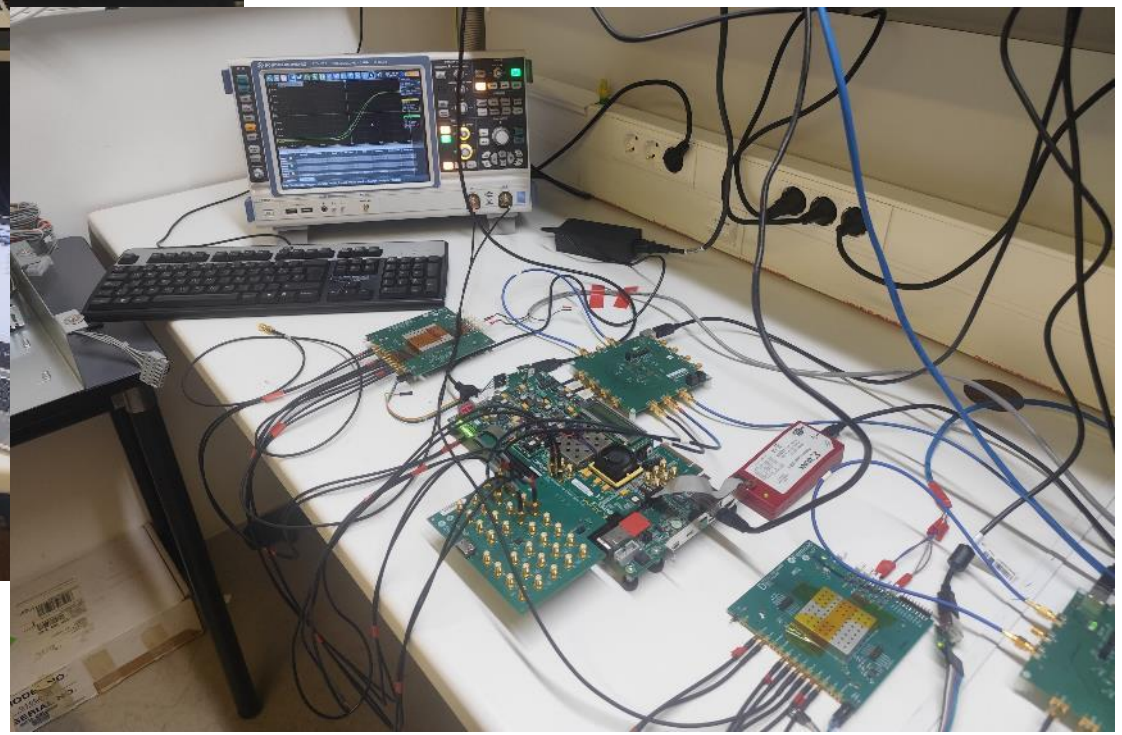


LVDS Clock Buffer replaced by output port



The cablish setup…

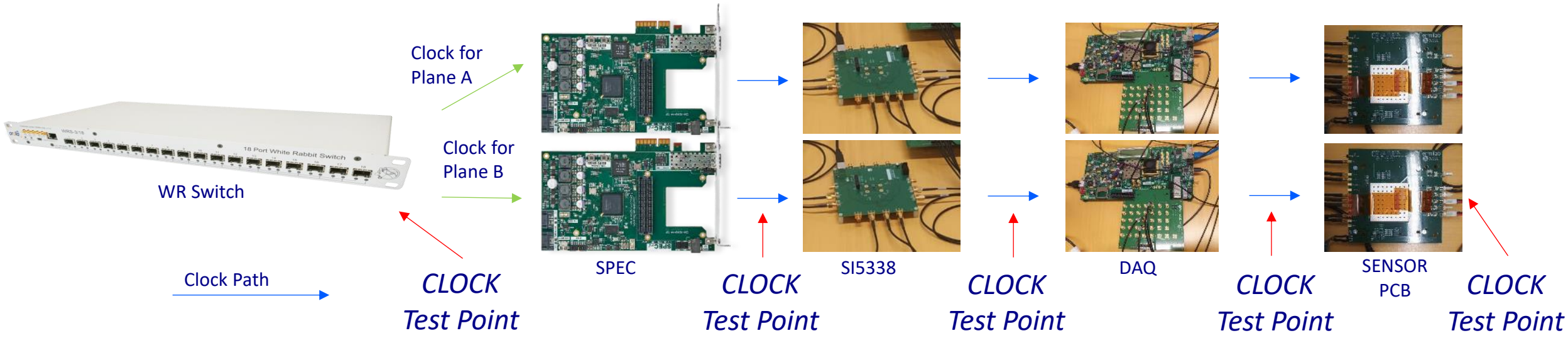




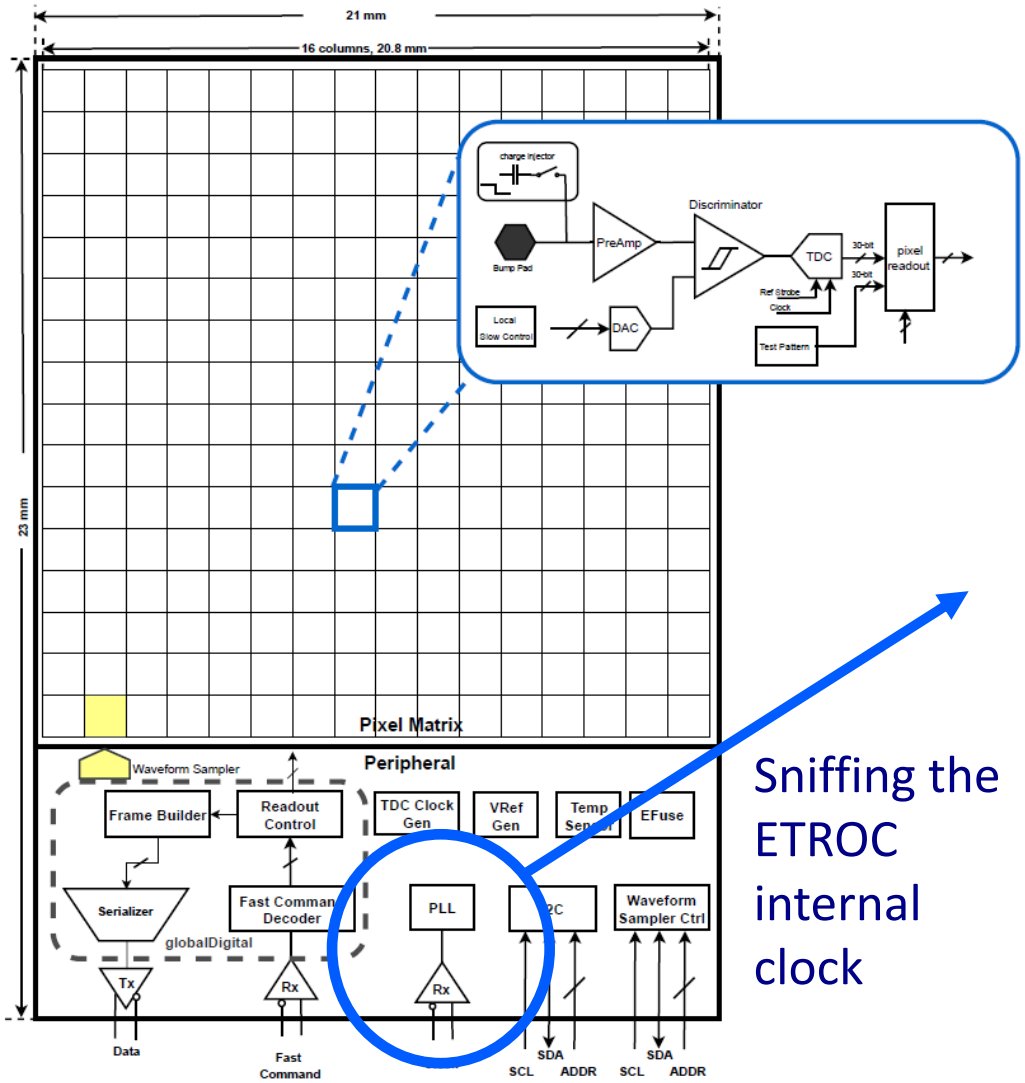
What are we now validating …

Phase A: Coaxial clock distribution with external clock synthesizer (40 MHz) using the Si5338 as 1:N fanout (transparent)

Phase B: WR based clock (125MHz) slaves using the SI5338 to synthesize and derive 40 MHz outputs to DAQ and sensor card



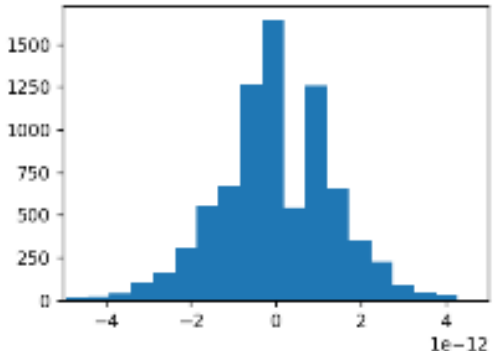
Jitter Performance; 40 MHz analog vs WR based distribution



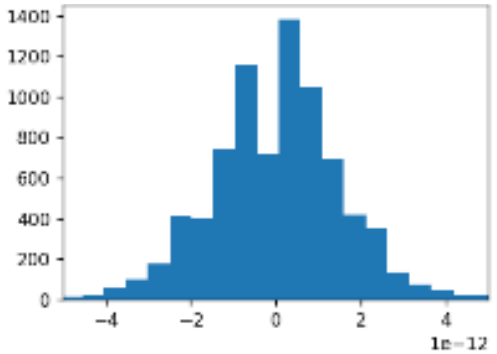
Sniffing the ETROC internal clock

40 MHz Ideal Clocking

Detector Plane A



Detector Plane B

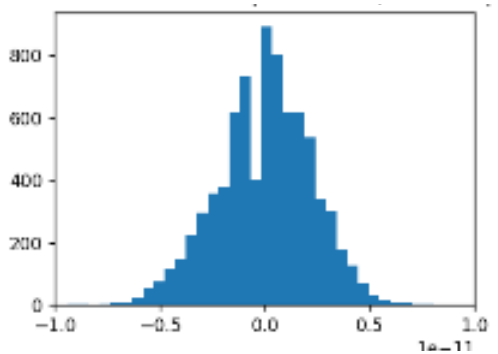


Plane A RMS jitter = 1.3658 ps

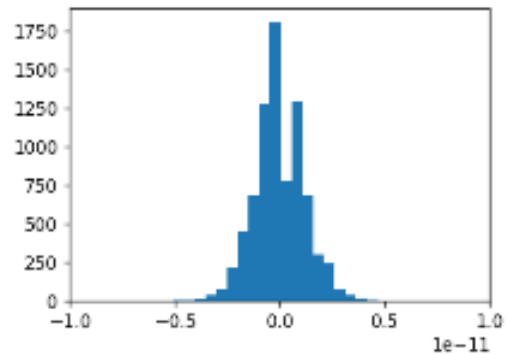
Plane B RMS jitter = 1.504 ps

White Rabbit Based Clocking

Detector Plane A



Detector Plane B



Plane A RMS jitter = 2.2489 ps

Plane B RMS jitter = 1.1864 ps

Close to Golden Reference System

Status and Future Plans

-Architecture of the Detector Prototype

Multiplane system based on ETROC validated

Compensated clock distribution (40 MHz) validated

WR based clock distribution prototype being verified; based on SPEC (hacked) + SI5338 (functional verification)

-Validation of WR COTS prototype and Measurement campaign

Physics; Study of clocking performance for Physics (image reconstruction) on-going

Clocking quality; Improve and perform further measurement

Proper instrumentation for Clock TIE in each plane

Skew calibration and mitigation between planes

Improve measurement campaign with WR based clocking

Performance from Master clock to WR slave, DAQ, sensor card and ASIC (sniffing internal clock)

Phase jumps after reset due to SI5338 re-start, mitigation

-Future plans for WR node, FMC cards…

Asses if we can “clean” the hack on the SPEC and new FMC for our commercial COTS prototype

Use an alternative platforms / implementations to the SPEC for our 4D application

Stress test on trigger synchronization between planes

Instituto Tecnológico de Aragón

¡Muchas gracias!