The PreProcessor system for the ATLAS Tile Hadronic Calorimeter at the HL-LHC

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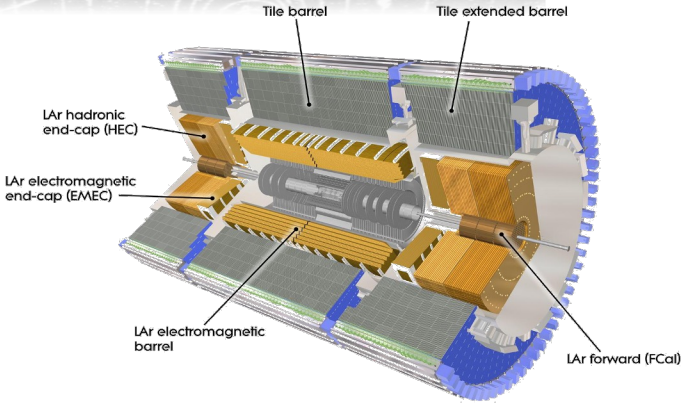
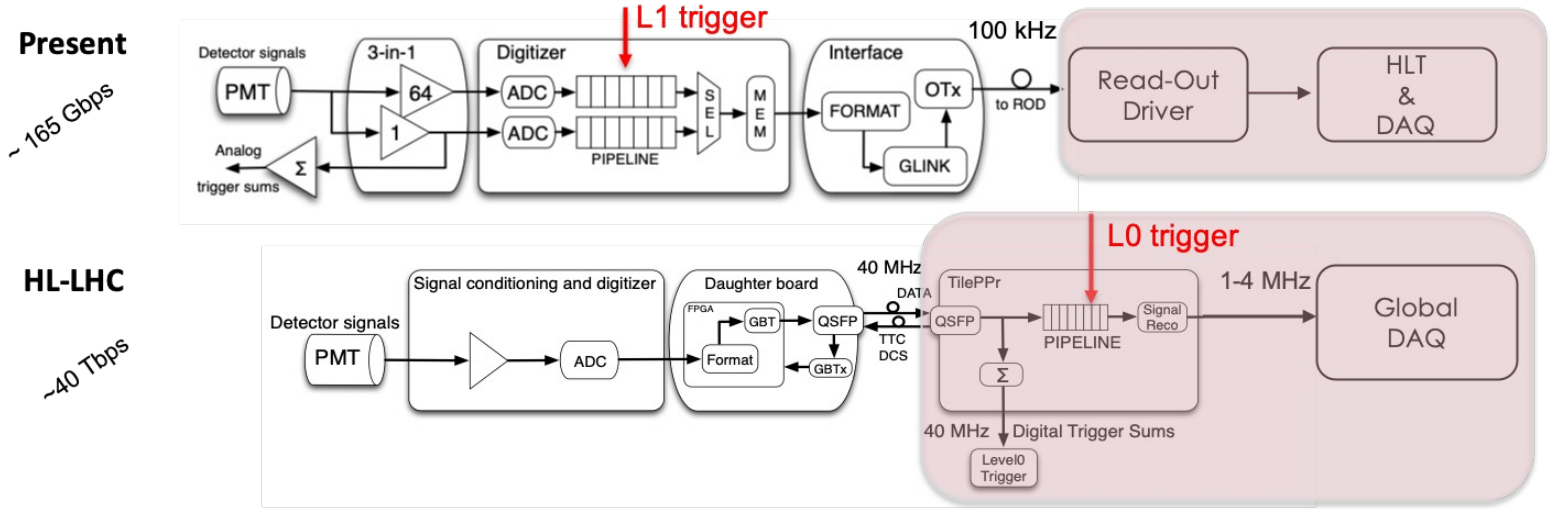
The TileCal detector and electronics

TileCal is the central hadronic calorimeter of ATLAS

- Plastic tiles groupped into cells readout photomultipliers via WLS fibers
  - ~10k photomultipliers/readout channels (two per cell)
- LHC: Sampling at 40 MHz → Trigger (40 MHz) and DAQ (100 kHz) paths → RODs
- HL-LHC : Sampling at 40 MHz → Full readout at 40 MHz → PreProcessors



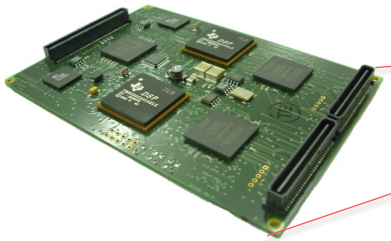
The IFIC TileCal Group is responsible of the design, production, maintenance and upgrades of the ROD and PPr systems



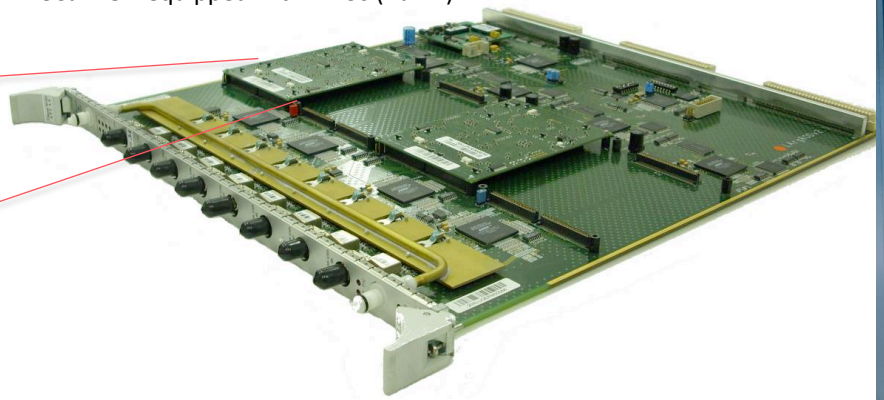
TileCal Read-Out Drivers

- Read-Out Drivers current DAQ (2008-2026) – interface between the front-end electronics and the High Level Trigger
  - 9U VME custom module equipped with up to 10 FPGAs and DSP-based PUs for bulk processing. 32 RODs to readout the entire detector
  - Deserialization, **data/trigger synchronization**, error checking, **signal reconstruction**, detector raw data compression, output data formatting, monitoring, **data flow control (veto)**
  - Data routing and formatting in FPGAs (VHDL), data processing in DSP (C & assembler)

Processing Unit (PU)

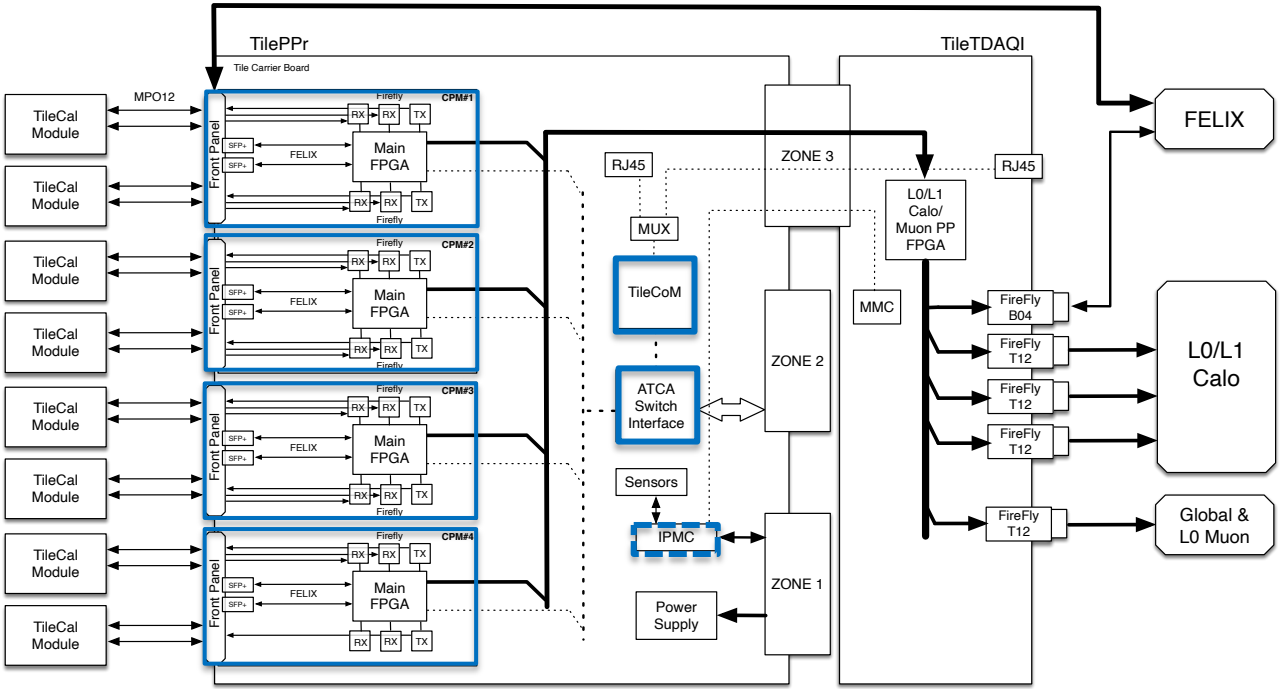


TileCal ROD equipped with 2 PUs (Run 1)



TileCal HL-LHC off-detector electronics

- The Tile PreProcessor is the core element of the off-detector electronics
  - Data processing, clock distribution, on-detector configuration, **low latency interface with LO trigger and readout systems**
  - **Modular concept**: optimize the design, manufacturing processes, enhance components maintenance and replaceability and facilitate future improvements in terms of functionality

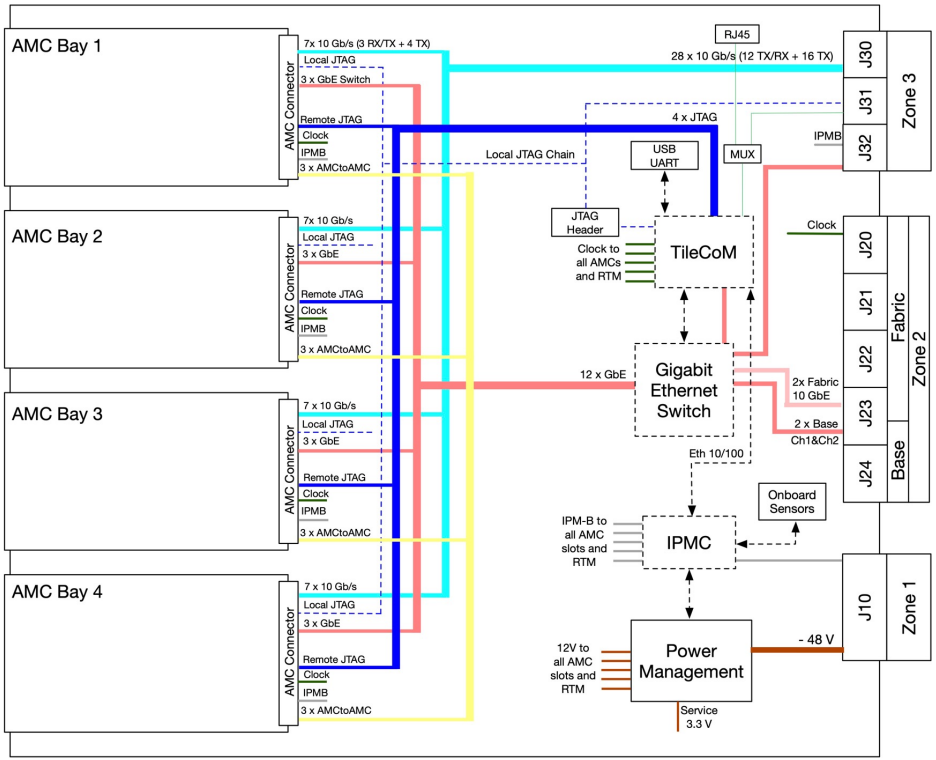


The TileCal-IFIC Group is responsible for the design and production of:

32 ATCA Carrier Boards
32 GbE Switch modules
32 TileCoM SoC modules
32 IPMCs
128 CPMs

TileCal ATCA Carrier Base Board

- Specifications comply with final requirements
  - ATCA backplane operation
  - 4 AMC slots interconnected with RTM through Zone 3
  - Ethernet interconnection with AMCs/RTM
    - Switch 16 x GbE
  - Board control and remote programming – TileCoM SoC
  - Health monitoring and control with IPM-Controller (CERN)
  - Most challenging aspect are the high aggregated throughput
    - 32 lanes (up to 35cm) x 10 Gbps



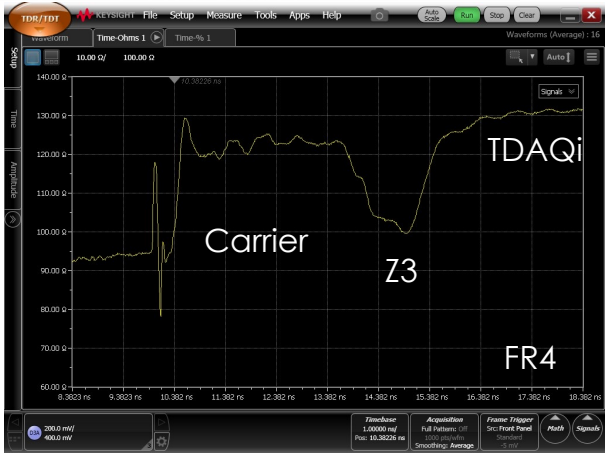
ATCA Carrier Board – Certification tests

Version 2.1 (2021)

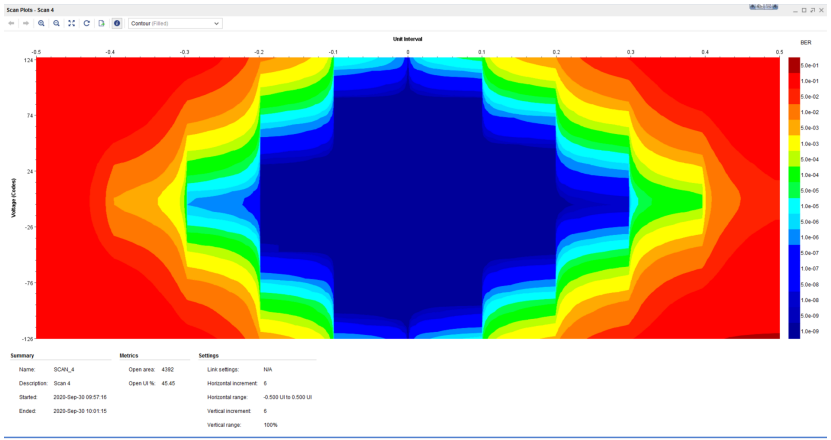
- Re-mapping and re-routing of long traces
- Low losses materials and impedance control during fabrication
- MEGTRON6 Panasonic: Df= 0.003 @ 6 GHz – Controlled Impedance
  - Excellent signal integrity results
    - BER **~1 x 10^{-17}** (26 days) for PRBS-31 at 10 Gbps for **35 cm traces** (longest)
    - Problems with AMC connectors assembly (press-fit)

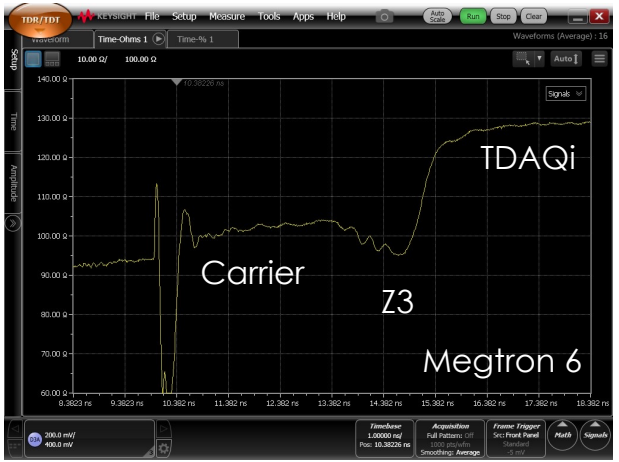
Version 2.2- Final version (2024 – On production)

- Remove validation-specific components that are not essential for operational functionality

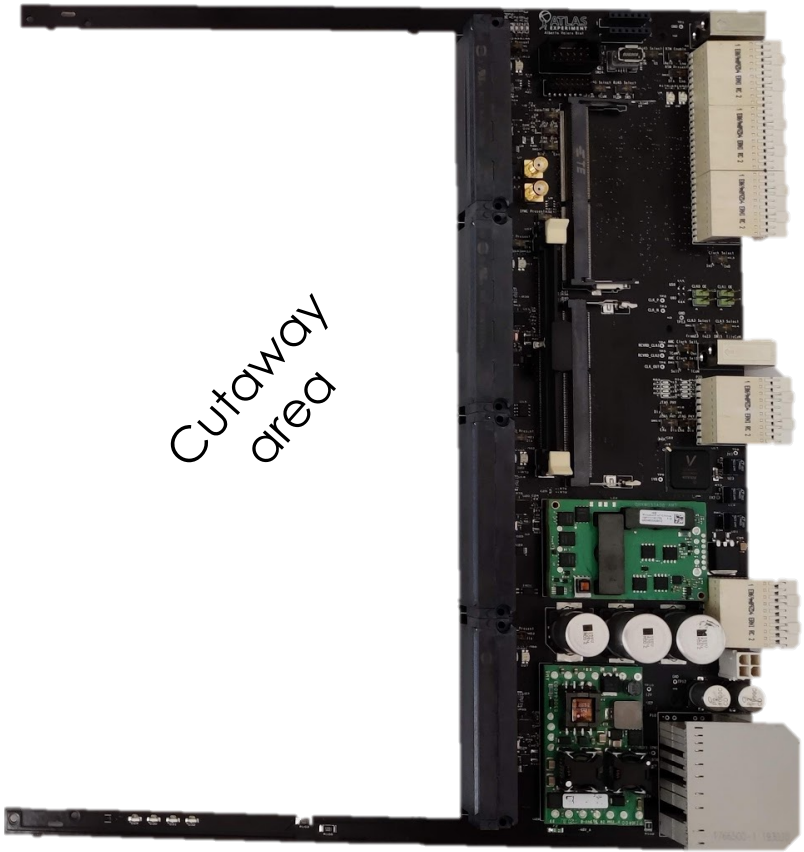


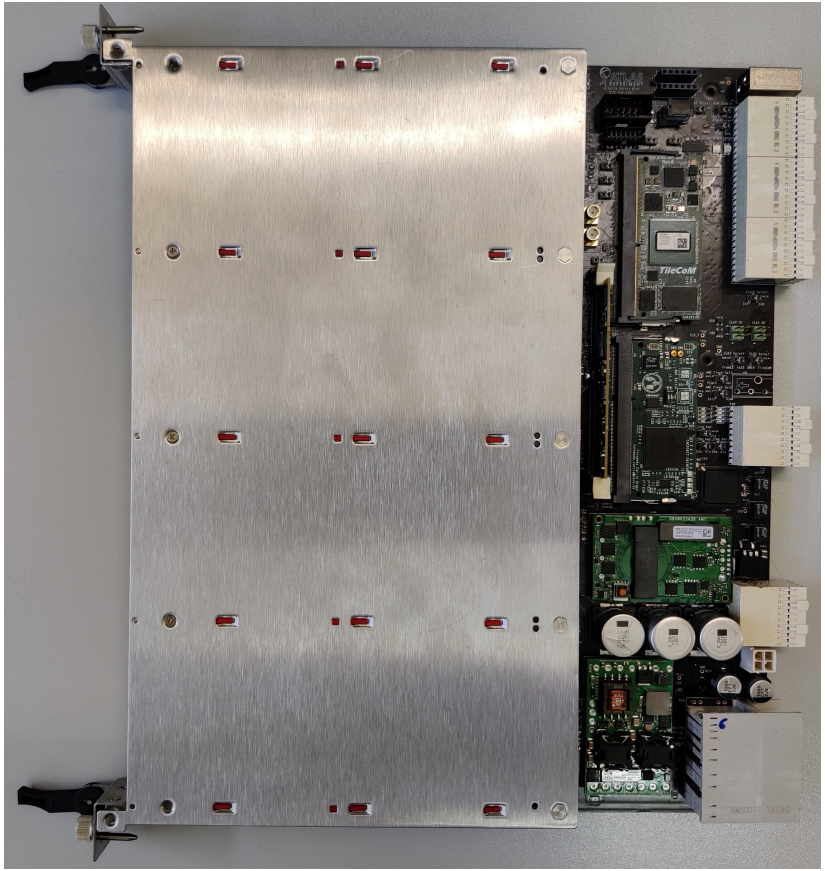
Differential impedance of the longest trace connecting AMC bay 4 and the TDAQi plugged in the Zone 3





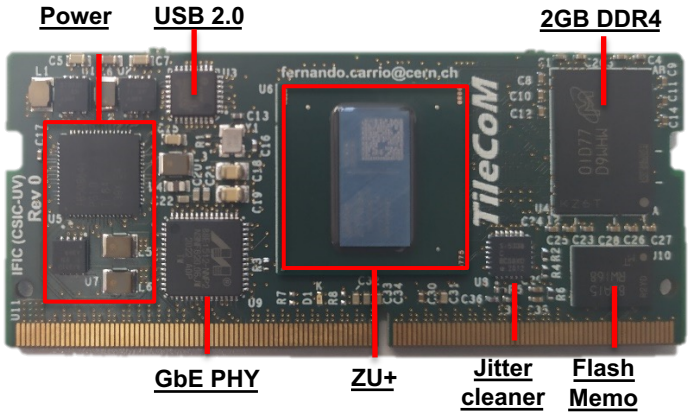
ATCA Carrier Board

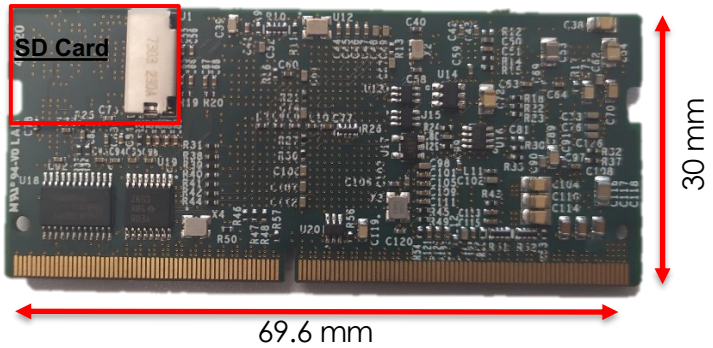


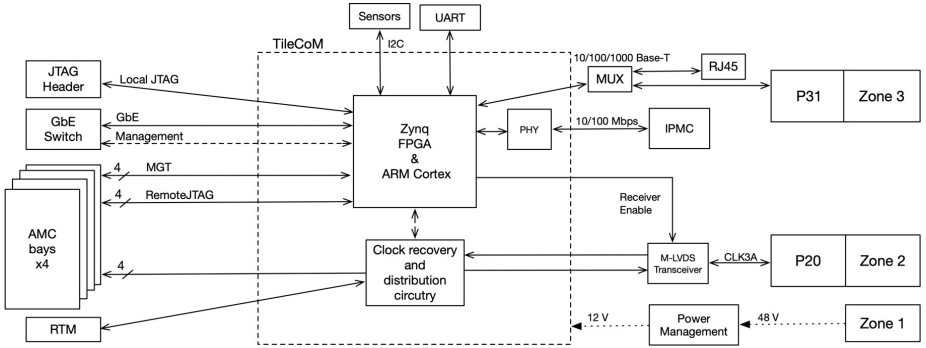


TileCoM hardware developments

- TileCoM System-on-Chip module – ARM processor
  - Detector Control System sensors reading
  - PPr system health monitoring
  - Remote FPGA programming
  - Local clock recovery and distribution
- High density of components (3 x 7 cm)
  - Zynq UltraScale+ ZU2CG, 2GB DDR4
  - SD card, GbE, USB 2.0, SPI, I2C, UART, 82 x GPIO (1.8V)
  - PCB with 10 layers (1.2 mm), FR4
  - Test board to validate all funcionalities
- First units produced. Design under validation



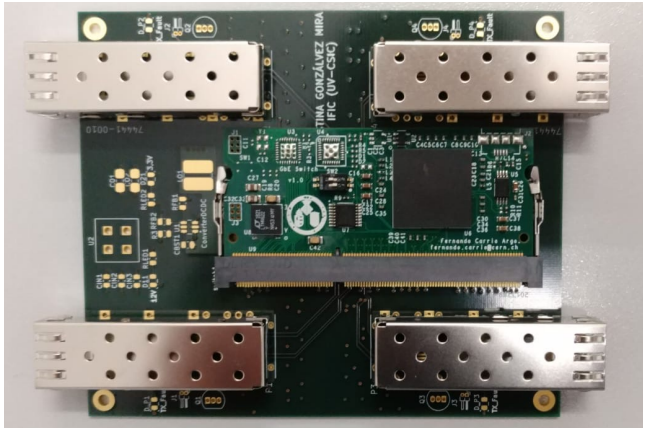


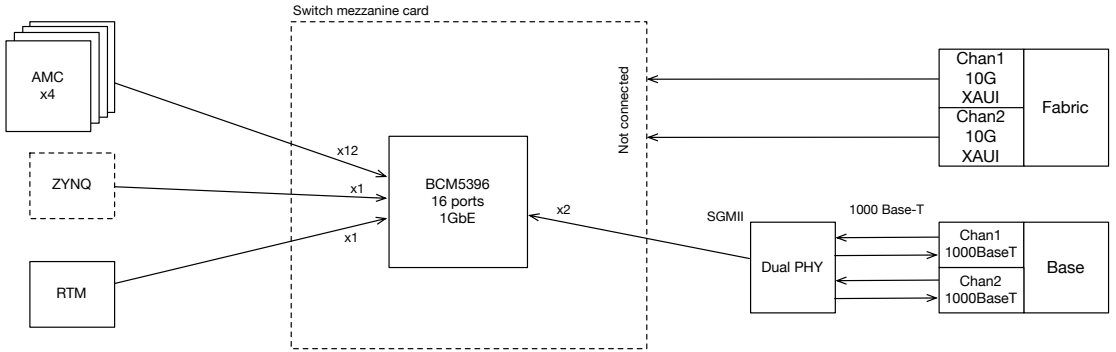


Switch module

- Switch module: SO-DIMM 204 pins
  - Functionality: provide external access through ethernet to configurable devices
  - 16 GbE ports to interconnect CPMs, TileCoM and TDAQi with the Base Interface (Zone2)
- Custom design. First units of final version produced and verified
  - Based on Broadcom BCM5396
  - Unmanaged operation. Configuration and monitoring from TileCoM
  - 16 GbE ports : 3 x AMC (12), 1xTileCoM, 2 x Zone2 BASE, 1xRTM
  - 2 Channel of FABRIC (10G) connected to Switch slot for future upgrades
- Final production of 50 modules ongoing

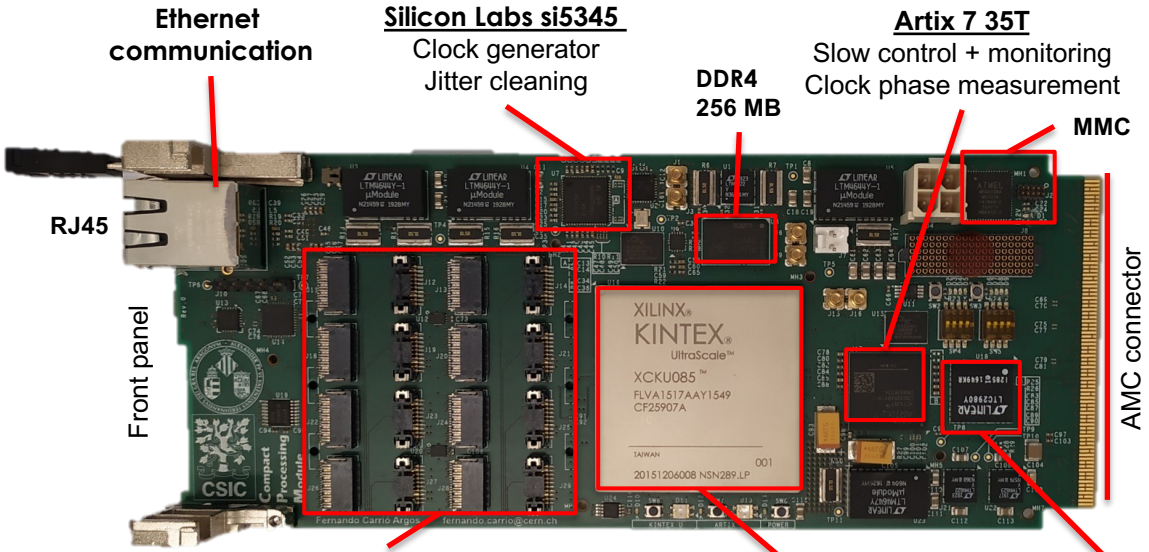
GbE switch





Compact Processing Module - Overview

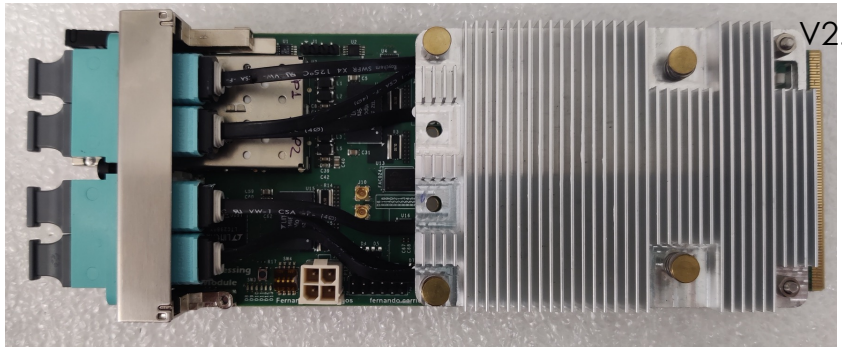
- Single AMC board with full-size form factor
  - **32 channels** through **8 Samtec Firefly modules** → High bandwidth readout system – Up to **400 Gbps** via optics
  - **14 channels** through AMC connector → – Up to **175 Gbps** via electrical backplane
  - **Kintex KU085 for proto(v1), KU115 for final design**

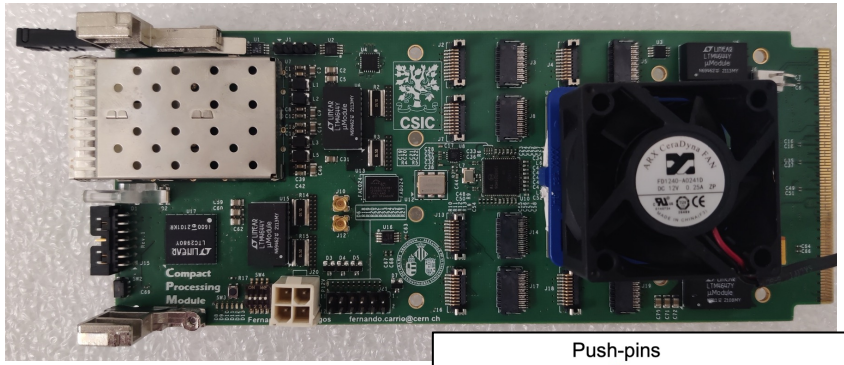


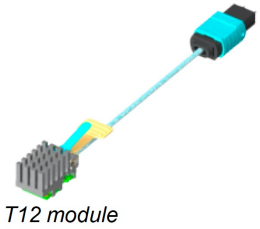
Compact Processing Module

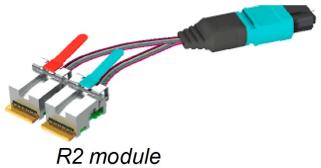
CPM v2.0

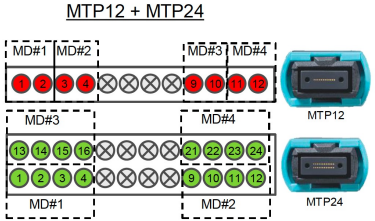
- All Artix7 FPGA functionalities moved to KintexUltraScale
  - **XCKU115-2FLVA1517E** – Higher clock frequencies – Higher data rates for GTH
  - Control and configuration of peripherals. Sensor/DCS readings
  - Interface with TileCoM
- New Samtec Firefly optical modules
  - **Improve fiber routing**
  - CPMv1: 8 bi-dirmodules (4 TX/RX)
  - CPMv2: 4 RX modules + 2 TX modules
- SFP modules for FELIX interface
  - Allocated in the front-panel
  - **Direct connection to FELIX**
- Removed non-essential components
- NOW:
  - 7 modules produced under validation then PreProducction
    - Components in hands
    - FDR this year
  - Firmware developments

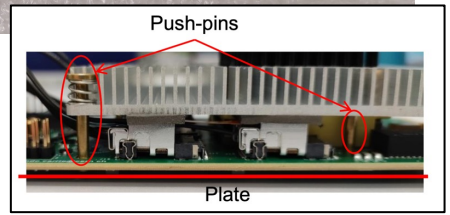





T12 module


R2 module





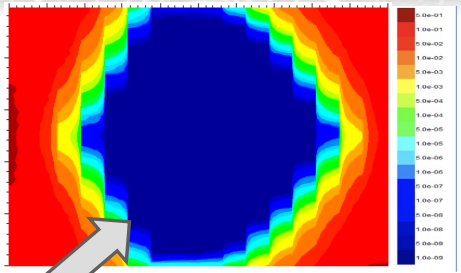
Signal integrity measurements

Samtec Firefly modules @ 4.8 Gbps & 9.6 Gbps

- Keysight DCA-X86100D sampling oscilloscope
- Acceptable jitter values measured with PRBS-31 data pattern

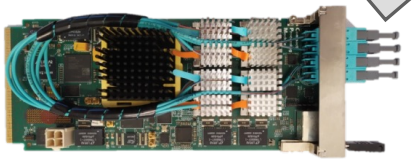
Bit Error Rate tests

- Test bench with two CPMs, local clocks and 1.5-meter fibers
- 32 links at 9.6 Gbps with PRBS31 pattern during one week
- Total BER better than $1.6 \cdot 10^{-17}$ for a confidence level of 95%



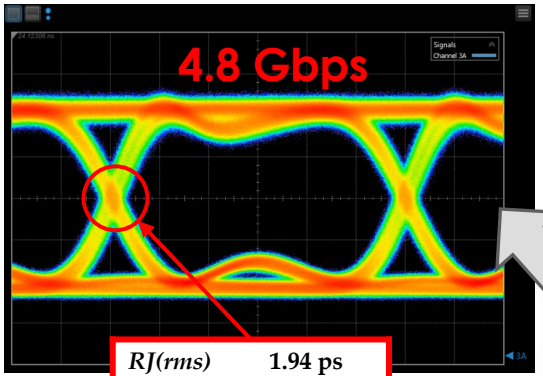
IBERT @ 9.6 Gbps (FPGA internal)

Eye Width	191.84 ps
Eye Height	73.15%

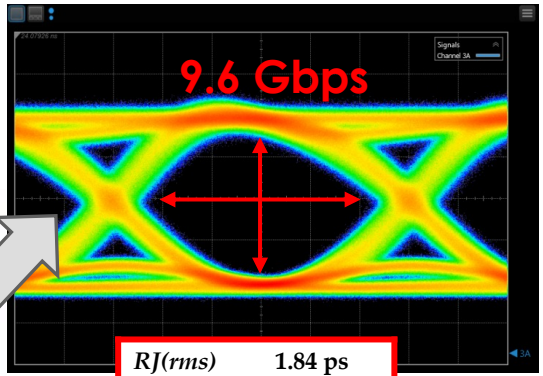


PRBS-31 @ 4.8 Gbps @ 9.6 Gbps

Eye Width	85.92 ps
Eye Height	87.10%



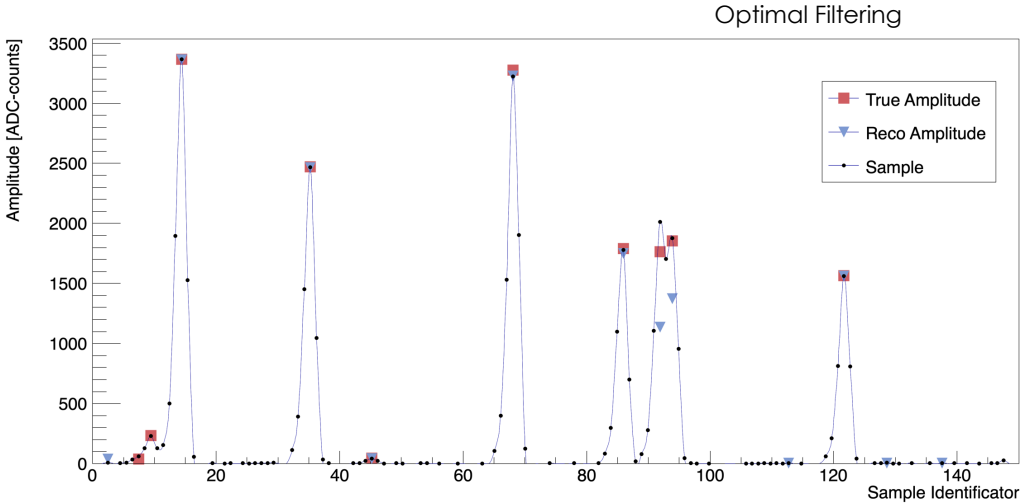
RJ(rms)	1.94 ps
DJ (δ-δ)	2.40 ps
TJ (10^{-12})	28.84 ps



RJ(rms)	1.84 ps
DJ (δ-δ)	5.85 ps
TJ (10^{-12})	30.96 ps

Firmware: Tile Signal Reconstruction

- Projects being organized with HDL-on-GIT (Hog)
  - Set of Tcl/Shell scripts plus a methodology to handle HDL designs in a Gitlab repository
  - Guarantees firmware reproducibility and assures traceability of files
- Infrastructure to perform firmware simulation studies using Questa/Modelsim with Python
  - Input: ascii file produced in Athena; Output: ntuple with reconstruction results
  - **CoCoTb: python package to interact with Firmware simulators**
- Implementation in FPGA of OF and Neural Network algorithms for 48 channels – reduced resources occupancy
  - In both cases Latency meets Level o trigger requirements (< 200 ns)



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FPGA implementation of a deep learning algorithm for real-time signal reconstruction in particle detectors under high pile-up conditions

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Abstract: The analog signals generated in the read-out electronics of particle detectors are shaped prior to the digitization in order to improve the signal to noise ratio (SNR). The real amplitude of the analog signal is then obtained using digital filters, which provides information about the energy deposited in the detector. The classical digital filters have a good performance in ideal situations with Gaussian electronic noise and no pulse shape distortion. However, high-energy particle colliders, such as the Large Hadron Collider (LHC) at CERN, can produce multiple simultaneous events, which produce signal pileup. The performance of classical digital filters deteriorates in these conditions since the signal pulse shape gets distorted. In addition, this type of experiments produces a high rate of collisions, which requires high throughput data acquisitions systems. In order to cope with these harsh requirements, new read-out electronics systems are based on high-performance FPGAs, which permit the utilization of more advanced real-time signal reconstruction algorithms. In this paper, a deep learning method is proposed for real-time signal reconstruction in high pileup particle detectors. The performance of the new method has been studied using simulated data and the results are compared with a classical FIR filter method. In particular, the signals and FIR filter

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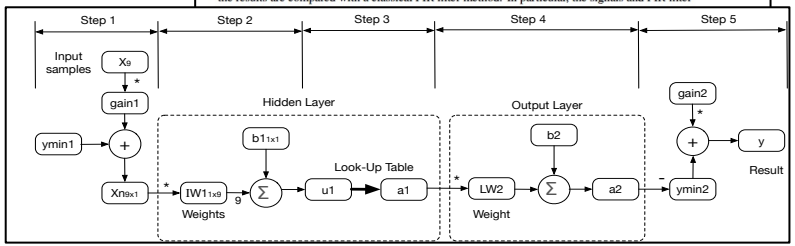
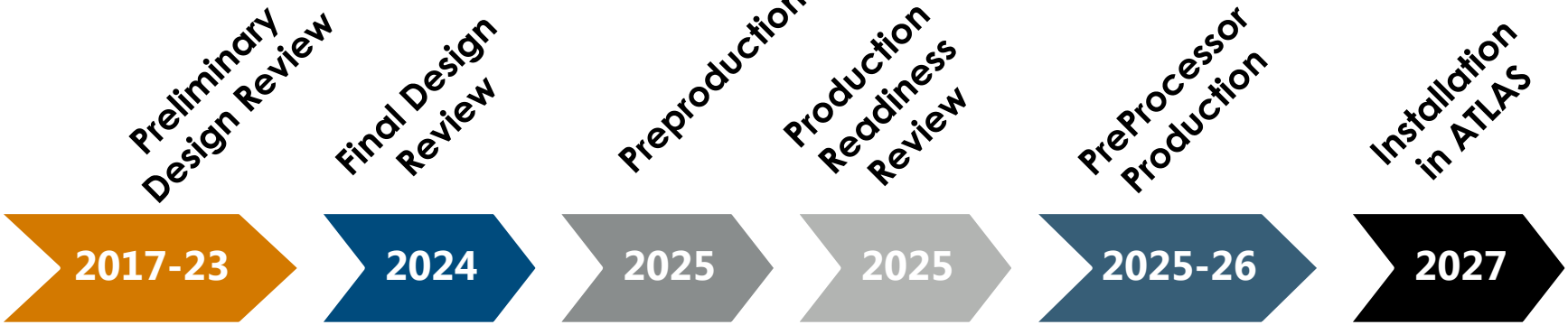
Latency
125ns



Roadmap towards HL-LHC operation



- **Prototyping**
- **Electrical tests**
- **Optical tests**
- **Test-beams**
- **Firmware devs**

- Full-size PPr
- Integration tests with on-detector
- Documentation
- Firmware opt
- Preproduction

- Test bench design
- Integration tests at CERN
- Validation at test-benches

- Tendering process
- Final production
- Validation and shipping
- Final integration tests

- Installation of ATCA crates
- Tests in ATLAS with on-detector and Trigger electronics

- Final design prototypes being manufactured now
- Preproduction (12.5%) from Q4 2024 to Q1 2025
  - 4 ATCA carriers, 16 CPMs
- Final production (87.5%) from Q2 2025 to Q3 2026
  - 28 ATCA carriers, 112 CPMs

32 Carriers, 128 CPMs in total (+ spares)

THANK YOU FOR YOUR ATTENTION!