Plan of Re-entrant BPM R&D for ILC Main Linac

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Requirements for Main Linac Cold-BPM in Cryomodule

(1) **The BPM measures beam position in cryomodule, bunch by bunch, with a resolution of less than 1 μm at $2x10^{10}$ electrons/bunch.**

-> low Q value for fast signal damping at 2K circumference

-> good signal-to-noise ratio for high resolution

-> high precision on mechanical center definition and electrical center definition

-> high common-mode rejection, high isolation for x-to-y coupling

(2) **The beam pipe diameter 78mm (big diameter).**

-> lead to low frequency resonant-mode BPM

-> no coupling to cavity HOM and no conflict with dark-current excited cavity HOM

(3) **BPM is installed inside of cryomodule, next to SC-cavity.**

-> simple structure with no contamination inside (clean-room compatible)

-> HPR rinse applicable

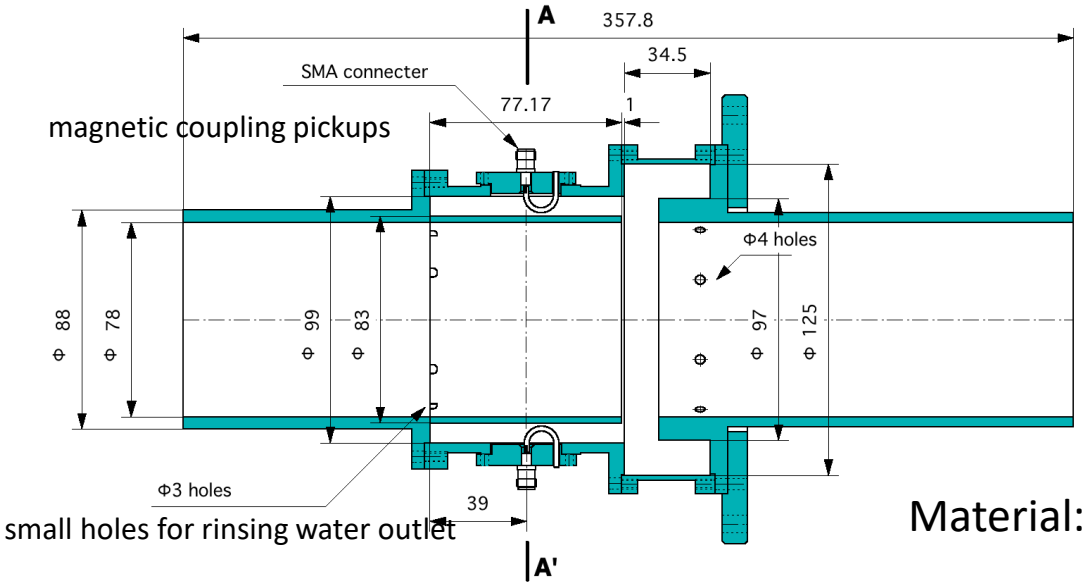
-> light weight for easy to handle/to install in clean-room

Design Base : Saclay re-entrant BPM

adding waveguide loading for CM-rejection and X-Y coupling rejection

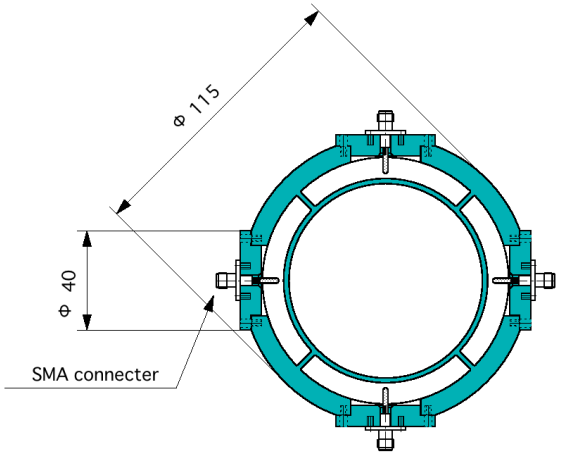
Proto-type BPM

Proto-type model

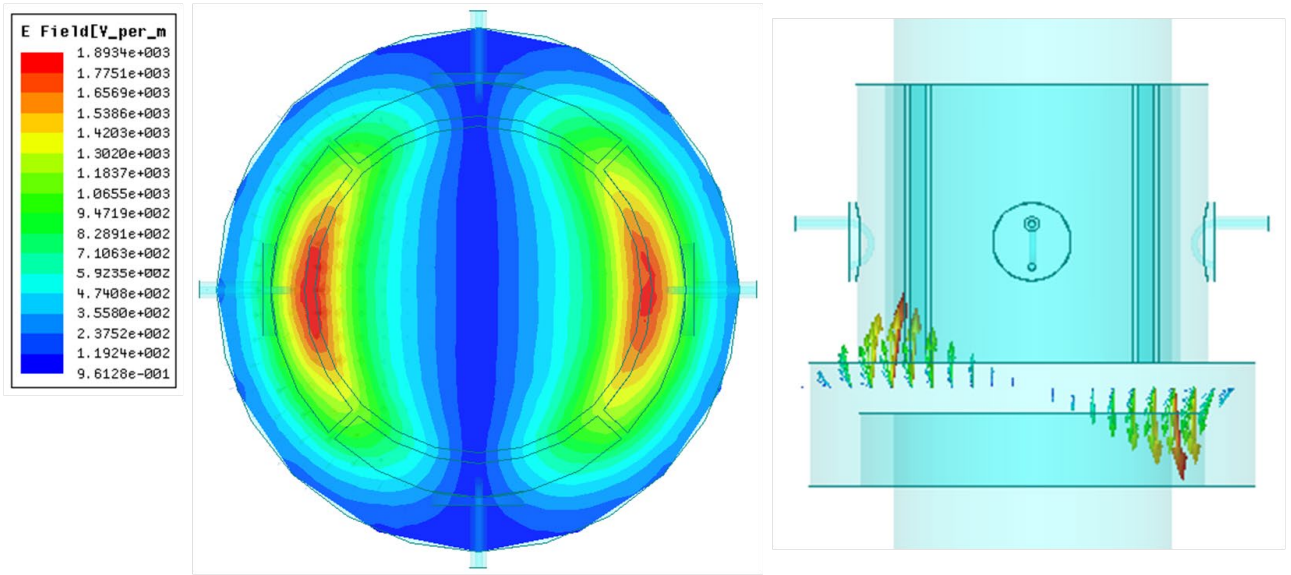


small holes for rinsing water outlet

Material: SUS



A - A' cross section



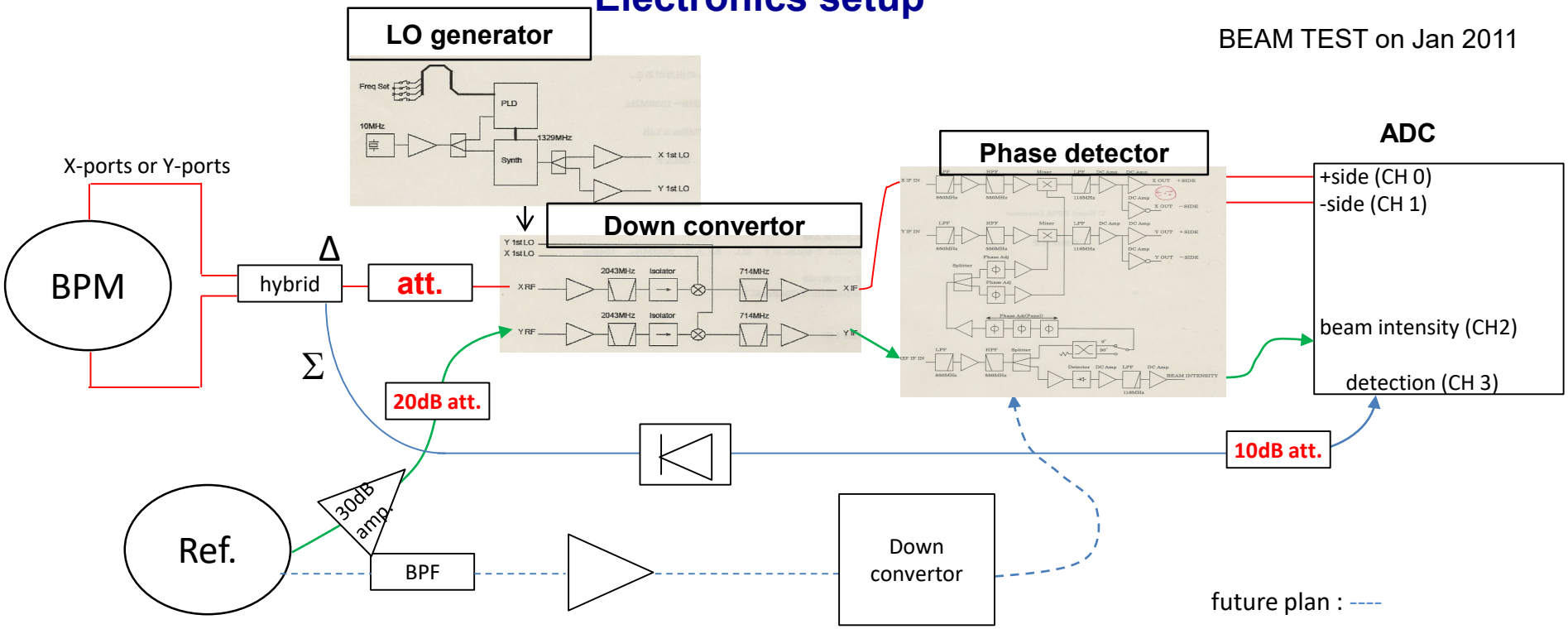
dipole mode: 2.04GHz (No interference with Cavity HOM)

Beam response test of prototype model at ATF-LINAC (2) using phase detection circuit

(phase between BPM cavity, Reference cavity)

Electronics setup

BEAM TEST on Jan 2011



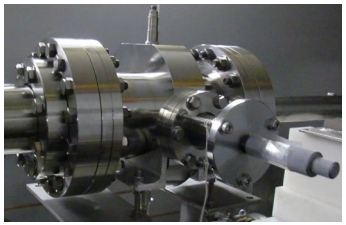
Both signal were down converted to 714MHz, then fed into the phase detector. Analog output of the phase detector were fed into integration ADC (charge ADC).

3 BPM for resolution measurement

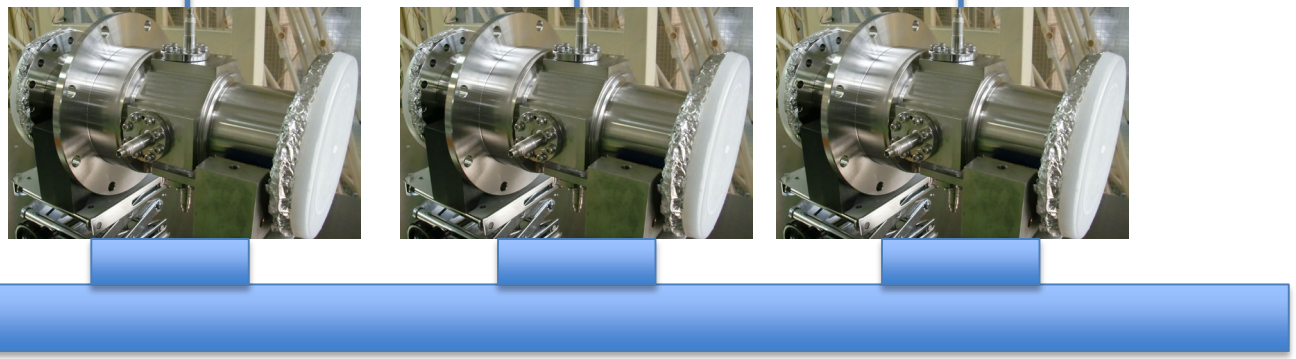
Beam Experiment for Vacuum-tight model

Two more BPMs are fabricated in Korea (KNU).

Reference cavity



3-BPM for resolution estimation



Digital signal acquisition

Down-converter(2040MHz ->80MHz) + OSC(8bits 5GS/s)

RF test results of 3 BPMs after installation at end of Linac

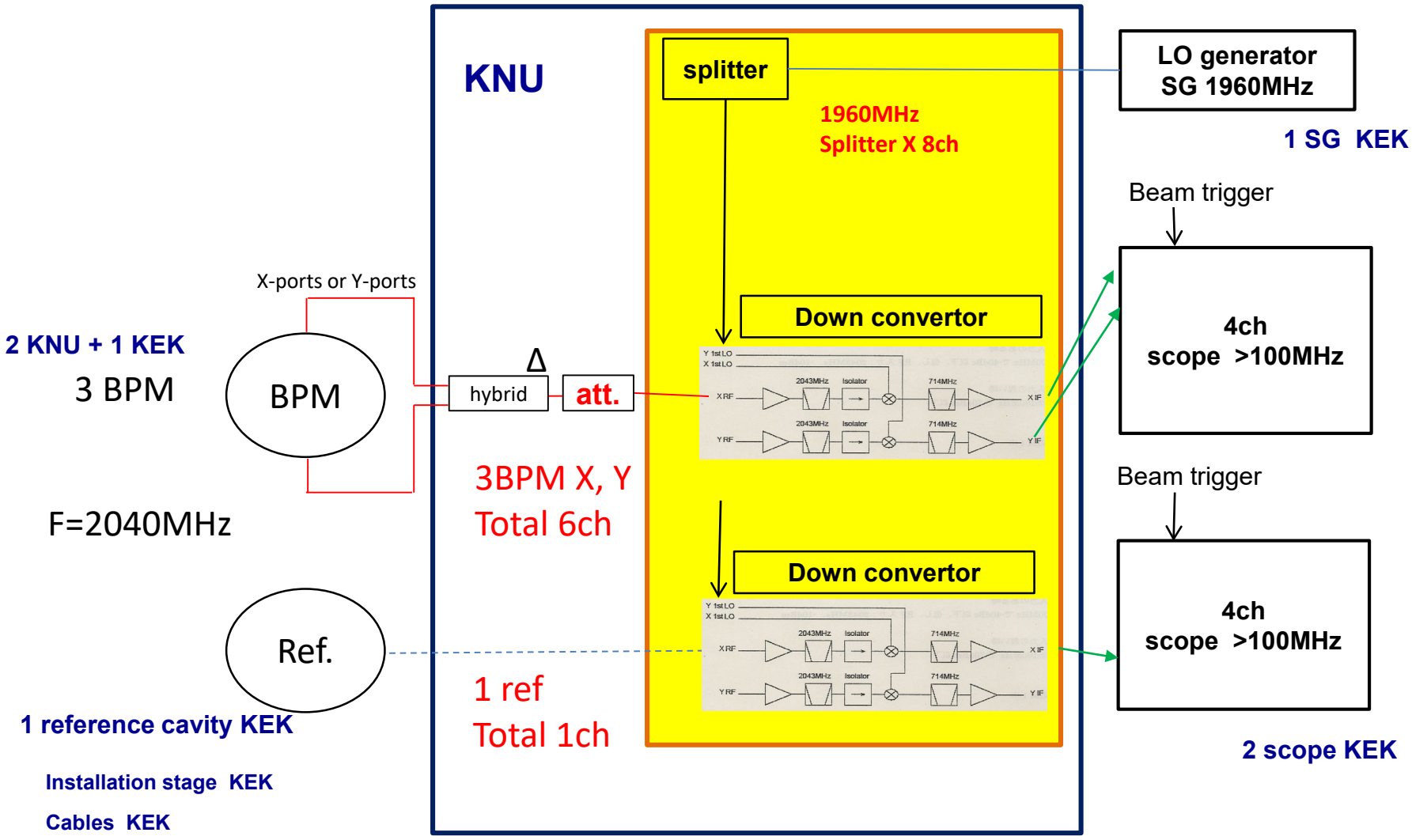
- All the parameters are calculated by using ave(S12+S21)

BPM #	Input port	Output port	f[GHz]	Δf [MHz]	QL	Q0	β	τ[nsec]
BPM-AX	1	3	2.015	11.9	169	577	2.41	13.4
BPM-AY	2	4	2.015	12.8	158	538	2.41	12.5
BPM-BX	1	3	2.050	10.3	199	871	3.37	19.5
BPM-BY	2	4	2.050	10.8	189	801	3.24	19.0
BPM-CX	1	3	2.022	9.27	218	633	1.91	17.2
BPM-CY	2	4	2.019	11.1	182	453	1.50	14.3

Three L-band BPM have a different resonant frequencies:
BPM-A = 2.015GHz, BPM-B = 2.050GHz, BPM-C = 2.020GHz

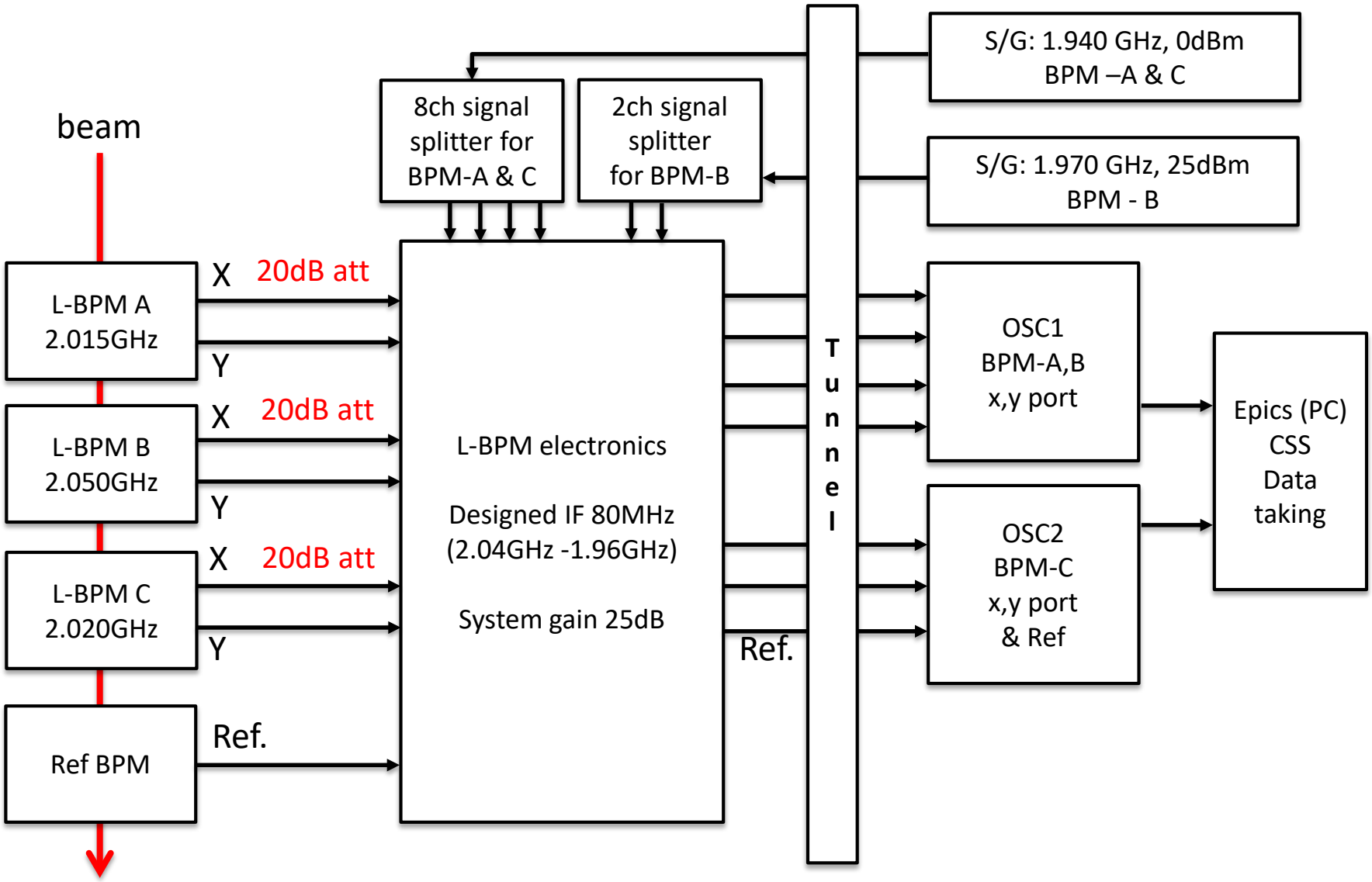
The BPM A & C are fabricated by A. Heo @ KNU
The BPM B is fabricated by H. Hayano san @ KEK

New 1st stage electronics

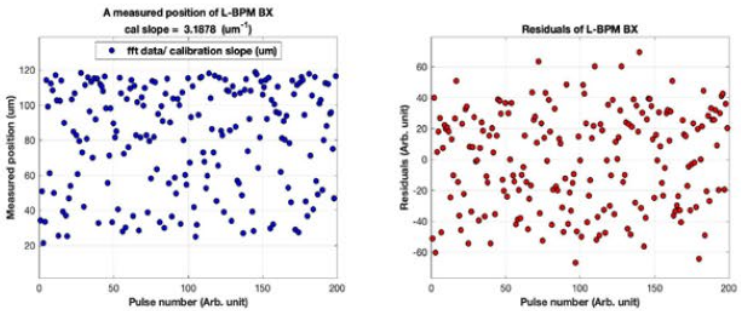


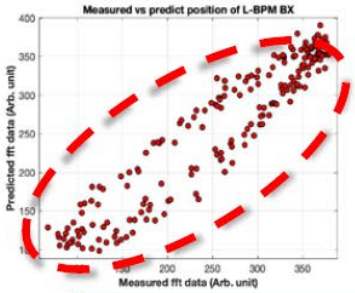
Electronics setup

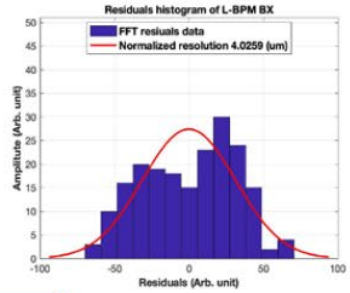
Beam test scheme



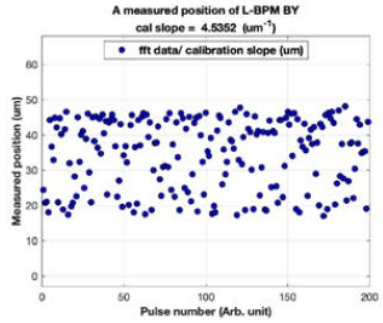
L-BPM Resolution run BPM-B with two S/G

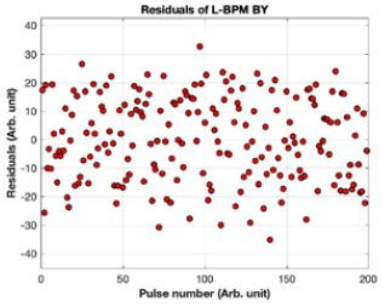


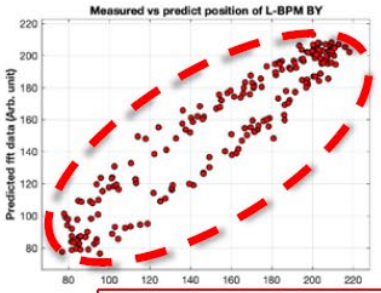


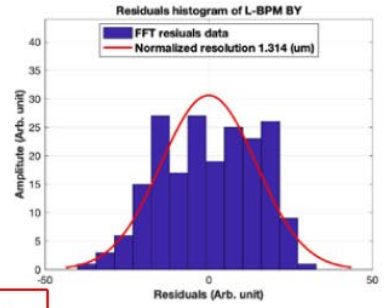


Poor correlation!



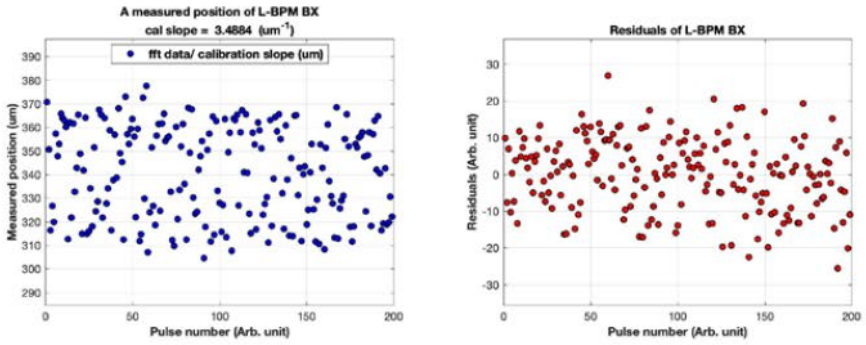


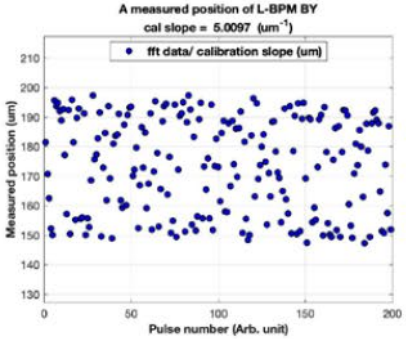


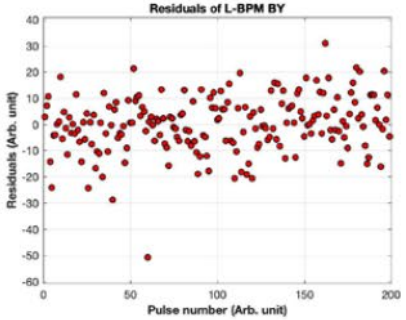


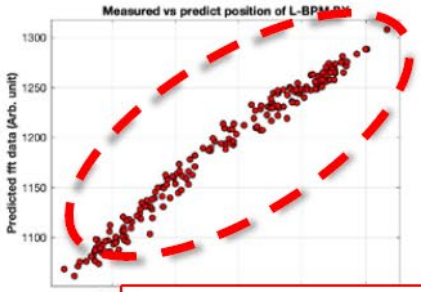
Poor correlation!

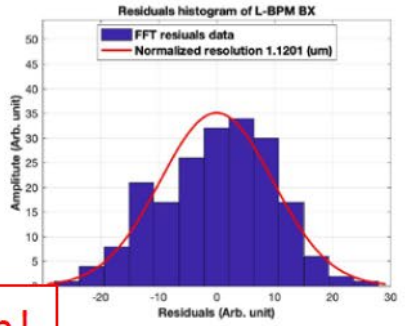
L-BPM Resolution run BPM-B with single S/G



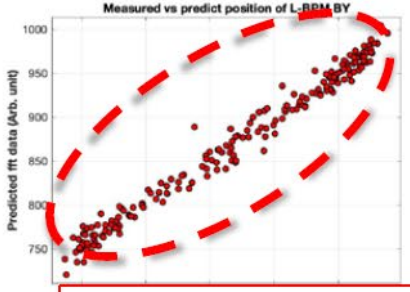


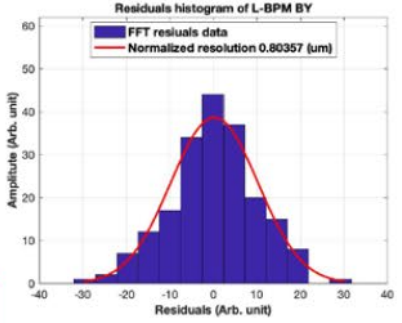






good correlation!

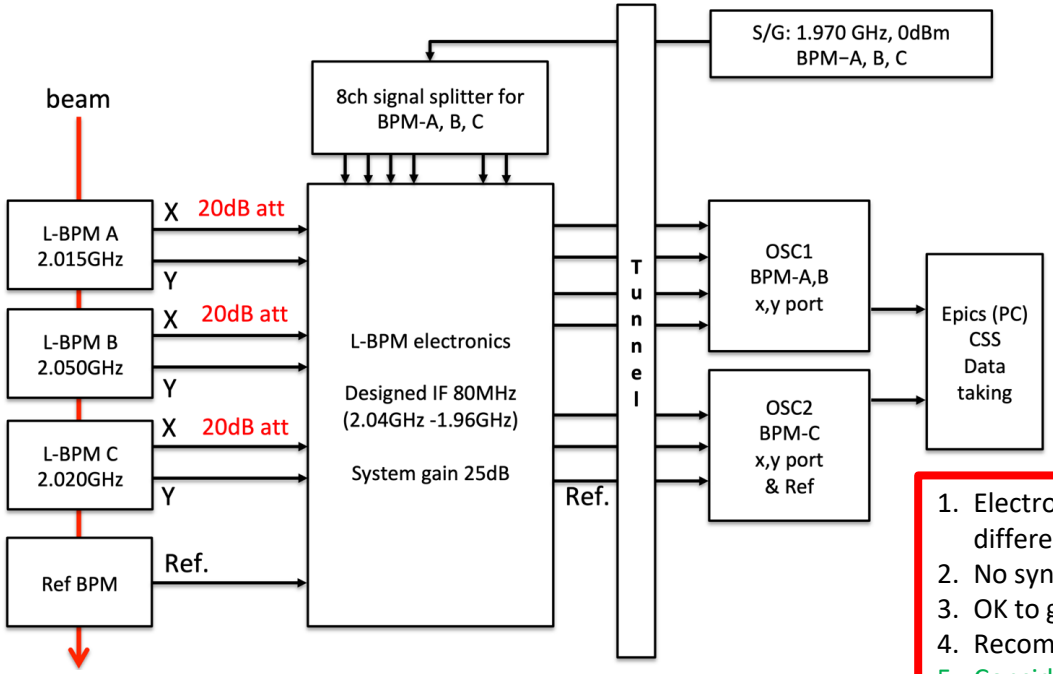




good correlation!

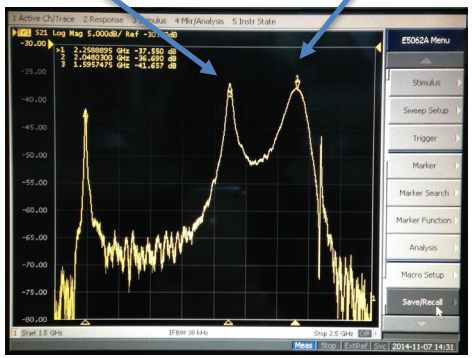
Next study purpose

Beam test scheme



dipole-mode (BPM mode 2.04GHz)

monopole mode (2.258GHz)



1. Electronics design that determines +- based on the signal direction difference between monopole and dipole.
2. No synchronization required for S/G and ATF DR RF signals.
3. OK to generate LO signal by individual dividing PLL by 3.
4. Recommend using 16bit ADC or Pico scope instead of 8bit OSC.
5. Considering the overall system, recommend developing new 1st stage electronics.
    1. **Generate 80MHz IF signal for each by dividing PLL by 3 and then perform digital mixing.**
    2. **Acquire signal using a 14~16bit ADC. (maybe. Possible)**
    3. Separate dipole mode and monopole mode using FFT in FPGA.
    4. Calculate beam position and phase using dipole mode.
    5. Determine +- beam position using the signal difference between monopole mode and dipole mode.

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Next study purpose

- Generate 80MHz IF signal for each by dividing PLL by 3 and then perform digital mixing

1.935GHz out
BPF: 1850~2040MHz

	Mean	RMS	σ (S-dev)
Frequency	1.935 GHz	-	-
Cycle-cycle jitter	-	5.3273 ps	5.3272 ps

1.970GHz out
BPF: 1850~2040MHz

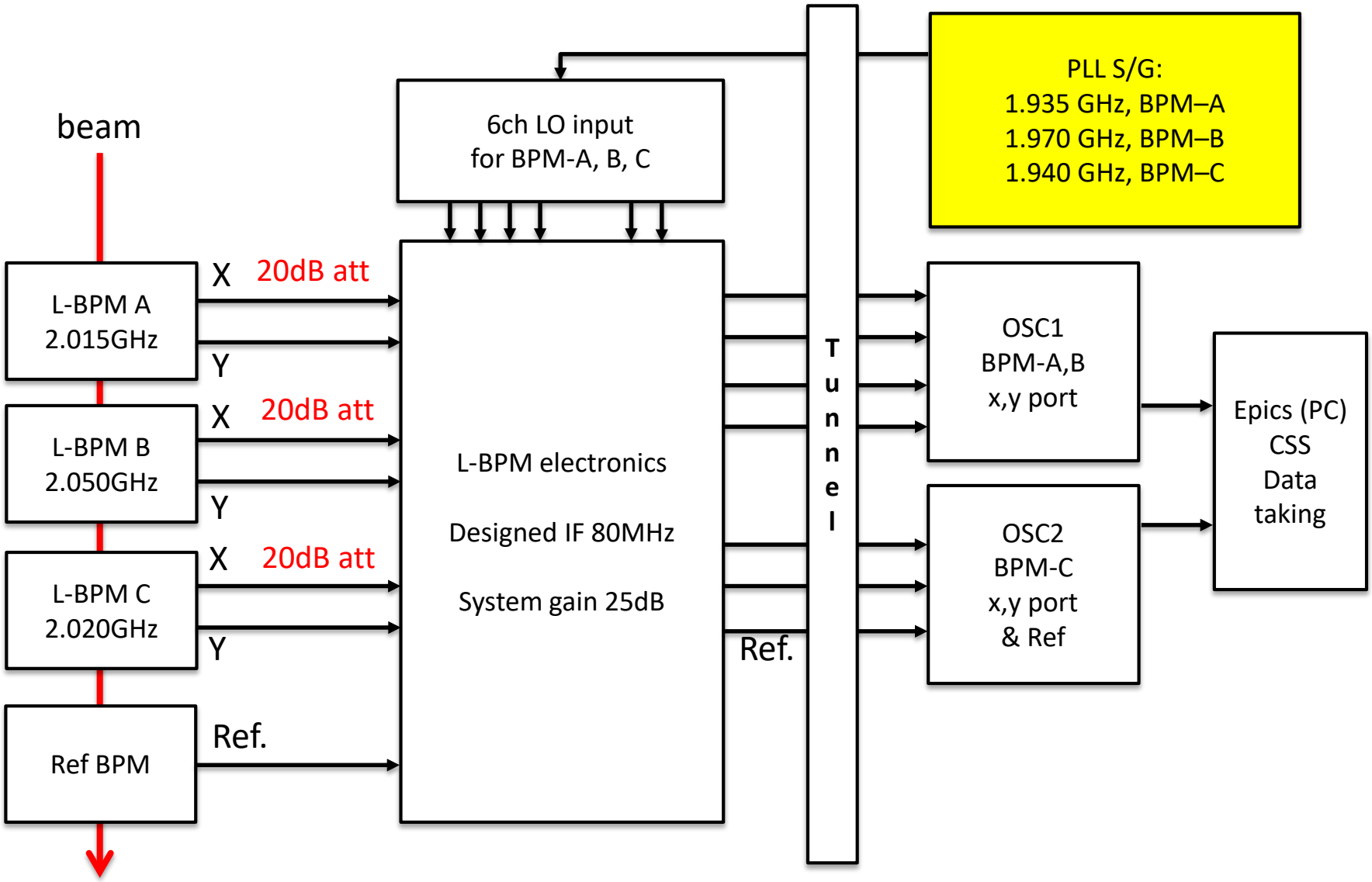
	Mean	RMS	σ (S-dev)
Frequency	1.9701 GHz	-	-
Cycle-cycle jitter	-	6.5004 ps	6.5004 ps

1.940GHz out
BPF: 1850~2040MHz

	Mean	RMS	σ (S-dev)
Frequency	1.94 GHz	-	-
Cycle-cycle jitter	-	5.3688 ps	5.3687 ps

PLL S/G:
1.935 GHz, BPM–A
1.970 GHz, BPM–B
1.940 GHz, BPM–C

Beam test scheme



Next study purpose

- L-band BPM resolution measurement by using new LO S/G.
- Second phase detector or new digital L-band BPM electronics development for beam position measurement.