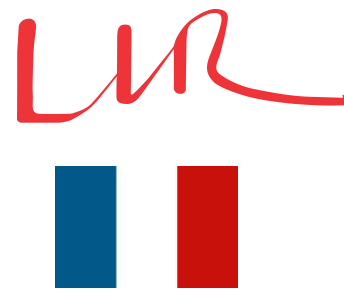


Status of Ecal-e

Roman Pöschl



On behalf of

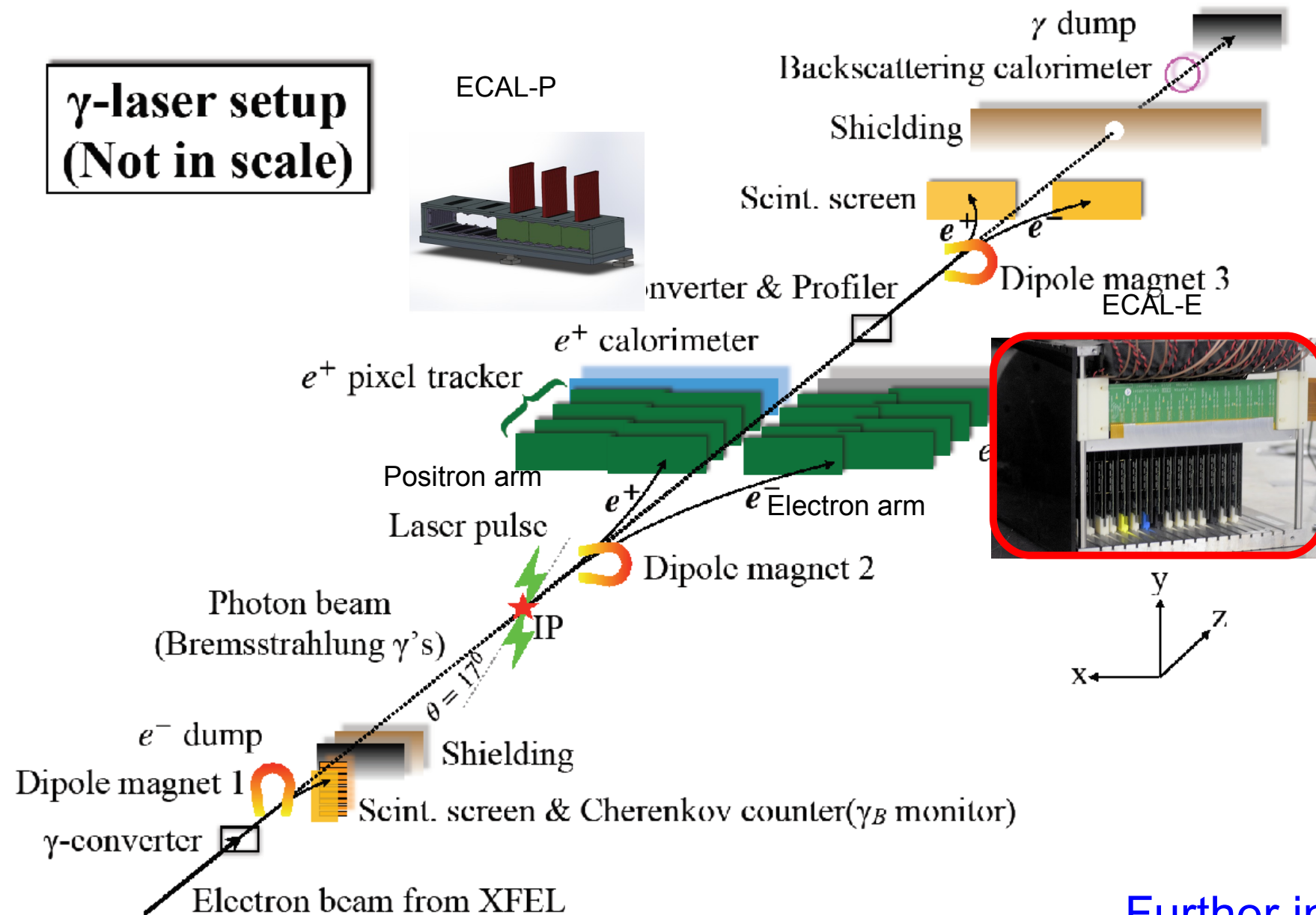


+ More groups that are not LUXE Members



Ecal Meeting – Valencia February 2024

Laser Und Xfel Experiment – QED in extreme fields



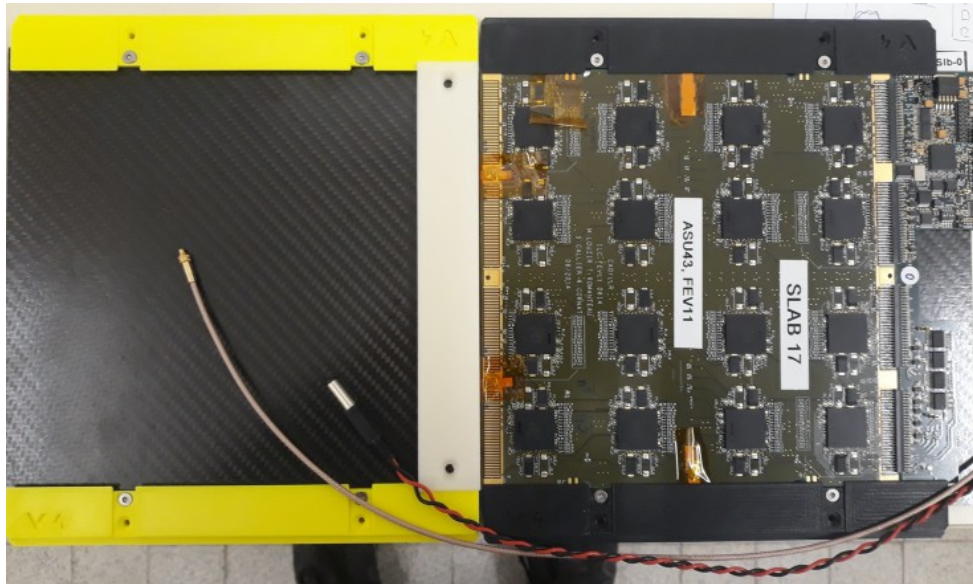
Granular calorimeters in positron and electron arms of spectrometer

- Our focus ECAL-E
- Main application electron measurement of Breit-Wheeler process in γ -laser setup
- Could also be used in early LUXE phase in case of delays of ECAL-P
 - *Dark photon search next to γ dump could be further option*
 - *Note here that already our short layers would have (almost) sufficient acceptance*
- Ideal application(s) of CALICE SiW Ecal technological prototype

Further interest by dark photon experiments
EBES (KEK) and Lohengrin (Uni Bonn)

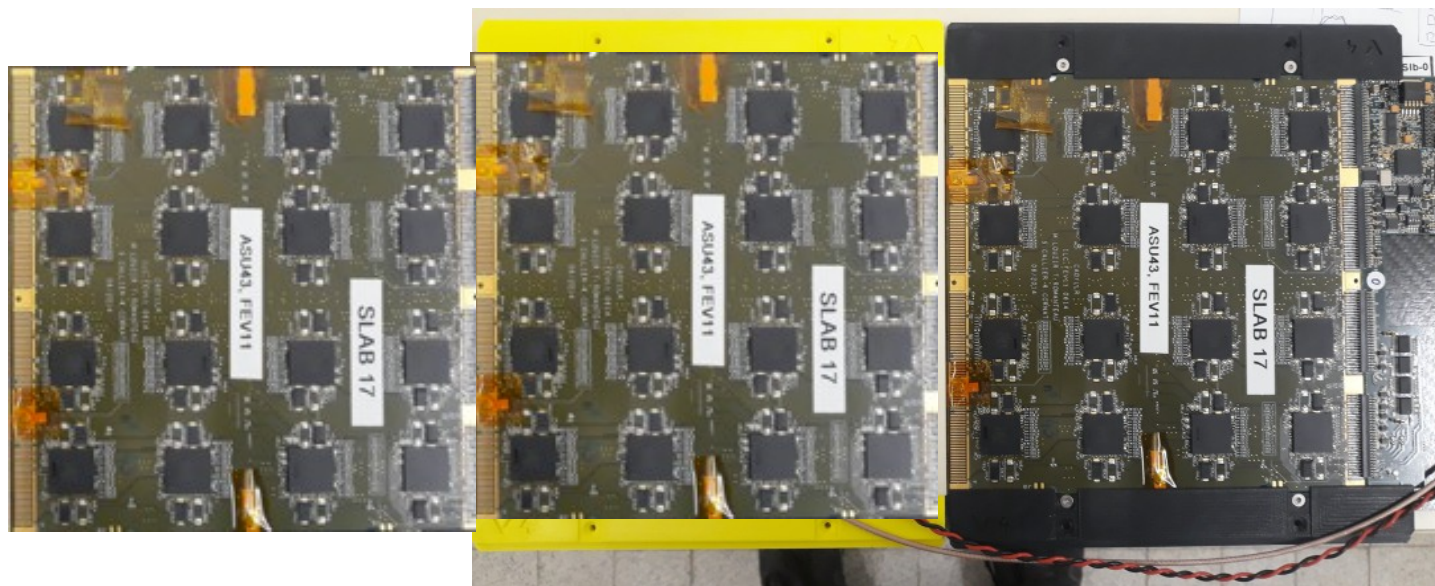
Plans (not only) for LUXE

Current: Tower of 15 $18 \times 18 \text{ cm}^2$ layers



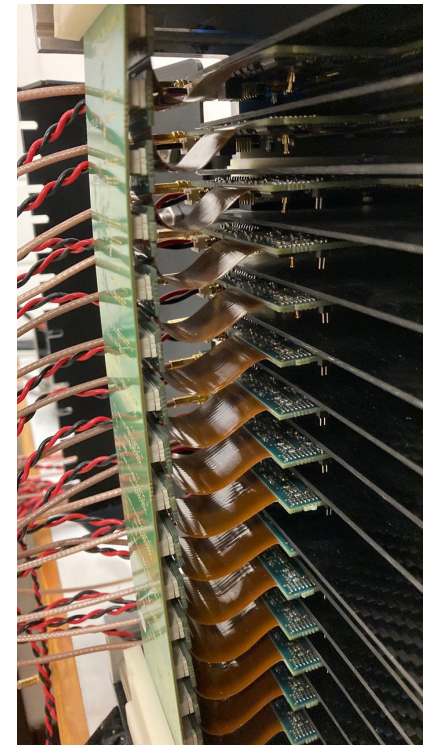
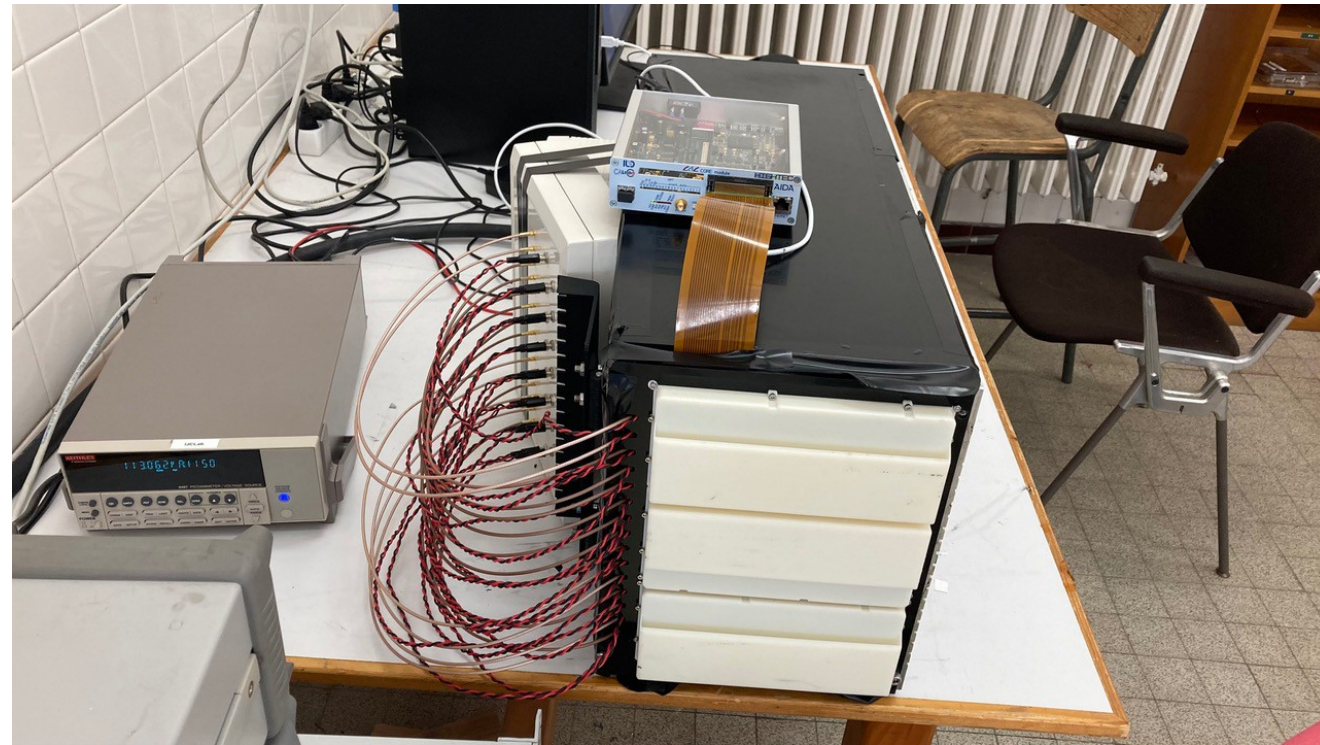
- Stack under revision
- Revision possible with small amount of funding
- Revised stack should/could be available during 2024

Future: Lateral extension to up to $18 \times 54 \text{ cm}^2$ layer (three towers), up to 15 layers of this type



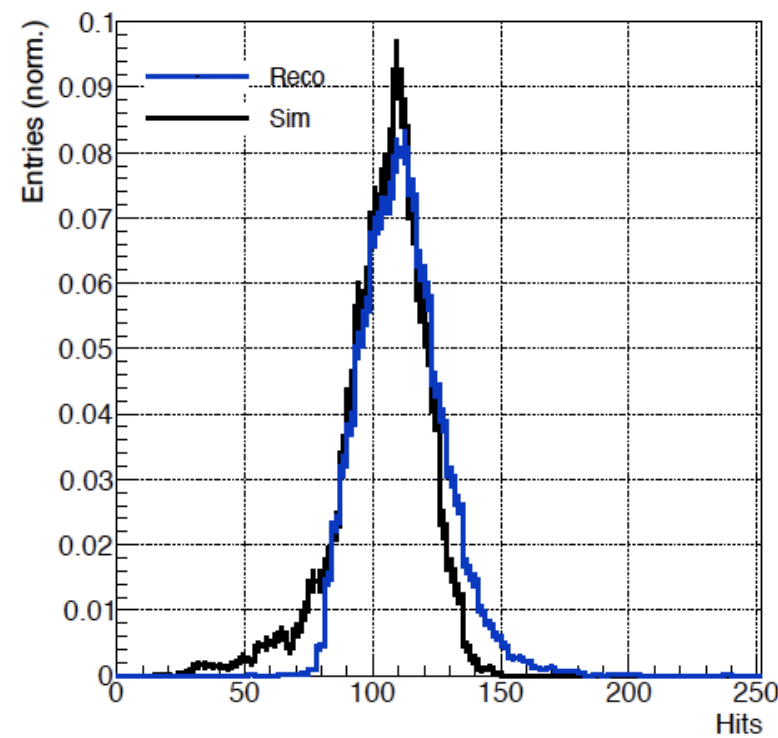
- Straightforward application of work for CALICE
- **Details of implementation in LUXE requires simulation study**
 - **=> need dedicated funding including person power!**
- LUXE stack = v0 of SiW ECAL engineering prototype

3

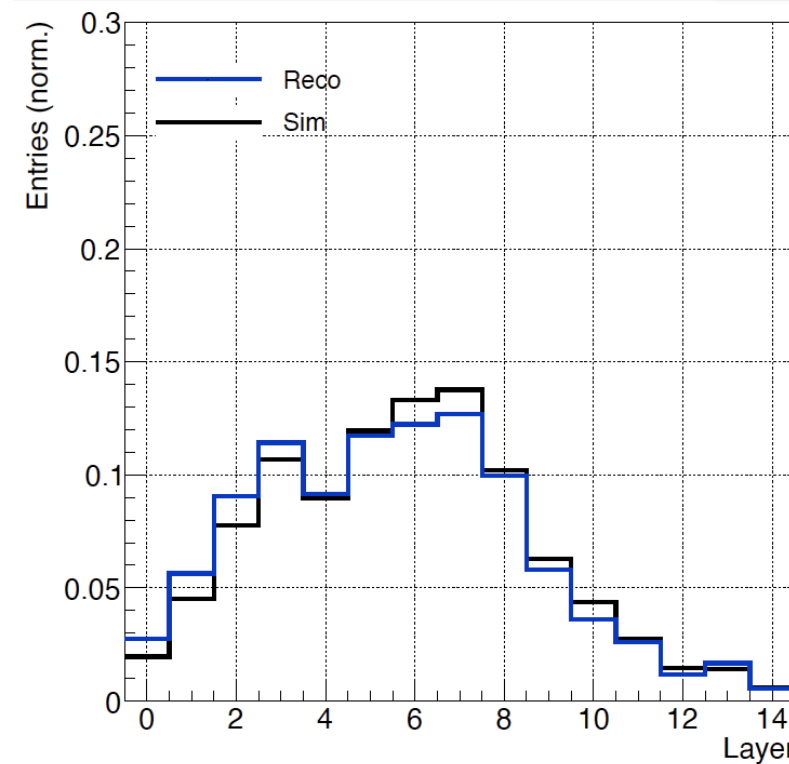


- 15 short layers equivalent to 15360 readout cells
 - Up to $21 X_0$
 - Overall size 640x304x246mm³
 - Flexible mechanical structure to adapt to beam conditions
 - Most of the layers produced 2016 - 2017
- Commissioned 2020-2022
 - ~450000 calibration constants for one ASIC feedback capa setting
- Testbeams (finally) in November 2021 and during 2022
- Mainly technical tests but also first real showers

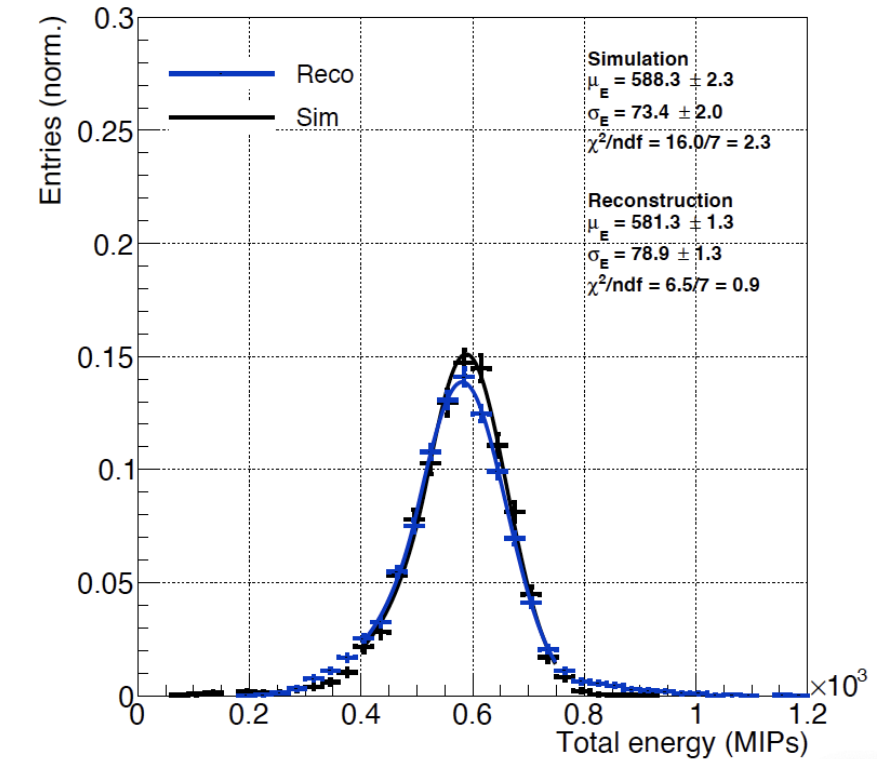
Total #of hits



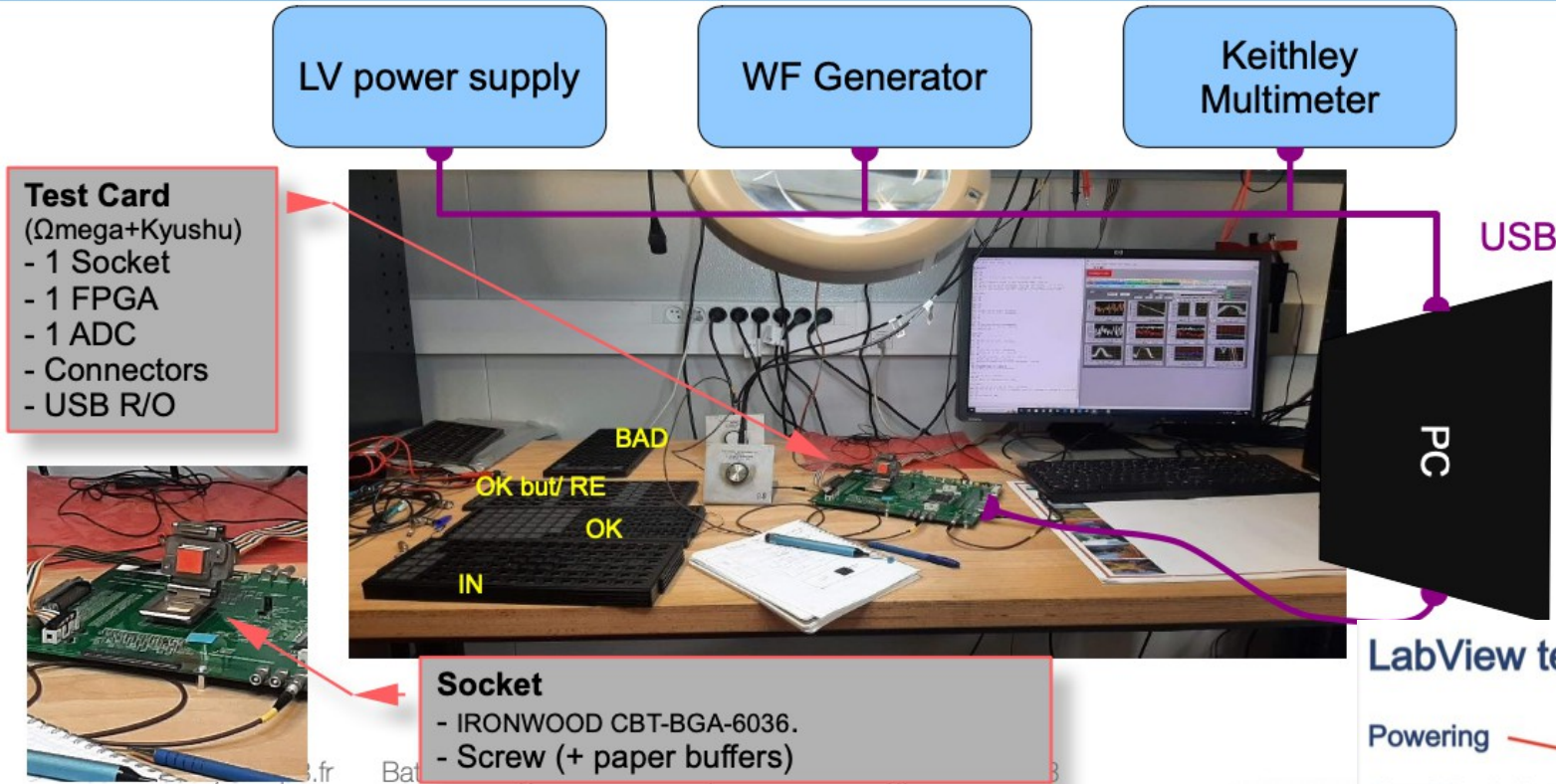
Hits/layer



(Total Energy)/MIPS



- Reasonable agreement between data and MC
- Energy resolution in ball park expected from simulation
- ILD: $\sigma E/E \sim 15\%/\sqrt{E}$ here $\sim 12-13\%$
 - reason: \sim factor 2-3 worse sampling ratios, “small” number of hits
- More analysis work required (including combined analyses)
 - Yuichi finished thesis -> person power needed

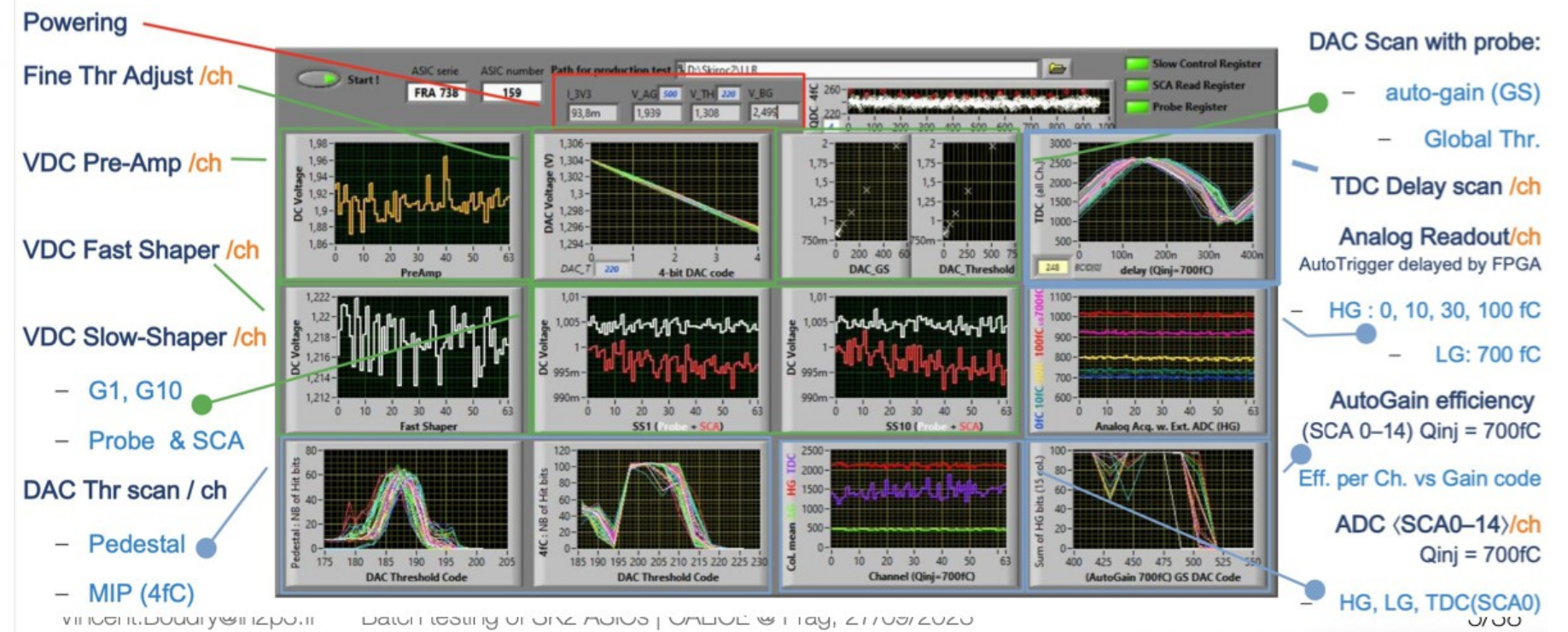


Testprotocol by OMEGA

LabView testing SW : Digital & Analogue probing 9 mins per ASIC (optim) © S. Callier

Testbench at LLR

- 151/400 SKIROCs tested until September 2023 (more since?)
- Satisfactory yield
 - Should be enough for
 - 9 18x54 cm² layers (to be verified)
- For more funding is needed
- DRD Calo run ?



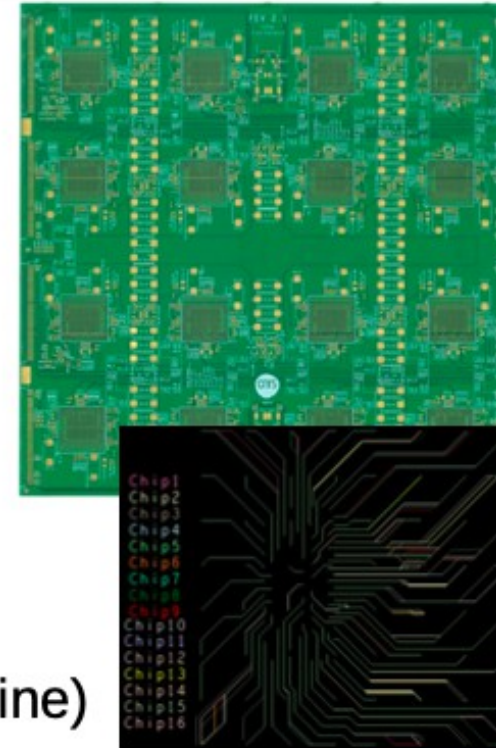
New FE boards

Improvements:

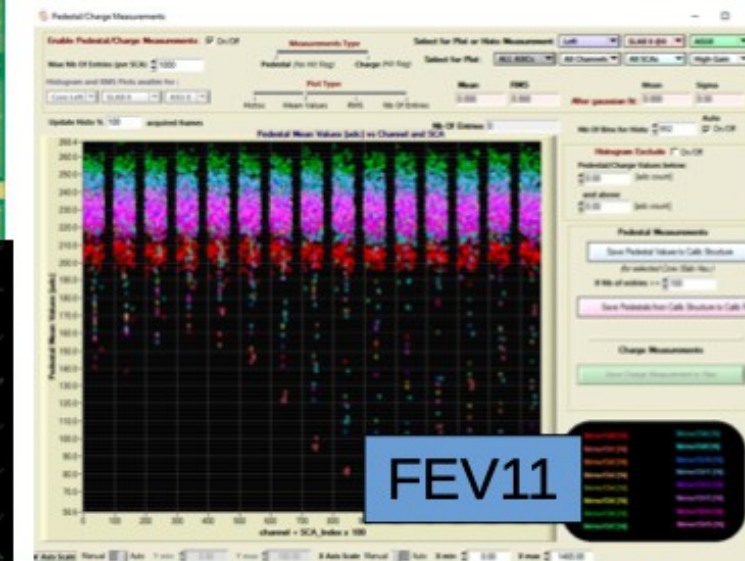
- Power distributions
 - Local power regulation
 - Local High Voltage filtering & Supply
- Signal distribution (buffering), data paths
- Monitoring (single ID, temp, probe analogue line)
- ASIC shielding/routing

Status:

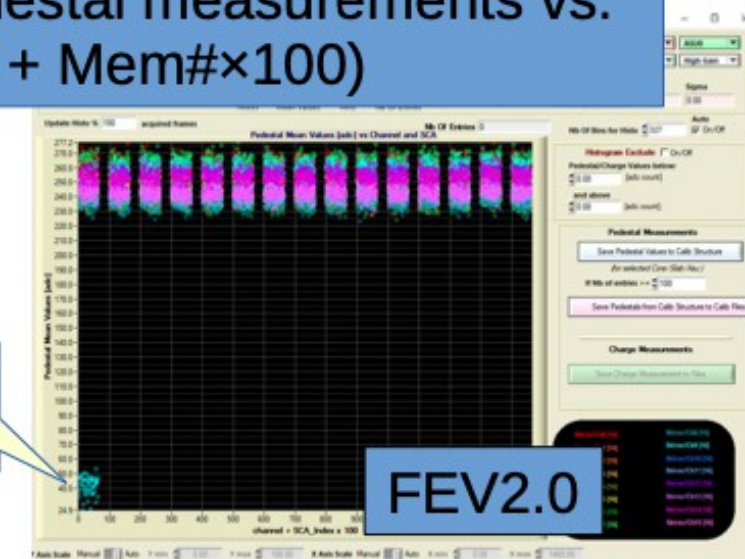
- pre-version 2.0 tested, minor corrections needed
 - Noise uniformity dramatically improved (ex: outliers in thr. / 20 !)
- version 2.1 produced, ... in metrology
 - before cabling, 2nd metrology, gluing, ...
 - All material available : ASICs being tested



LLR, IJCLab, LPNHE, OMEGA

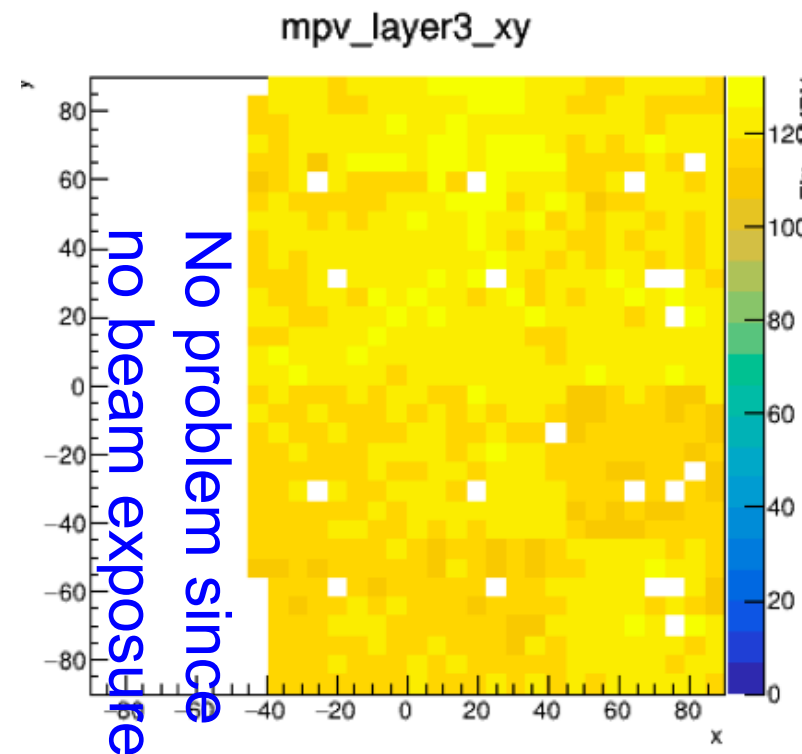
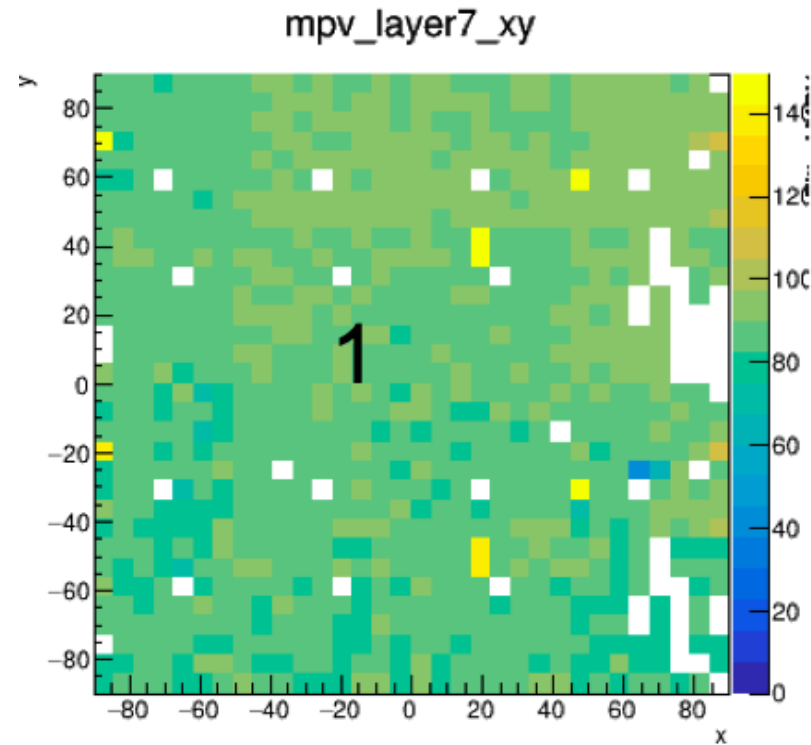


Pedestal measurements vs.
Ch# + Mem#×100)



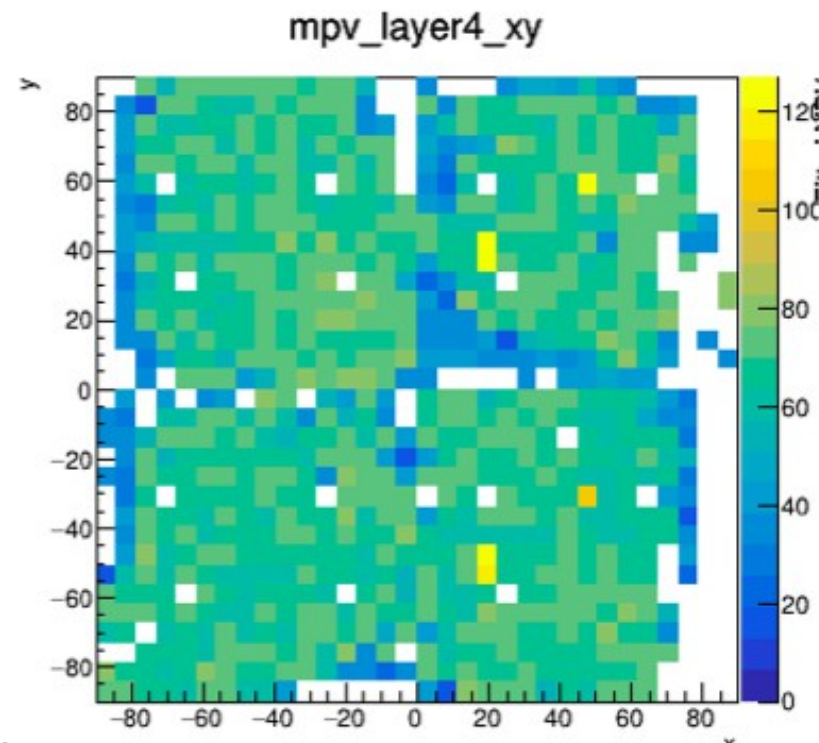
Goal: build 15 layer stack for 2024 based on these Boards

- Beam test at DESY in June
 - At least two new boards
- Four fully equipped PCBs available for (electronics) tests
 - One at IFIC (as far as I remember)
- Apart from « conclusion » on gluing (see later) need to ramp up with work in lab
 - Restart of test benches
 - Clarify issues with e.g. HV Kapton
 - Firmware modifications to test analogue probes
 - Tests could be carried out by internship (approved for ~May – June) under guidance of PostDoc



We have good layers ...

- Homogeneous response to MIPs over layer surface
- > 90% efficiency for MIPs
- Here white cells are masked cells due to PCB routing
 - understood and will be corrected

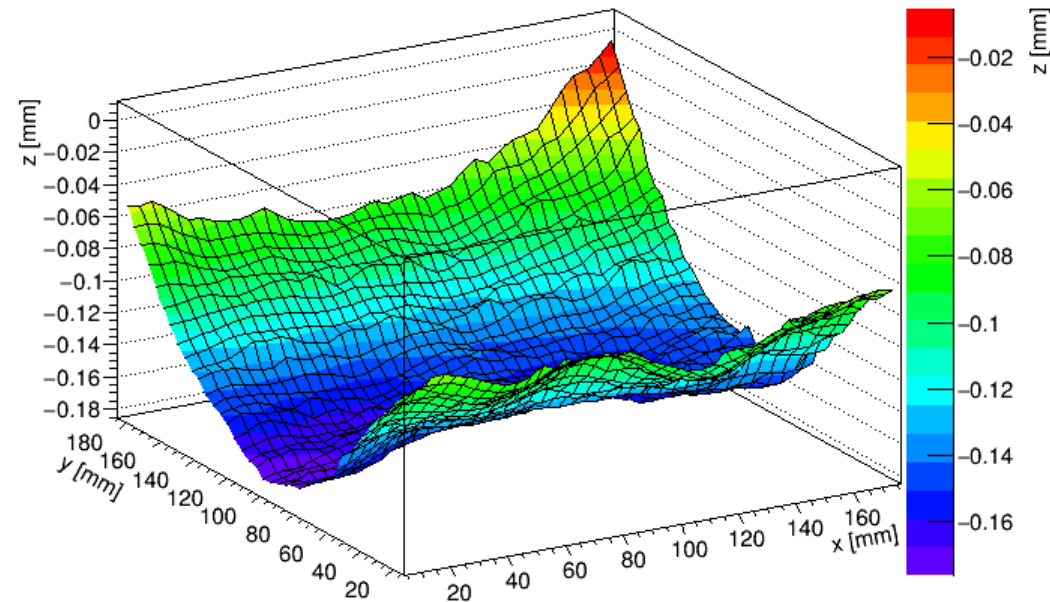


... and bad layers

Inhomogeneous response to MIPs

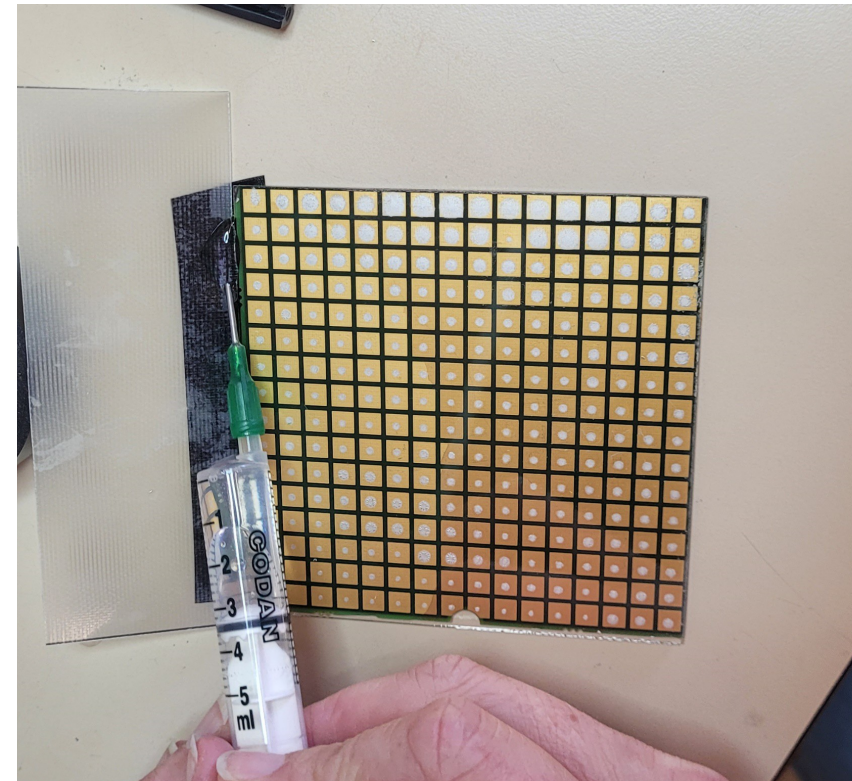
- Partially even no response at all, in particular at the wafer boundaries
- Visual inspection confirmed with electrical tests show that the sensor
- Got delaminated from the PCB -> glues dots have failed
- **Intensive topic of study**

Control of PCB Deformation



- We suspect mechanical deformation of PCB to be at the origin of the delamination
- => Control PCB shape at different steps of manipulation
- (e.g. After heating during component mounting)
- Work on consistency of measurements between IJCLab and IFIC

“Underfill”



- Low viscosity glue flows around glue dots
- Development in close contact with Epotek
- Seems to work -> “Solid piece”
- Requires second curing step at 80°C

“Double sided tape”



- Underfill “replaced” by double-sided tape
 - Holes with laser
- Encouraging first experience
- Details see Adrian's talk

Setup for mechanical tests



After breaking the glass



- Cards supported with underfill seems to resist better to external force than w/o
- Tests with double sided scotch started

- **Slow but steady progress on SiW Ecal**
 - Visible progress on data analysis
 - Need to ensure knowledge transfer since PhD student(s) are on leave
 - New PCBs available
 - Limited amount of ASICs available
 - Sensors for revision of CALICE stack available
- **Bottleneck is solution of wafer delamination issue**
 - Two solutions are studied in close cooperation between IFIC and IJCLab
 - ... plus support by DESY thanks to DMLAB
- **Funding**
 - Some funding available for stack revision
 - Limited additional person power due to recently approved French-German project CALO5D on machine learning and timing for granular calorimeters
 - Would be rather for Ecal core business, not particular for LUXE
 - Some results of project (might be) transferrable to LUXE
- **Dedicated work for LUXE would need supplementary funding of the order of 150-250 kEUR plus person power**
 - Difficult to spot at this moment
 - Minor support for prototyping by labs and local funding calls (lottery but not impossible)
 - Therefore, only commitment is that we'll do our best to revise the existing CALICE stack
 - May benefit from activities in DRD Calo (e.g. ASIC purchase)

Backup