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ECAL-p readout status

This research was funded by the National Science Centre, Poland, under the grant no. 2021/43/B/ST2/01107

ECAL-p LUXE workshop, 13-17 February 2024, Valencia

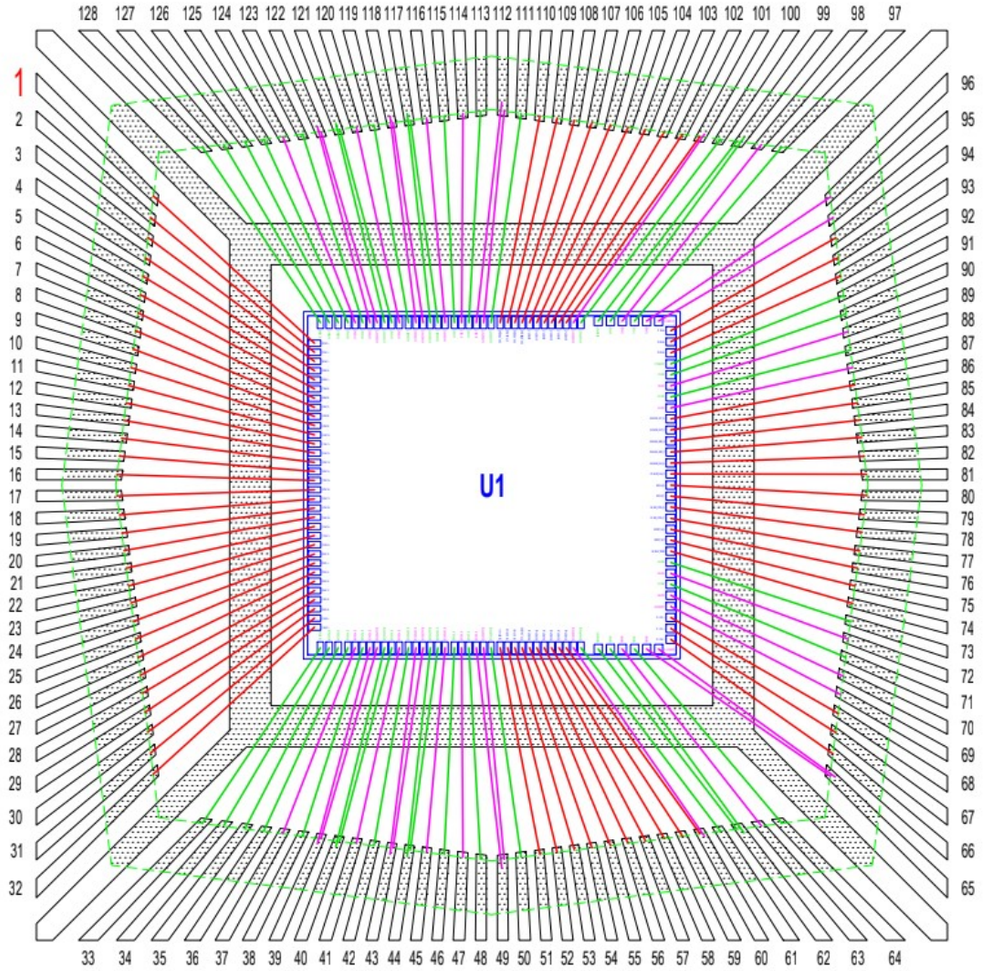
Agenda

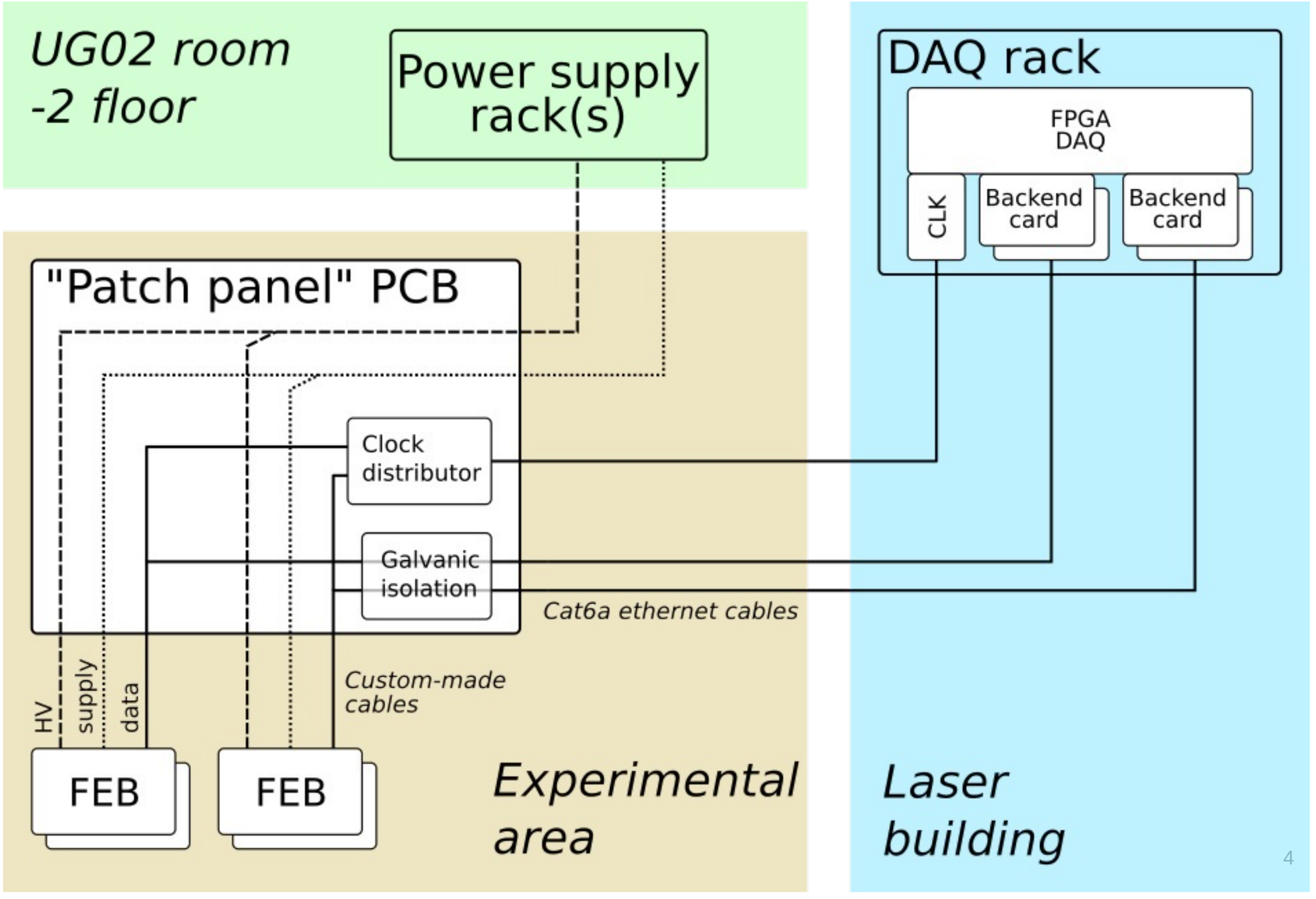
- Readout hardware
  - Architecture
  - Status
- FEB design
  - Mechanical issues

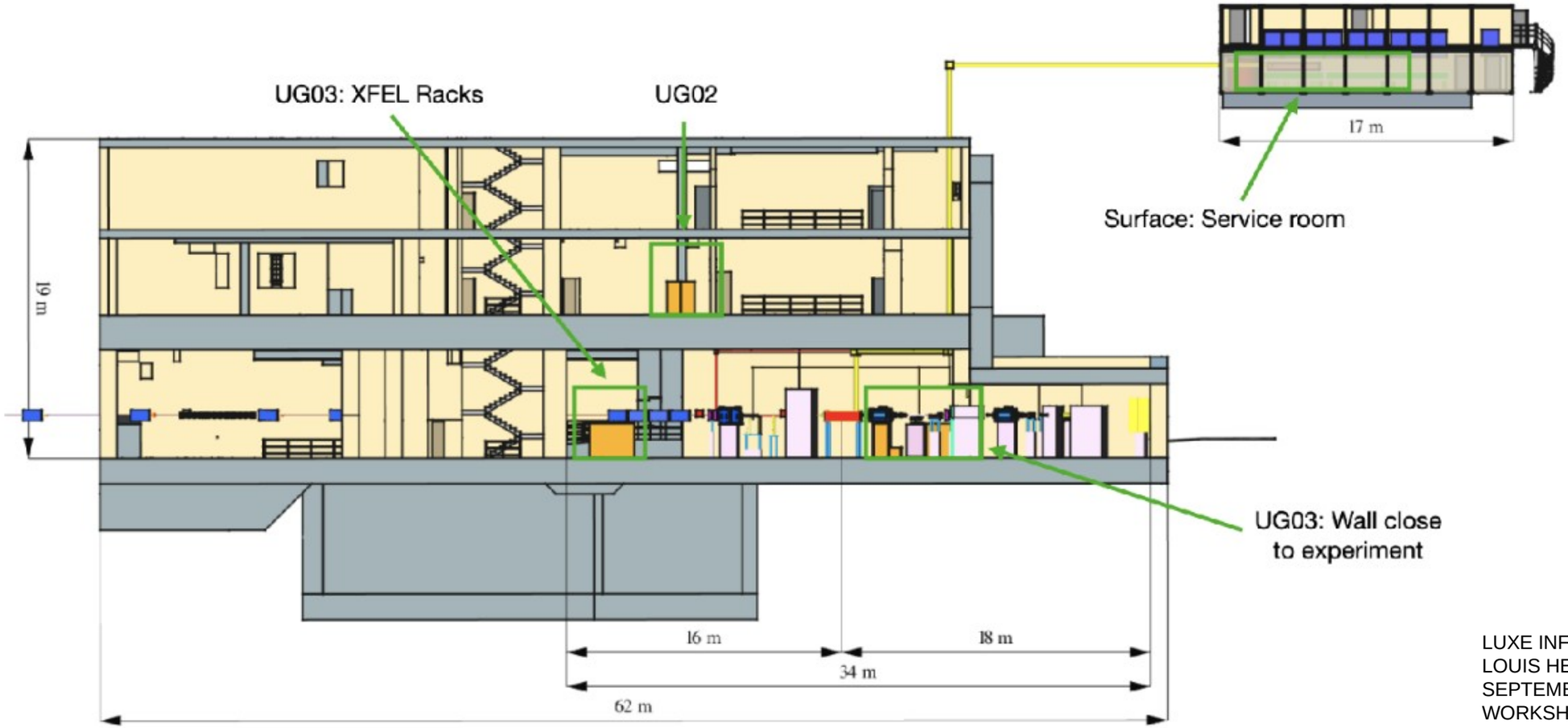
Current readout status – FLAXE ASIC

- Technical details about packaging fixed (bonding scheme, marking)
  - We did not get the final confirmation and shipping date yet...

- The expected shipping date of ~1000 packaged ASICs is around ~April 2024




UG02 room
-2 floor
Power supply
rack(s)
DAQ rack
FPGA
DAQ
CLK
Backend
card
Backend
card
"Patch panel" PCB
Clock
distributor
Galvanic
isolation
Cat6a ethernet cables
HV
supply
data
Custom-made
cables
FEB
FEB
Experimental
area
Laser
building



LUXE INFRASTRUCTURE
LOUIS HELARY
SEPTEMBER 4TH 2023 - LUXE WORKSHOP

- **Position foreseen for backend electronics:**
  - In UG03 (not accessible during data-taking).
  - In UG02 (potentially accessible at every time but for short stay and space limited).
  - In surface building (further away), space to be understood.

Area	Length
UG03: Side north wall	7 m
UG03: EuXFEL rack	16 m
UG02	26 m
Surface: service room	≈ 50 m

Readout scheme – FLAXE communication and control

FLAXE ASIC requires six signals:

- Main clock (20 MHz)
- Acquisition control (aka. pre-trigger)

} Common for all FEBs

- Reset (slow, asynchronous, no timing requirements)
- Data bus:
  - SCK (data clock, independent from main clock)
  - MOSI (data from FPGA to FLAXE)
  - MISO (data from FLAXE to FPGA)

} One bus per FEB
40 buses in parallel

We decided to distribute separate reset lines to each FEB:

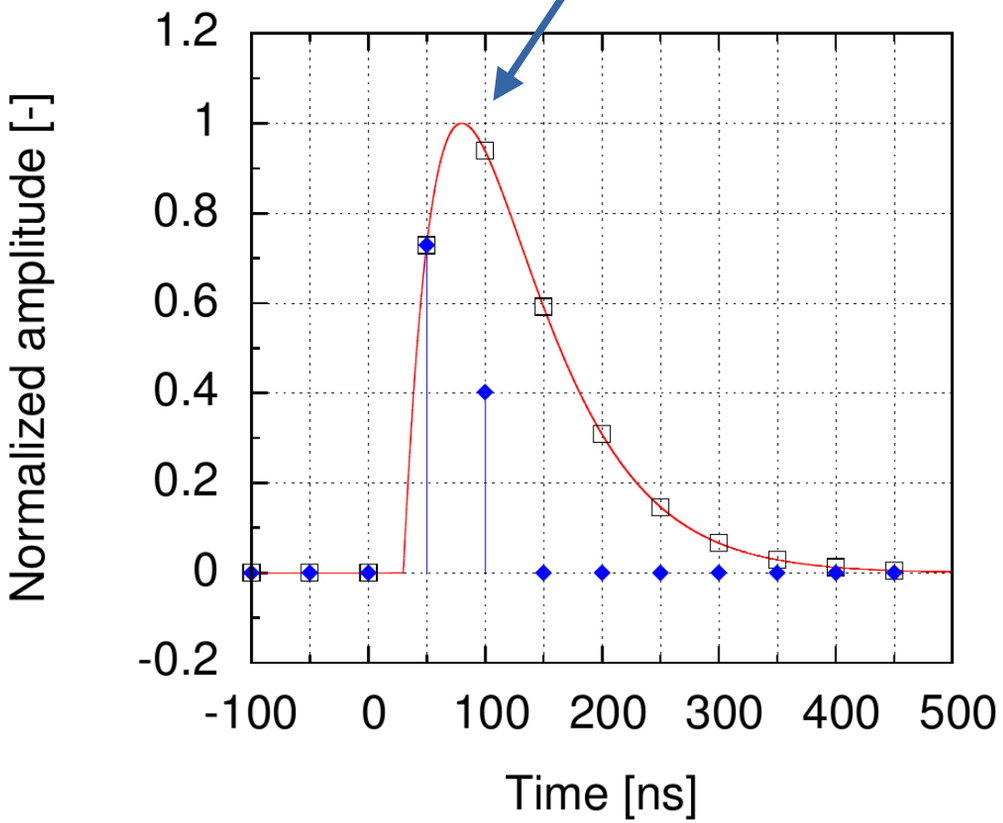
- We can reset only a selected FEB, not the whole ECAL-P
- It will be difficult to achieve higher granularity (like one reset per sensor or ASIC) and we do not think it is necessary

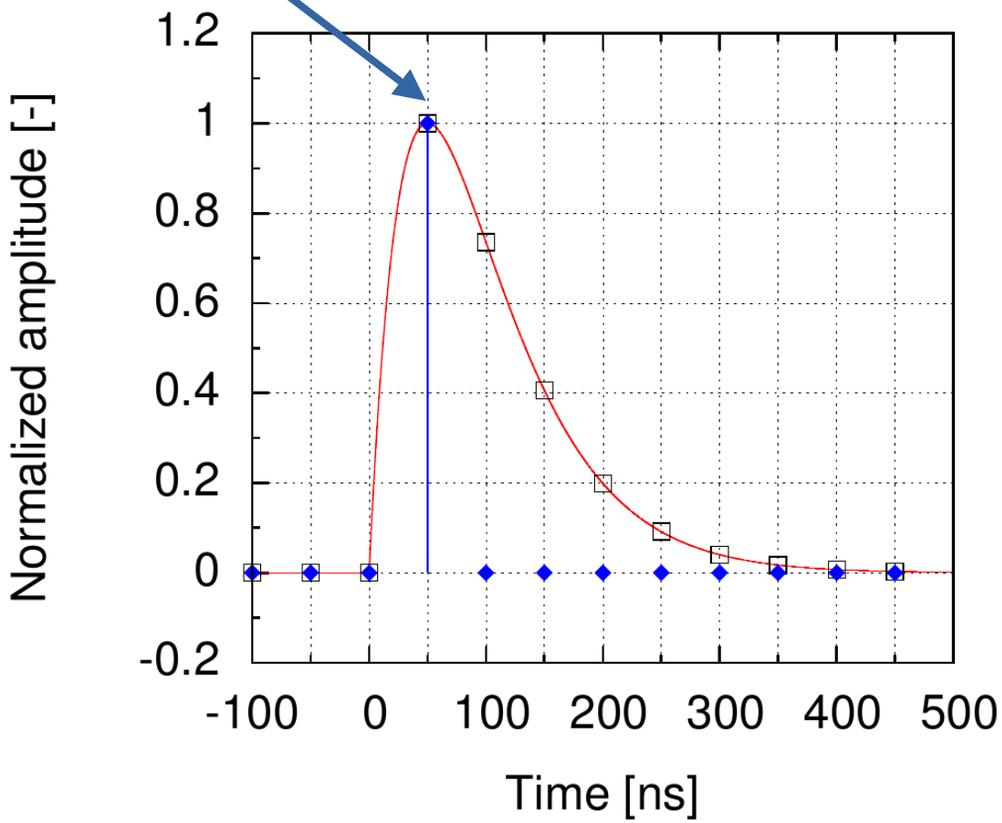
Readout scheme – sampling modes

We should try to run readout in synchronous mode during the experiment:

- One sample directly at pulse maximum → amplitude from simple pedestal subtraction → better SNR

We still need asynchronous mode (and reconstruction) for testbeam and cosmic muons





Readout scheme – sampling timing and clock requirements

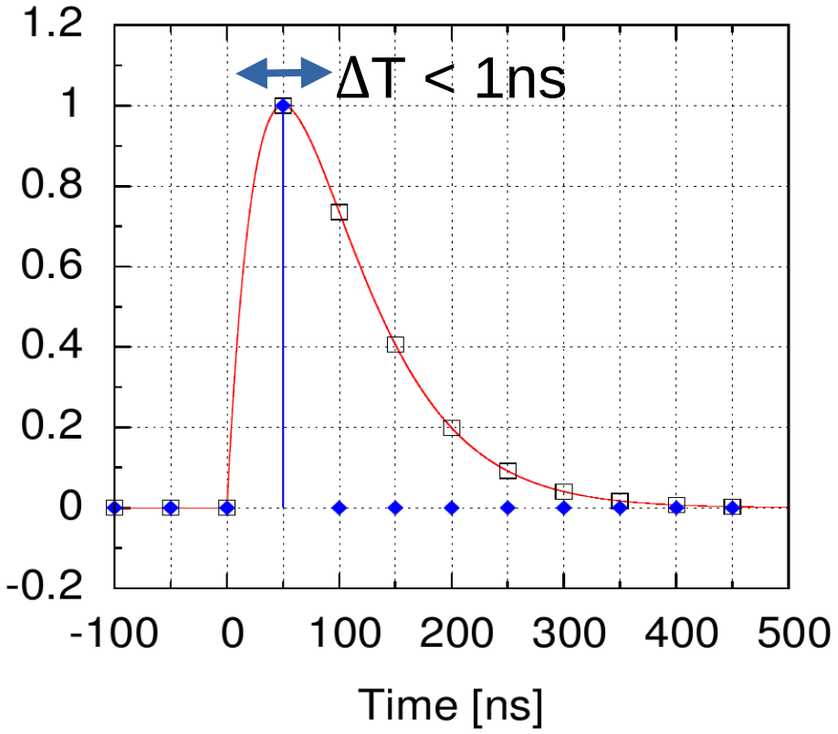
For synchronous mode we need precise clock distribution:

- Skew between all FLAXE ASICs in whole ECAL-P
- Clock phase drift in respect to machine clock

} below 1 ns (±500ps)

We need to create clock from main 45MHz LCS clock with configurable phase shift

- Sophisticated PLL directly controlled by the FPGA

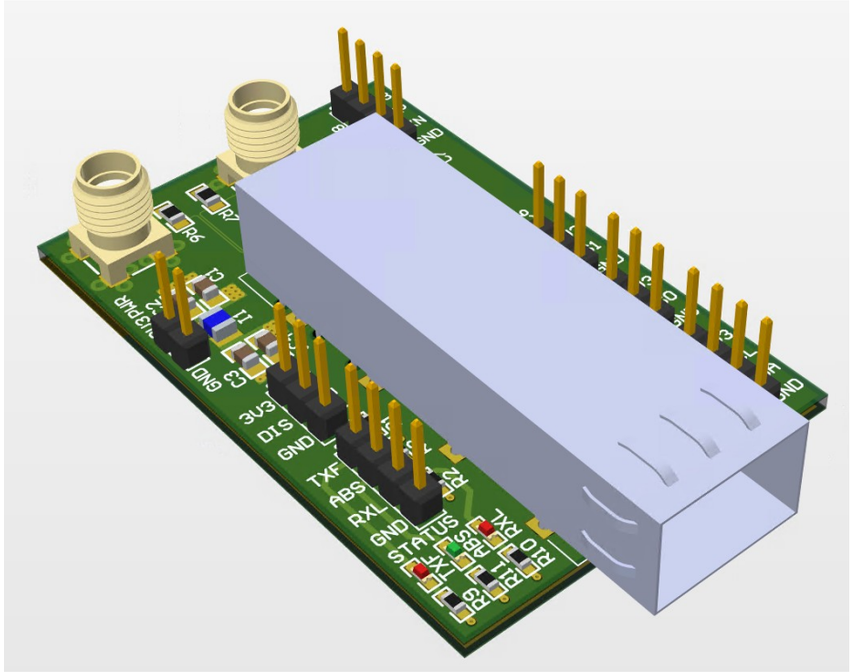


- We need to create 40 copies of the clock, one per each FEB
- To keep the skew and drift as low as possible we should keep the length of the parallel clock distribution as short as possible → clock distributor close to the FEBs

Data and clock transmission medium tests - setup

Test setup:

- Signal generator providing 20MHz square wave
  - Custom “SFP breadboard” PCB,
    commercial 1Gbps SFP modules (GBC PHOTONICS SF-MM85055D-GP, FOUNDRY TXN31111000001),
    50m long multi-mode fiber (OM2 Qoltec 54030)
  - 50m long, low-loss 50Ω coaxial cable
    Siva Cavi RF240LTA (1.4 EUR / m)
  - 50m long Cat6a RJ45 cable
    Logilink CQ3143S
- High speed scope measuring the signal delay and jitter
- Climatic chamber



Test program

- Delay and jitter measurements for temperature in range from -20 to +50 ^{o}C
- *Delay and jitter measurements for varying humidity (not done yet)*

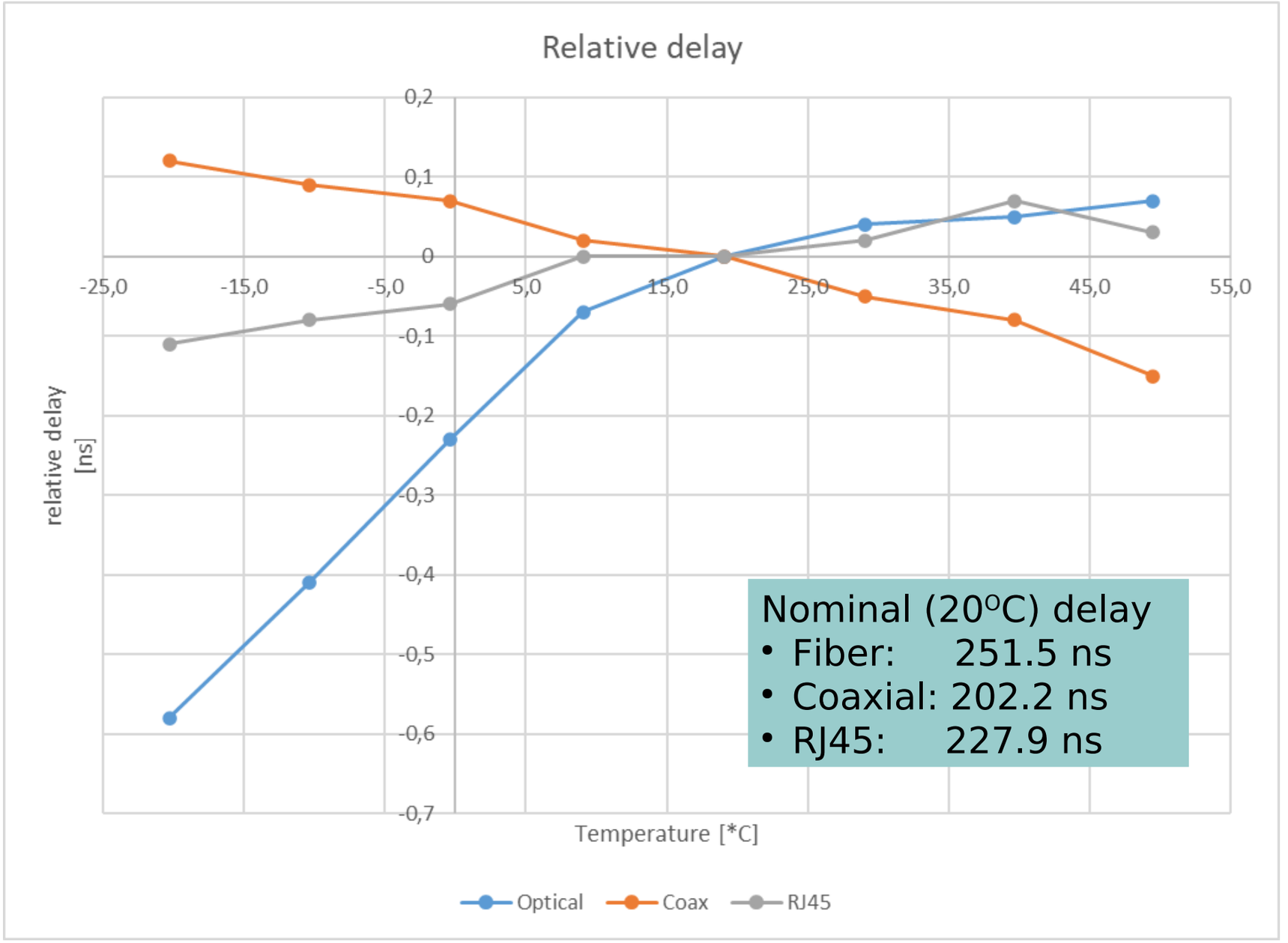
Data and clock transmission medium tests - results

Delay drift

All three medium have drift <1ns

Fiber is surprisingly the worst one ranging from -0.6ns to +0.1ns!!

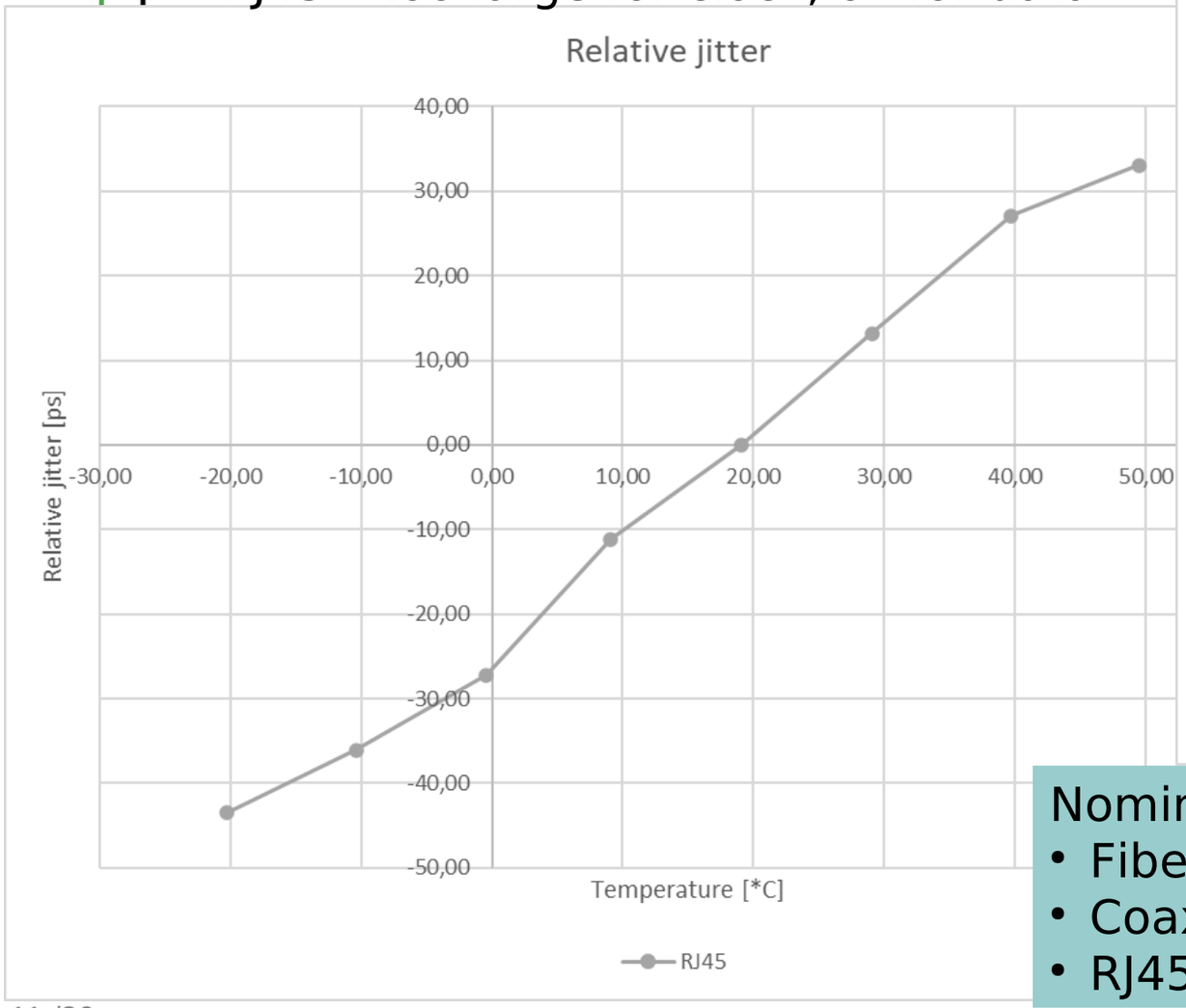
Coaxial cable seems the best choice, with drift < ±150ps

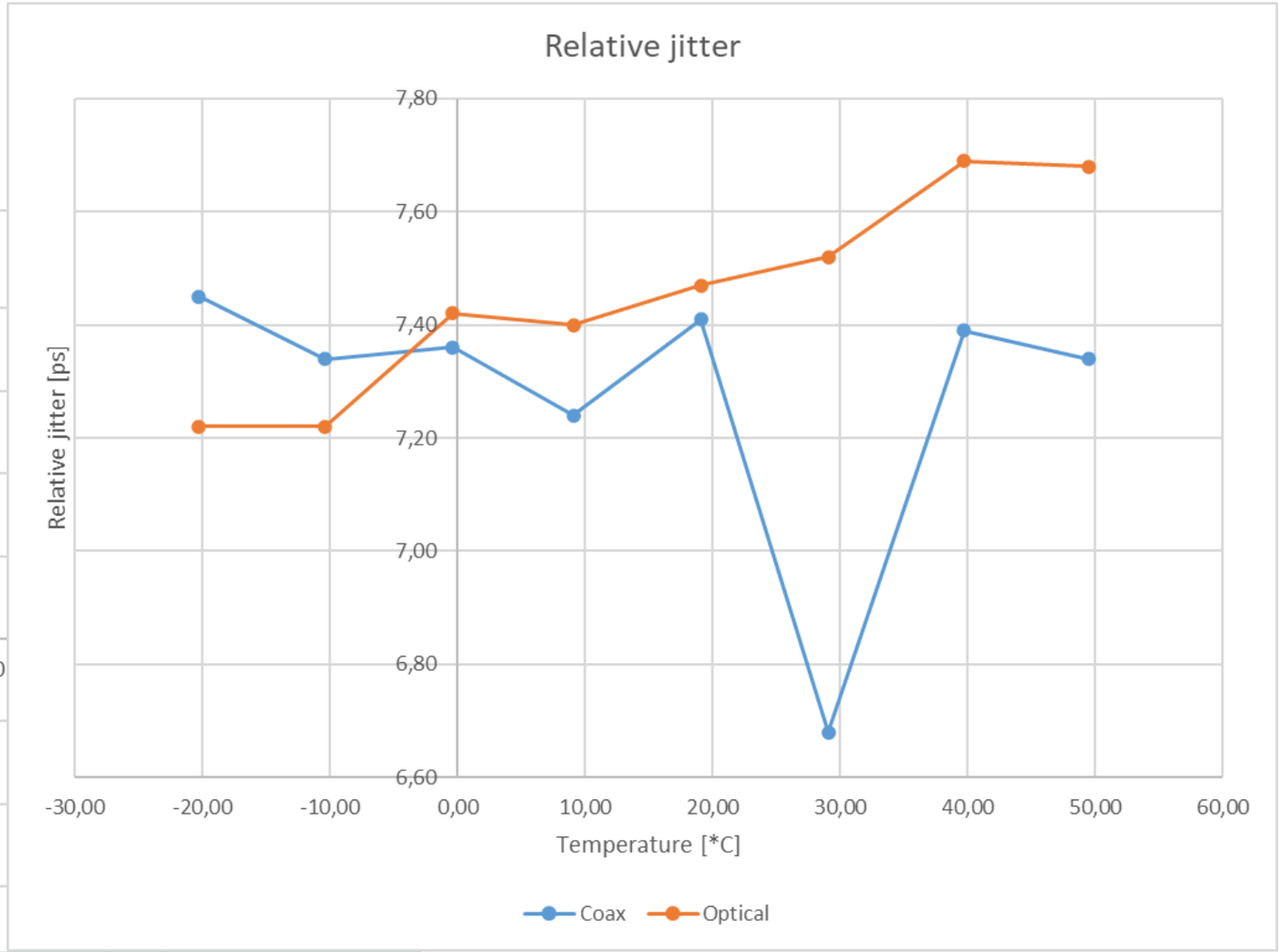


Data and clock transmission medium tests - results

Relative jitter

RJ45 – too large for clock, ok for data





Nominal (20°C) jitter
- Fiber: 7.4 ps
- Coaxial: 7.4 ps
- RJ45: 161 ps

Fiber, coaxial – ok!

Data and clock transmission medium tests - results

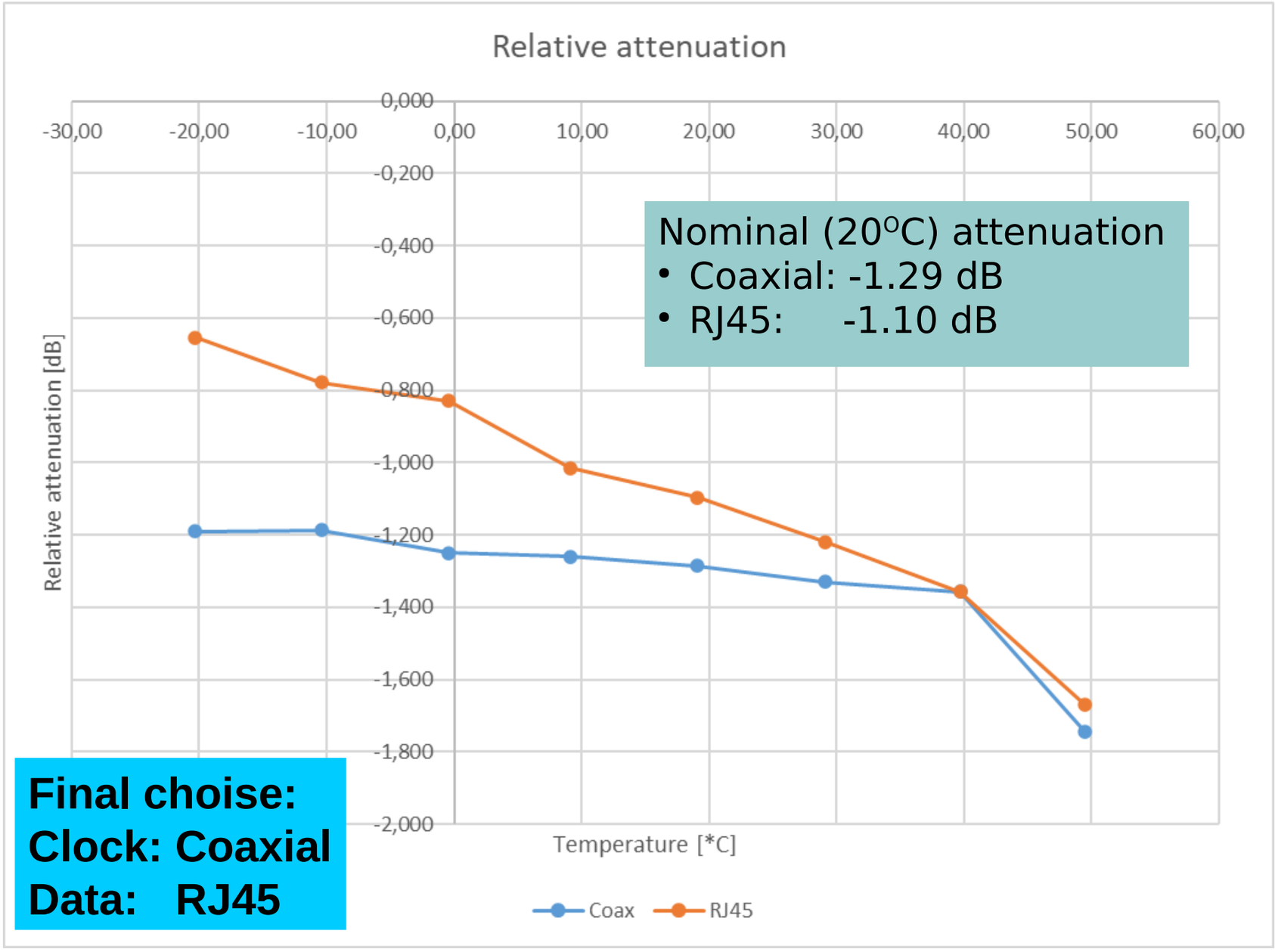
Attenuation

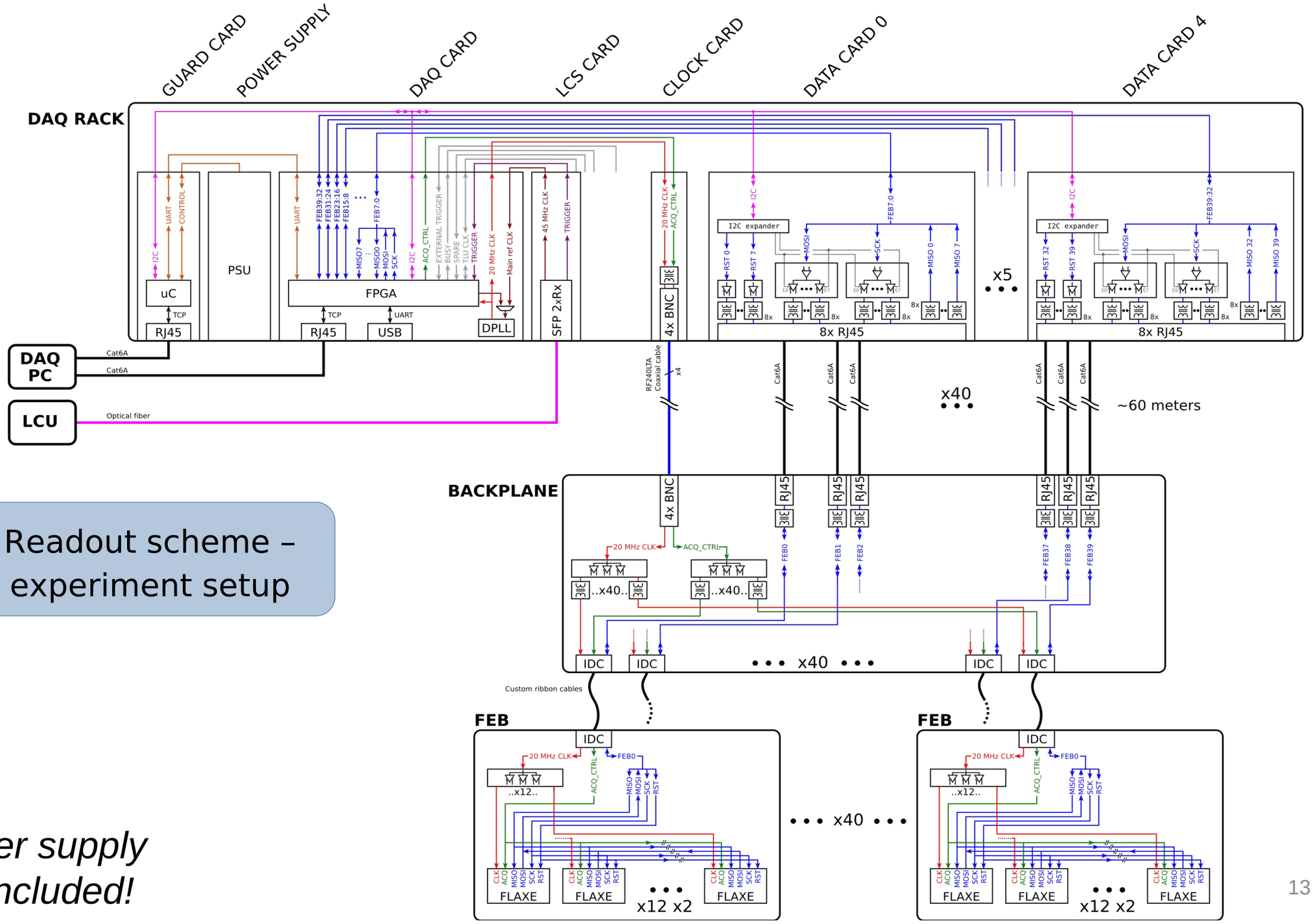
Both coaxial and RJ45 attenuation well suited for clock and data transmission:

Worst case is -1.8dB (80% of original amplitude) after 50m.

We can expect less than -3.5dB (67% of the original amplitude) after 100m

No attenuation data for fiber since SFP receiver recreates the electrical signal

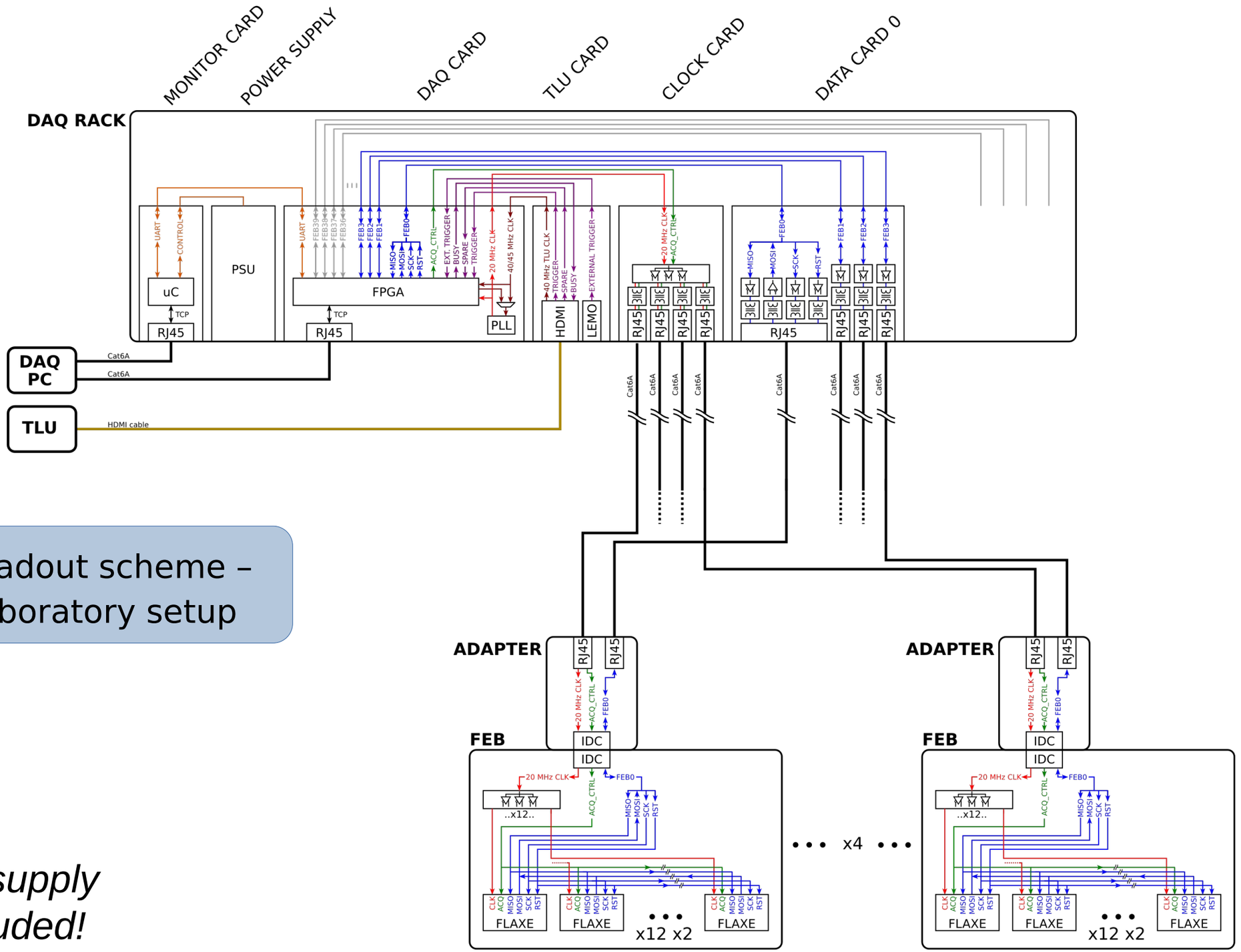




Readout scheme – experiment setup

Power supply not included!

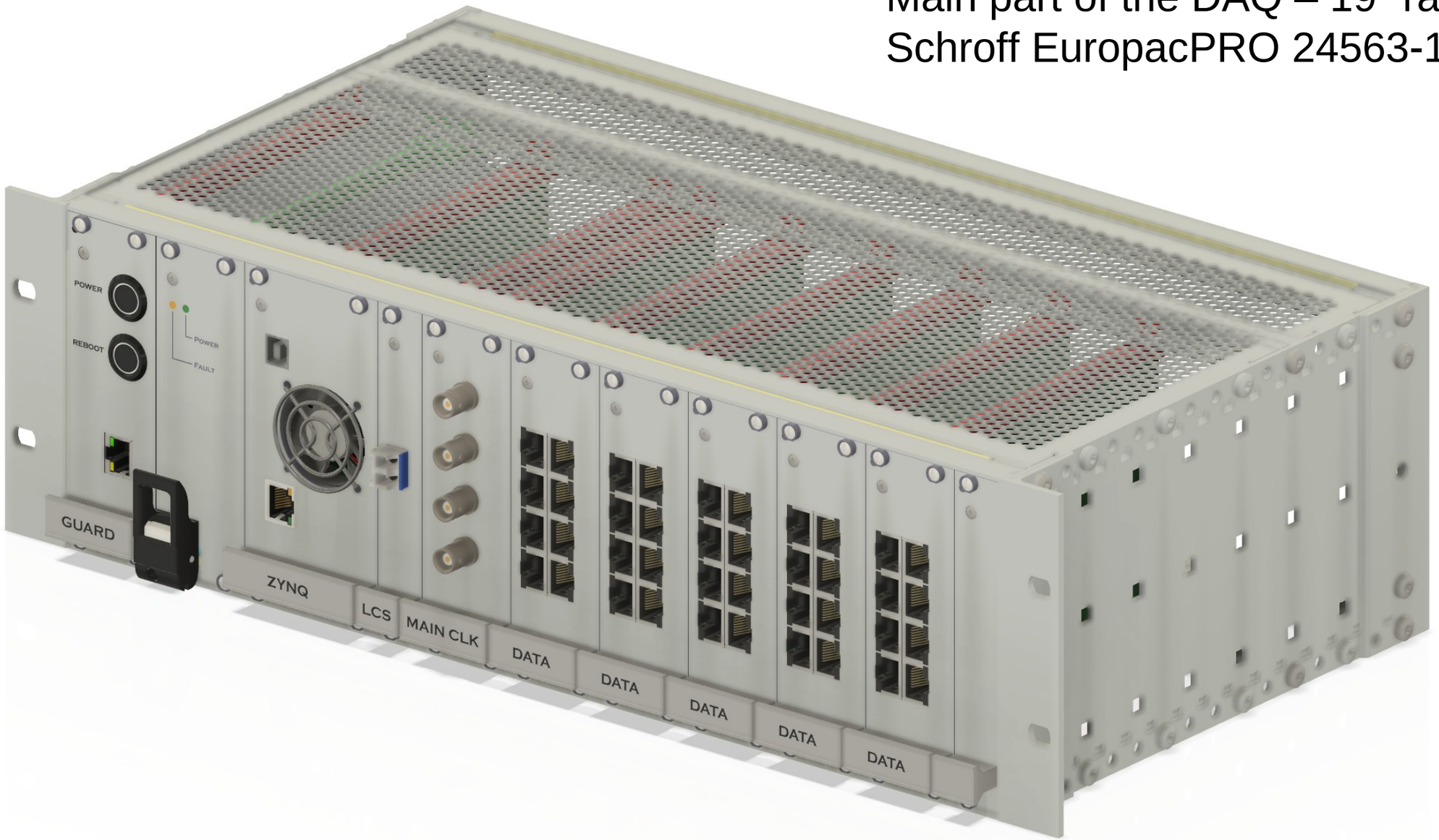
Readout scheme – laboratory setup



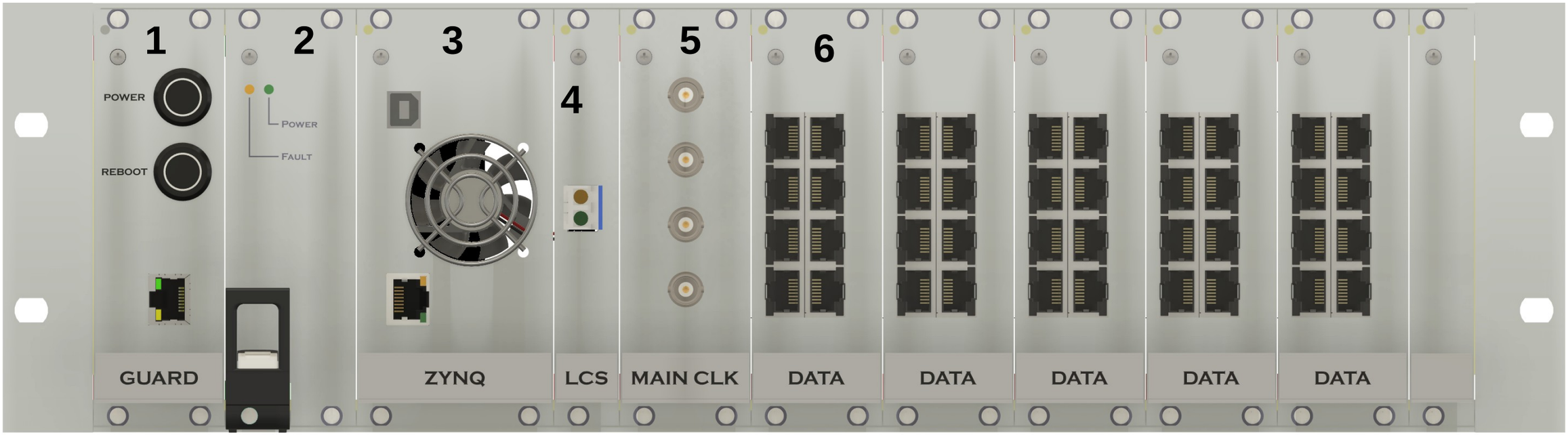
Power supply not included!

Readout hardware – DAQ rack

Main part of the DAQ – 19” rack
Schroff EuropacPRO 24563-142

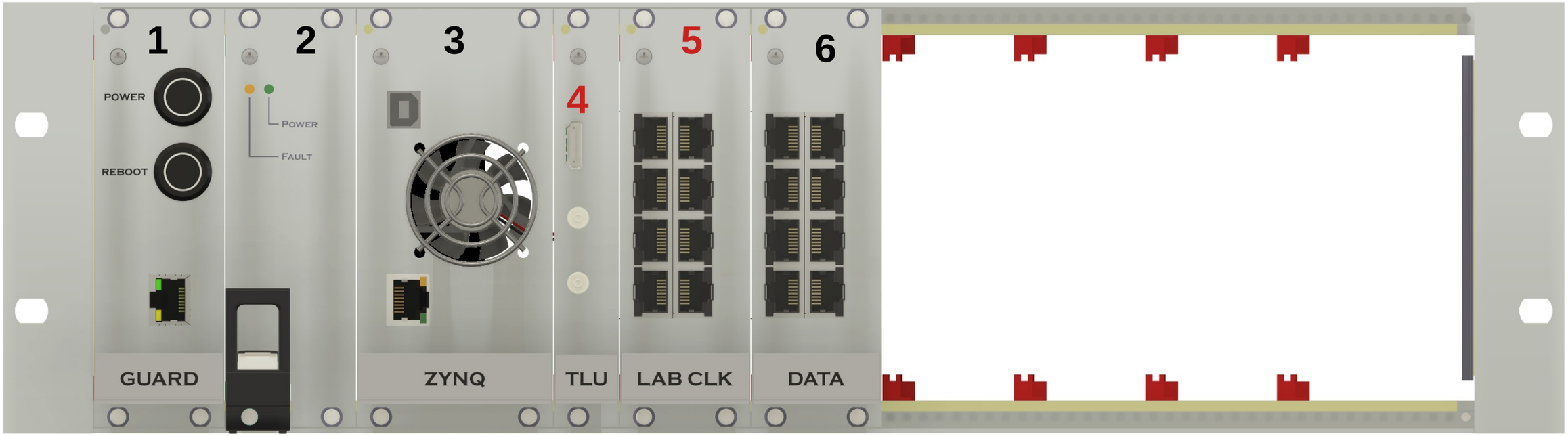


Readout hardware – DAQ rack – experiment configuration



1) Remote power supply control and DAQ health monitor
2) Rack power supply – Schroff CompactPCI 250W, 13100-141
3) Main DAQ card with Zynq Ultrascale+ FPGA on a Trenz TE-0808 module
4) LUXE Control System (LCS) slave card – *not defined yet by LUXE DAQ group…*
   Receives LUXE system clock (45MHz) and pre-trigger from the main DAQ system
5) Main FLAXE clock (20MHz) and acquisition control signals 50Ω coaxial driver
6) FEB data and reset interface. Each card serves eight FEBs → 5 cards in total for full-stack calorimeter

Readout hardware – DAQ rack – laboratory configuration



1) Remote power supply control and DAQ health monitor

2) Rack power supply – Schroff CompactPCI 250W, 13100-141

3) Main DAQ card with Zynq Ultrascale+ FPGA on a Trenz TE-0808 module

4) TLU interface card (for testbeam) with external trigger inputs (for laboratory)

5) Main FLAXE clock (20MHz) and acquisition control distributor for laboratory tests. Serves eight FEBs at the same time, but without <1ns precision (no synchronous sampling)

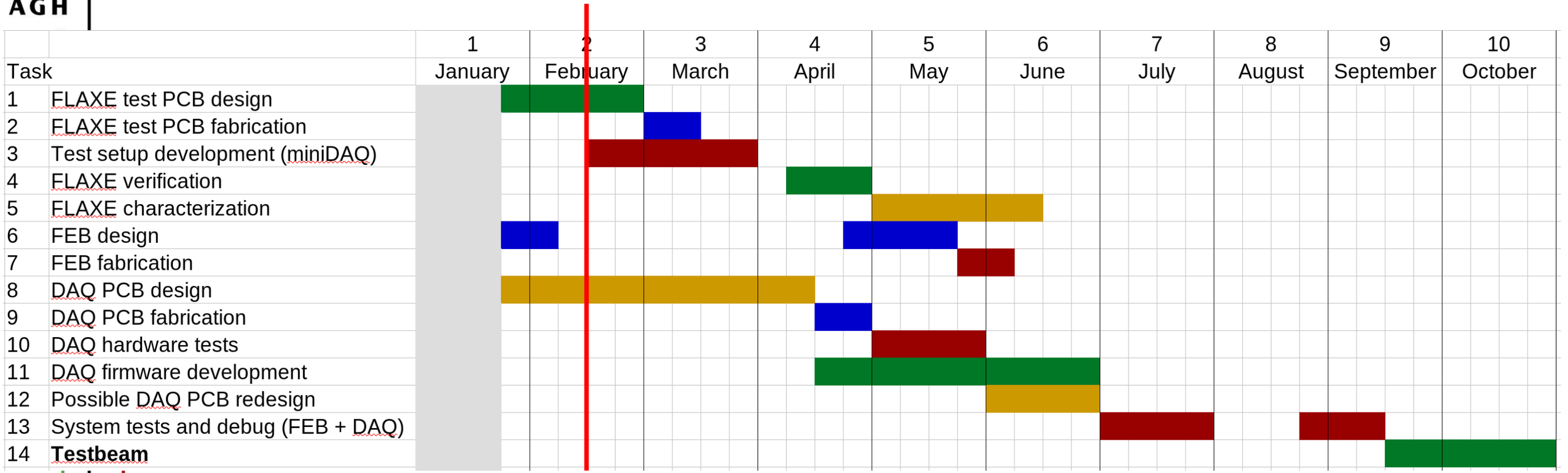
6) FEB data and reset interface. Each card serves eight FEBs

Readout hardware – PCB status

	Concept	Schematic	PCB
FLAXE test board			
FEB	85%	60%	30%
Patch panel	50%		
Rack (cards)			
Backplane			
Guard			
DAQ		30%	
LCS			
TLU		10%	
Clock experiment		10%	
Clock laboratory		10%	
Data			

- Most of the PCBs in the schematic design phase
- Two already completed – backplane and guard card
- One absolute mystery – LCS slave card – not needed soon, so it can wait for the final decisions about the overall LUXE DAQ system

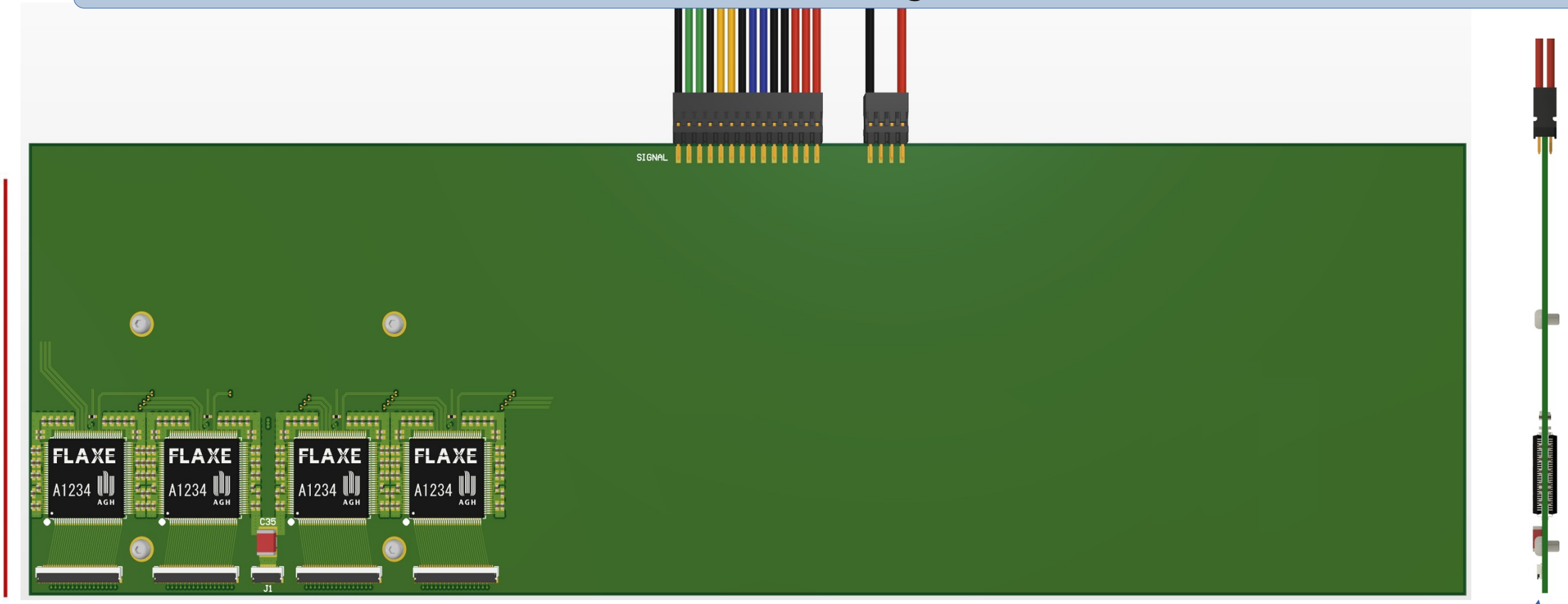
Current readout status – schedule



Our goal is a testbeam at the end of Q3 2024 with at least one FEB (layer)
We should discuss the testbeam program in more details...

We have now a huge showstopper at AGH:
Due to administrative issues, we are currently unable to purchase any electronic parts or outsource PCB manufacturing.
Our administration searches for the solution, but we may need to find an alternative solution within our collaboration...

FEB design



Most challenging parts done:

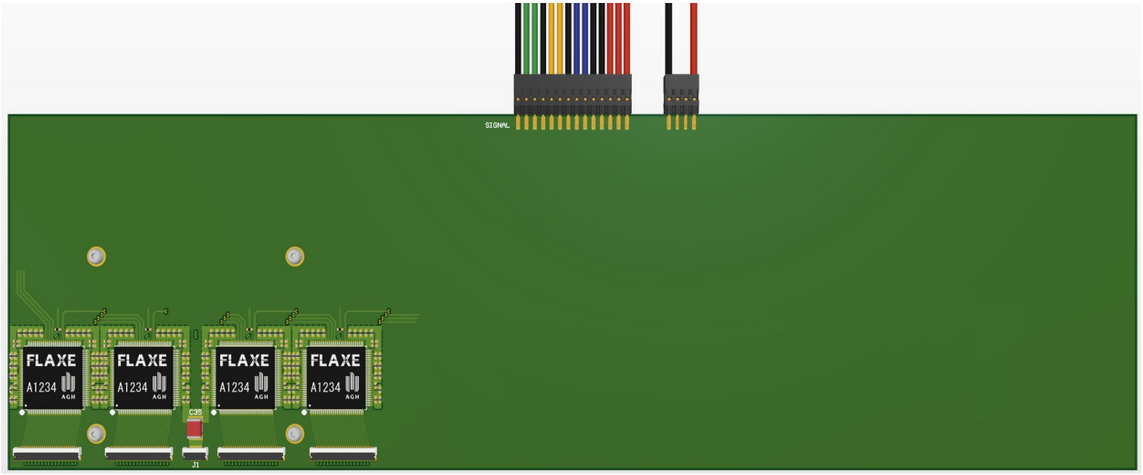
- Eight FLAXE ASICs and their decoupling fitted within 90mm (sensor width)
  ASICs placed “back-to-back” on top and bottom layer of the PCB (see side view)
- Backplane connector fitting the 4.5mm pitch found
- Fanout connectors arranged – required by fanout deisgn

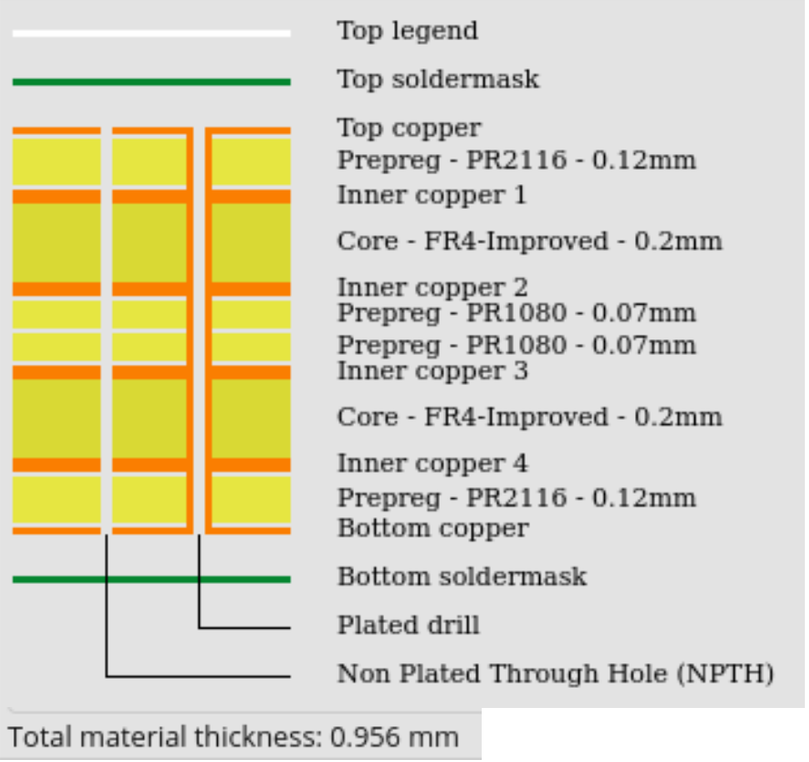
FEB design

- Only one sensor populated so far:
  What will the distance between neighboring sensors on the layer?

- No power supply scheme yet:
  What will be the HV granularity:
  - **One HV supply channel per FEB?**
  - **One HV supply channel per sensor?**

- PCB thickness: **1mm**
  - It is absolute minimum for 6-layer PCB with controlled impedance (differential pairs routing on top/bottom layers) from all manufacturers.
  - 0.8mm is possible only for 4-layer PCB (with controlled impedance), but this would significantly deteriorate FLAXE supply distribution (larger noise...)

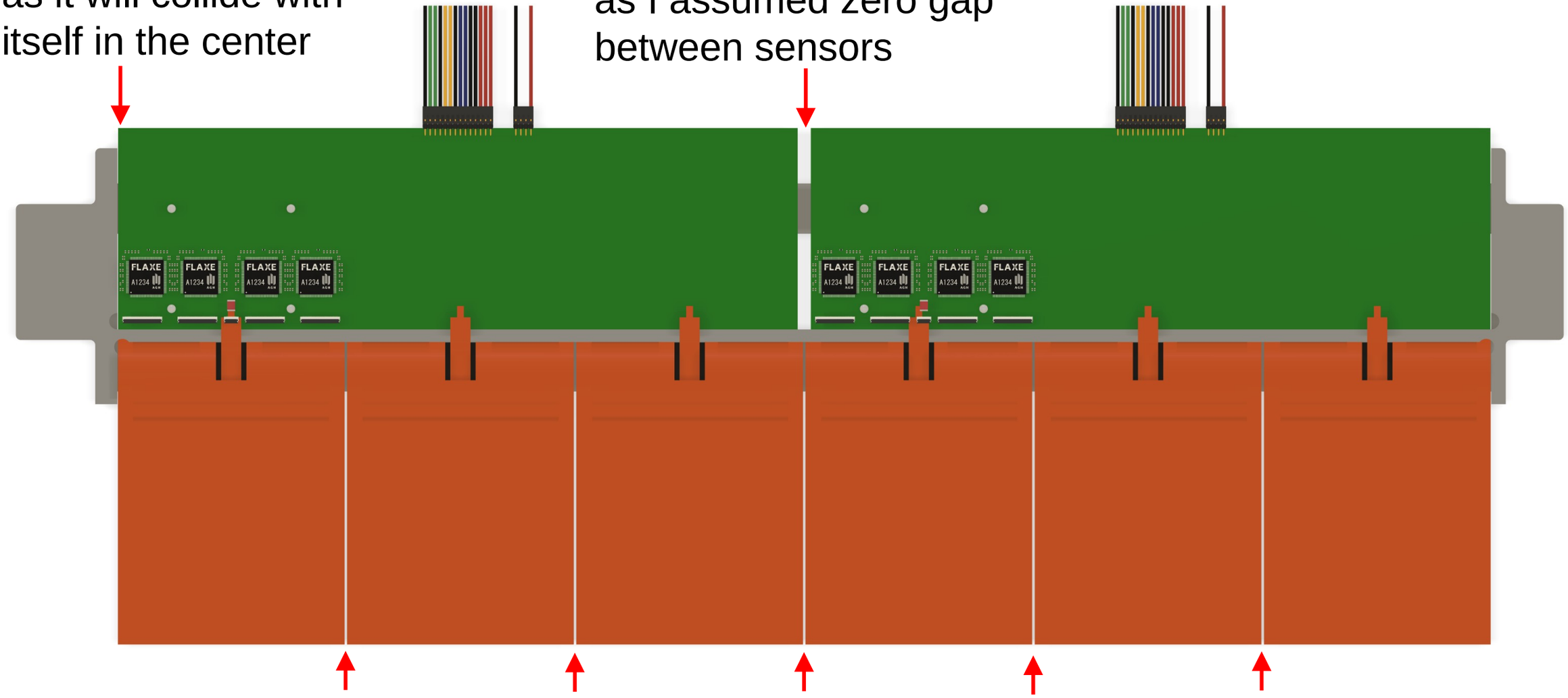




FEB design – “Tframe” design

PCB cannot be wider as it will collide with itself in the center

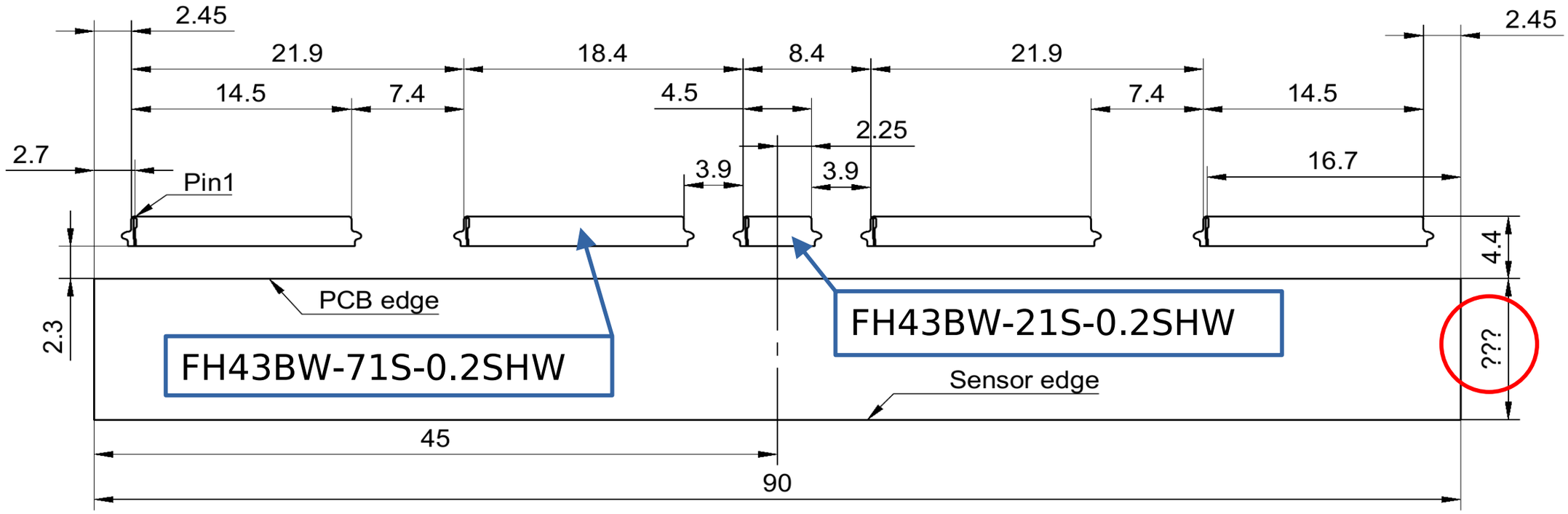
Huge gap between FEBs as I assumed zero gap between sensors



1mm gap between sensors – how large will it really be?

FEB design – fanout connectors

FanoutEdge_Drawing.pdf ← *PDF with the drawing uploaded to Indico*



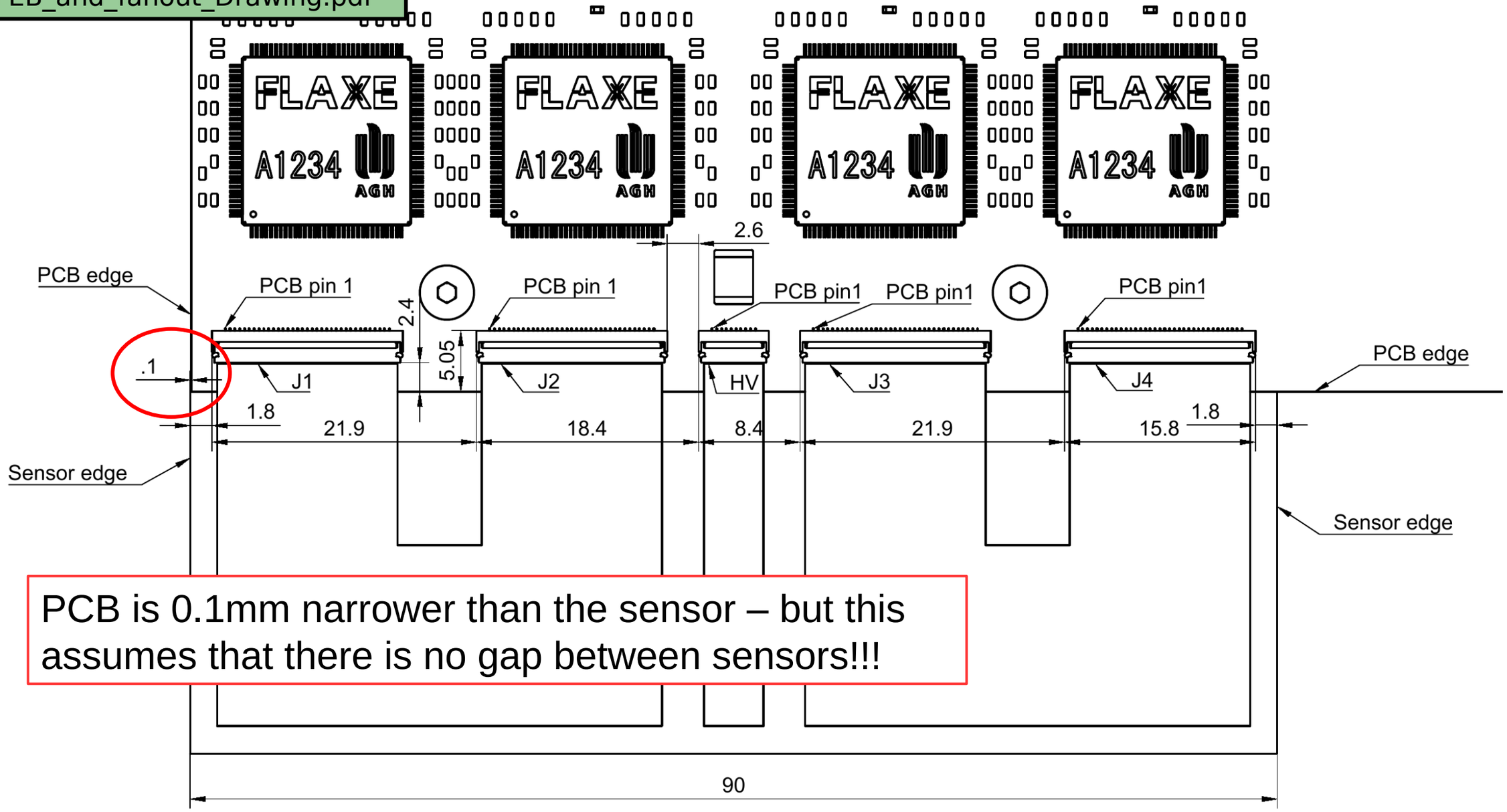
Fanout length should match the distance between sensor edge and the FEB connector position with some, but not so large, slack (0.5mm???)

For HV a 21-pin (slightly overkill) version of the fanout connector proposed:

- The same flex plug design as for main fanout
- Some pins on the edges can be left unconnected to increase the HV clearance to the ground

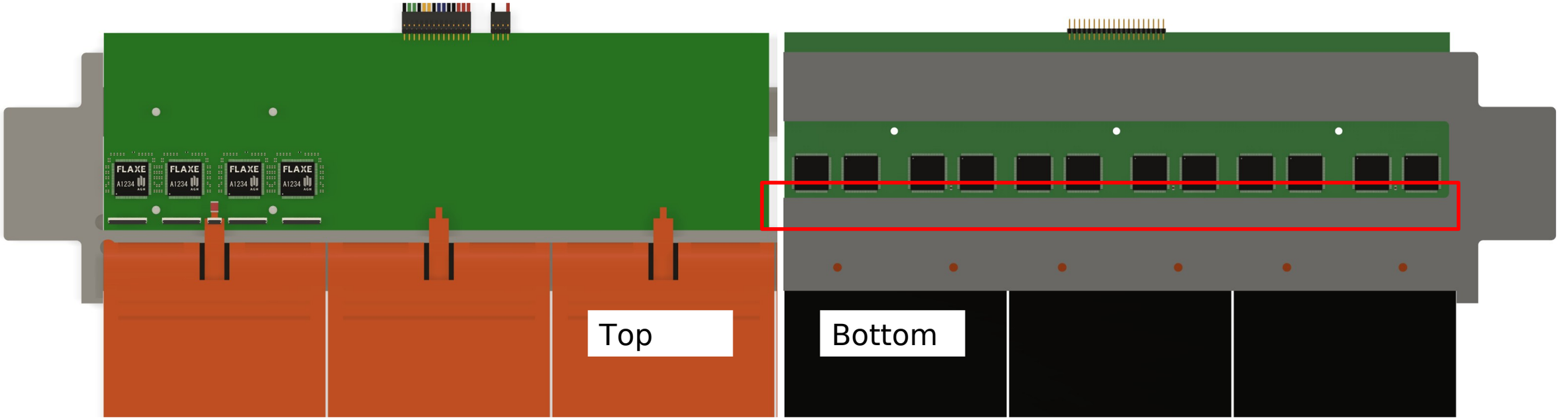
FEB design – fanout connectors

FEB_and_fanout_Drawing.pdf

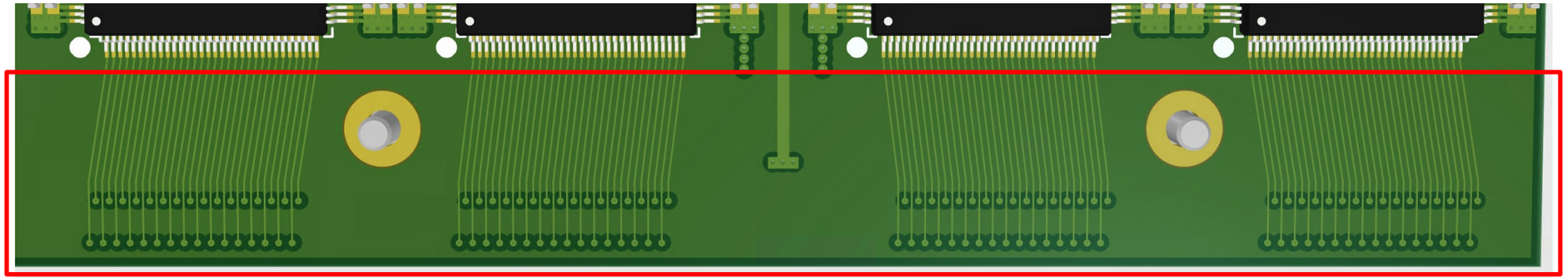


PCB is 0.1mm narrower than the sensor – but this assumes that there is no gap between sensors!!!

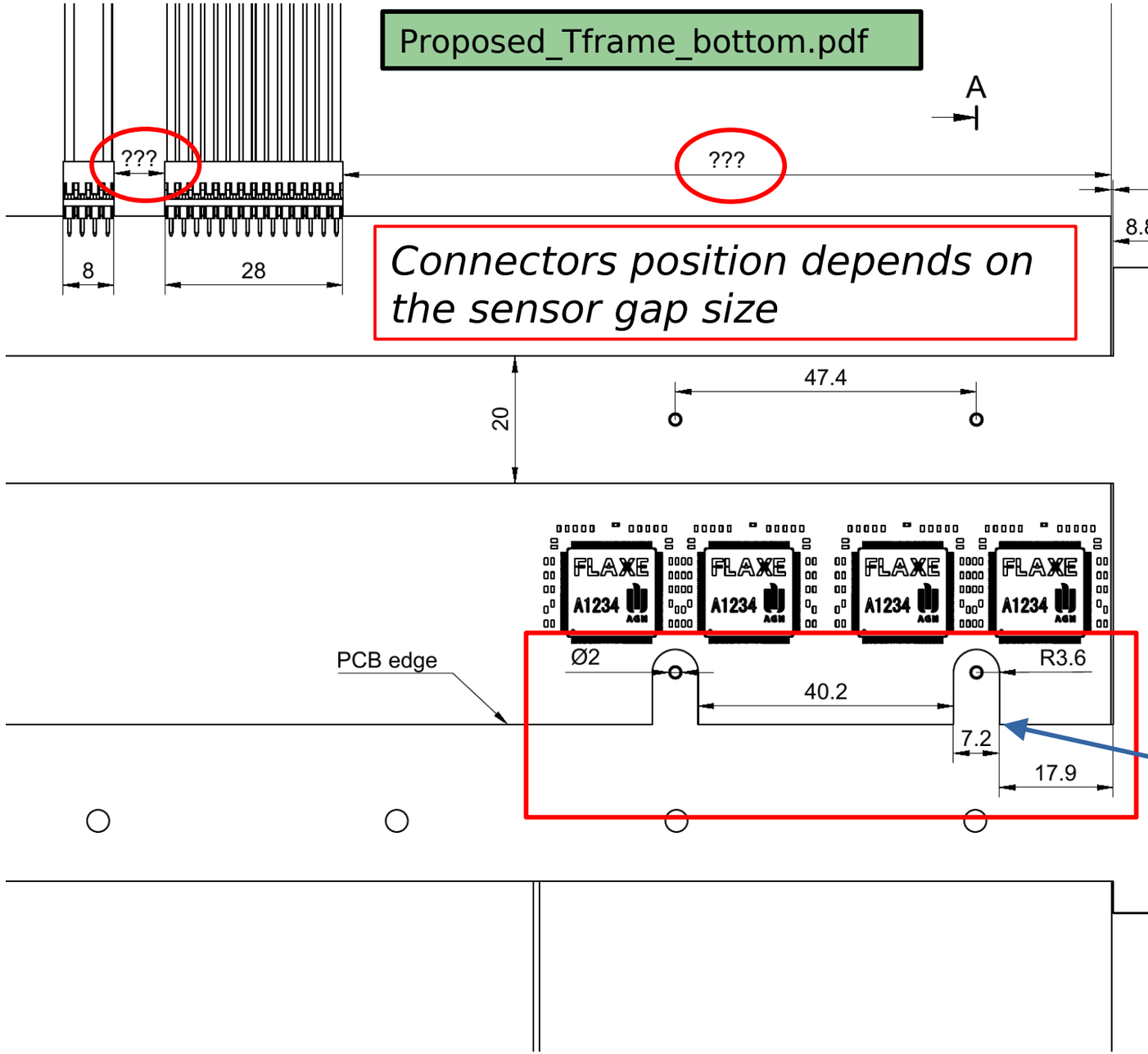
FEB design – “Tframe” design



- A part of the Tframe goes beneath the FEB, touching the PCB bottom layer
- Half of the fanout routing between connector and ASICs goes on bottom layer
- Covering the fanout signals with conductive plate will significantly (~10%) increase total sensor capacitance, moreover only for half of the channels



FEB design – proposed “Tframe” design

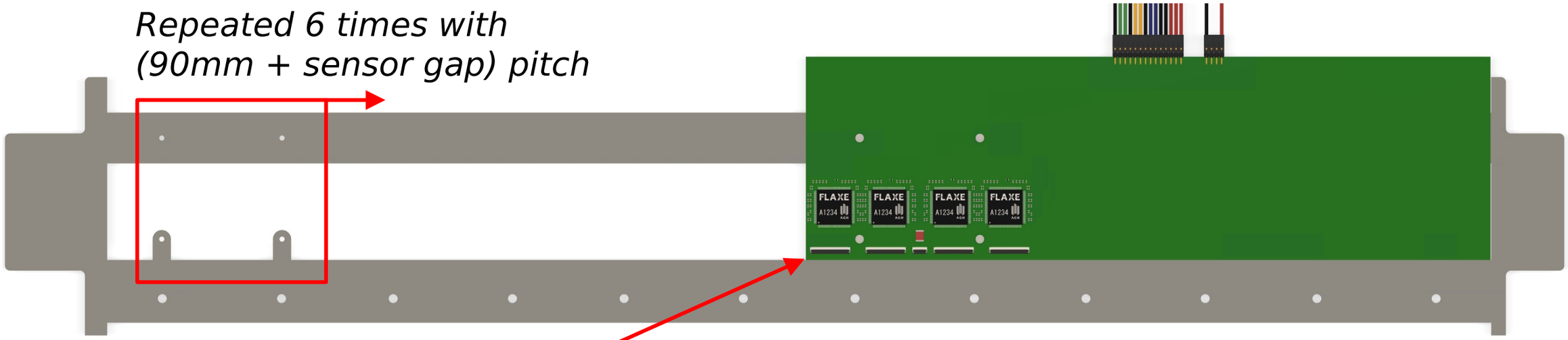


I propose to design a tabs (protrusions) going beneath the FEB PCB in regions without routing

- M2x3mm screws (Bossard 1726536) used to fix FEB to the Tframe
- Maximal possible tab dimensions are presented in the drawing
- 90^{o} corner currently in the design – what is really possible? *Last minute comment from Piotr: 2mm radius possible, fine for FEB PCB*

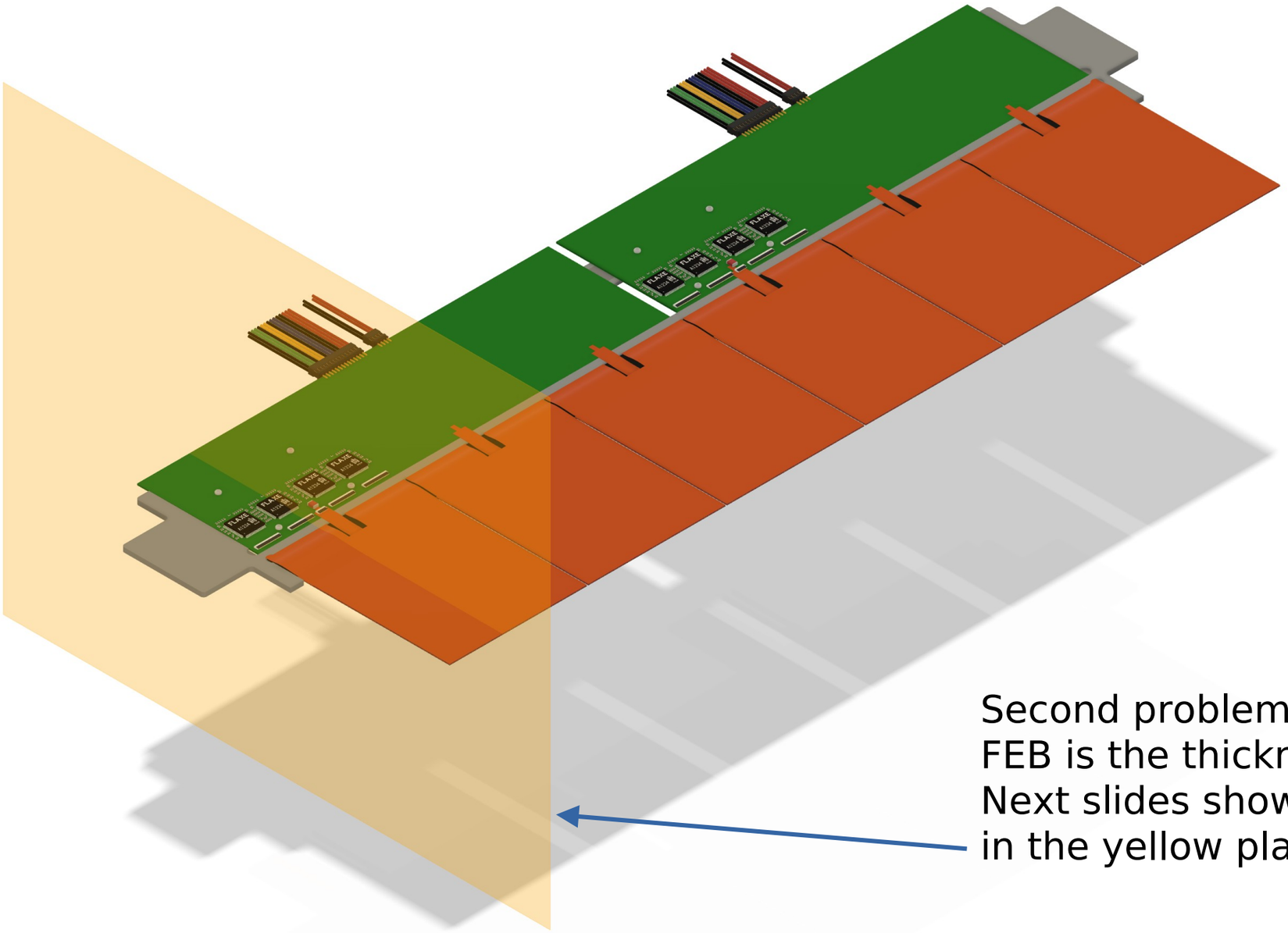
FEB design – “Tframe” design

Repeated 6 times with
(90mm + sensor gap) pitch



- Should the lower edge of the FEB PCB touch the Tframe, or there should be a gap?
- Do you think four M2 screws per sensor (12 screws per FEB) are enough to fix the PCB to the Tframe?

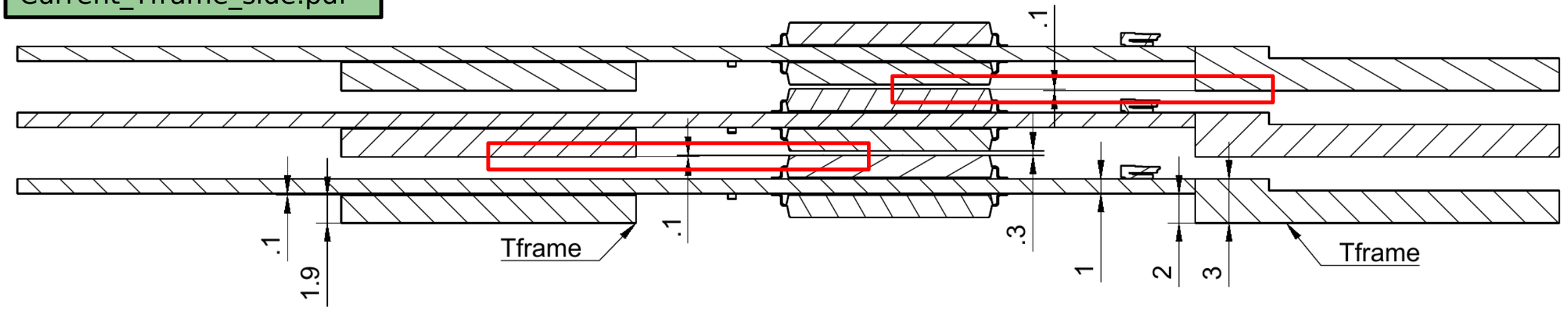
FEB design – “Tframe” design



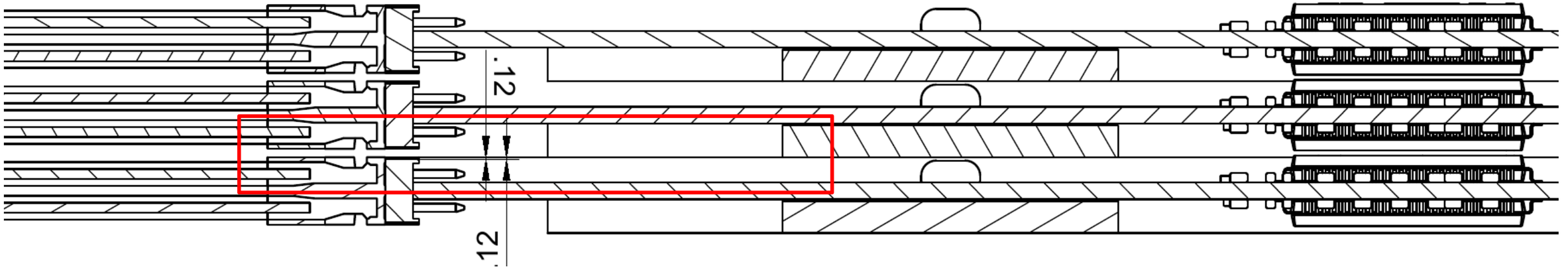
Second problem with Tframe and FEB is the thickness.
Next slides shows the cross-section in the yellow plane.

FEB design – “Tframe” design

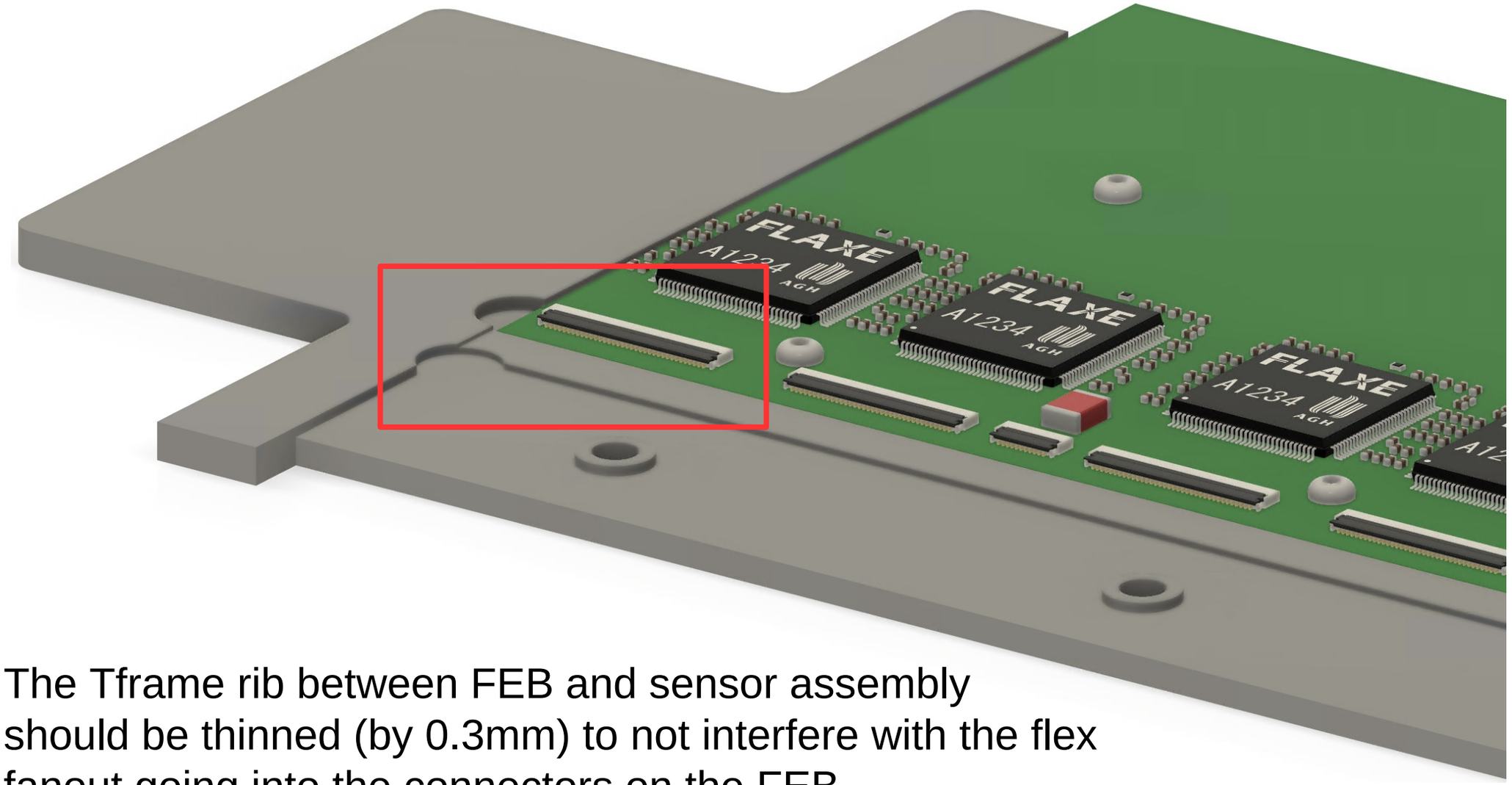
Current_Tframe_side.pdf



- With the top of the FEB PCB aligned with top of the Tframe, there are collisions:
  - between Tframe and an ASICs on the next layer
  - between Tframe and the backend connector



FEB design – “Tframe” design



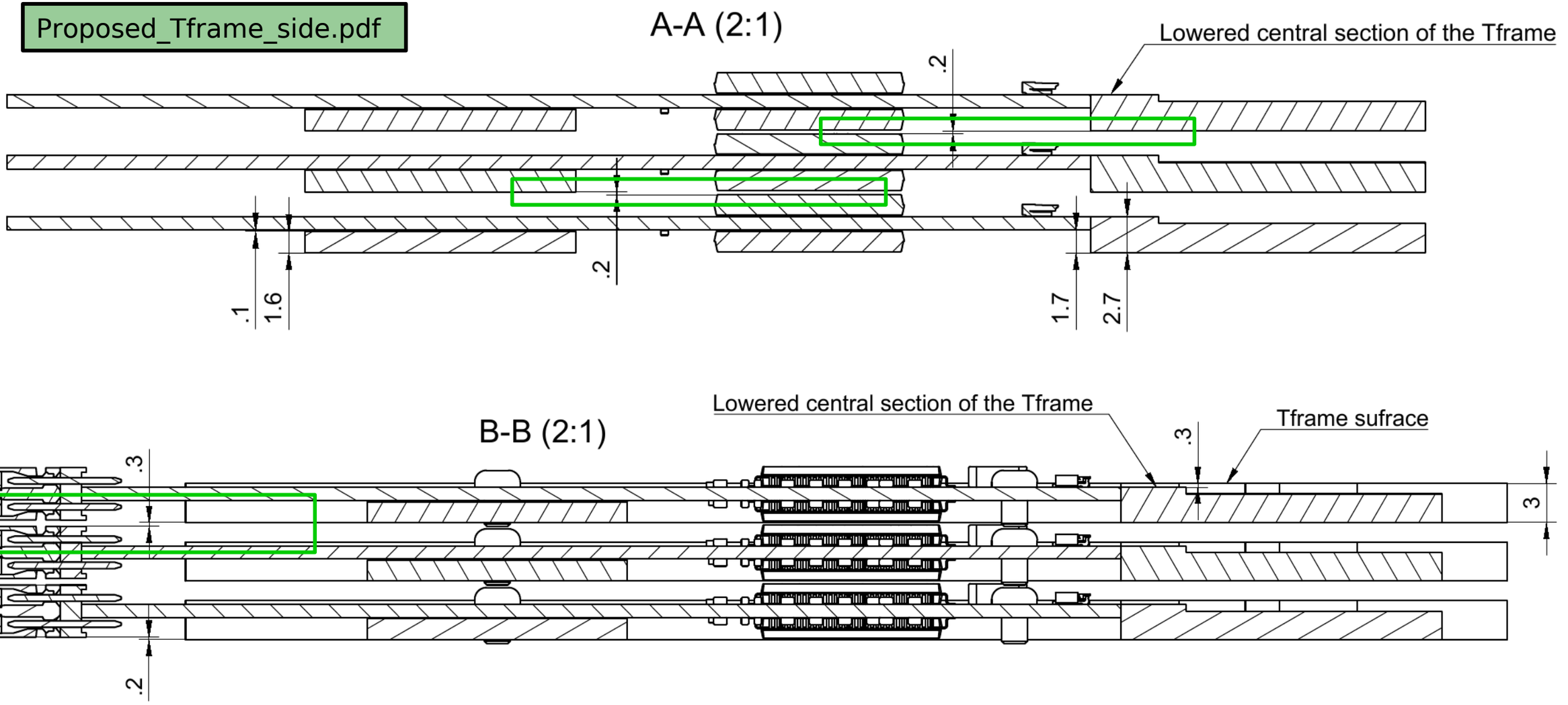
The Tframe rib between FEB and sensor assembly should be thinned (by 0.3mm) to not interfere with the flex fanout going into the connectors on the FEB

Is it possible to make this section thinner? (or see the second option on the next slides...)

FEB design – “Tframe” design

We propose to put the PCB 0.3mm lower (top surface of the PCB 0.3mm below Tframe top surface). This resolves all the collisions

Proposed_Tframe_side.pdf



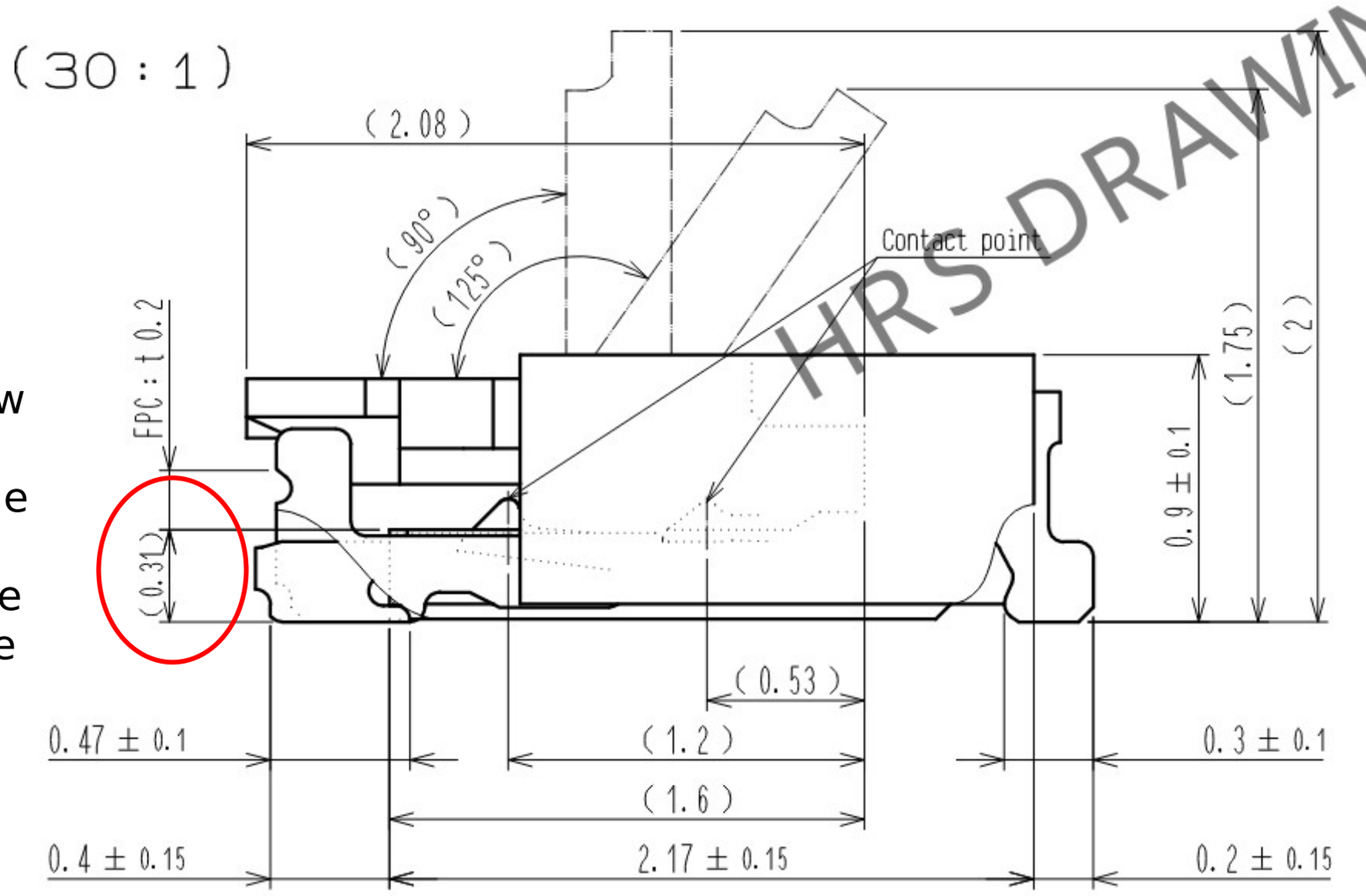
FEB design – “Tframe” design

FH43BW-71S-0.2SHW(10) drawing:
https://www.hirose.com/product/p/CL0580-2819-5-10#documentSection

The bottom surface of the FPC (fanout flex plug) is **0.31mm** above top PCB surface.

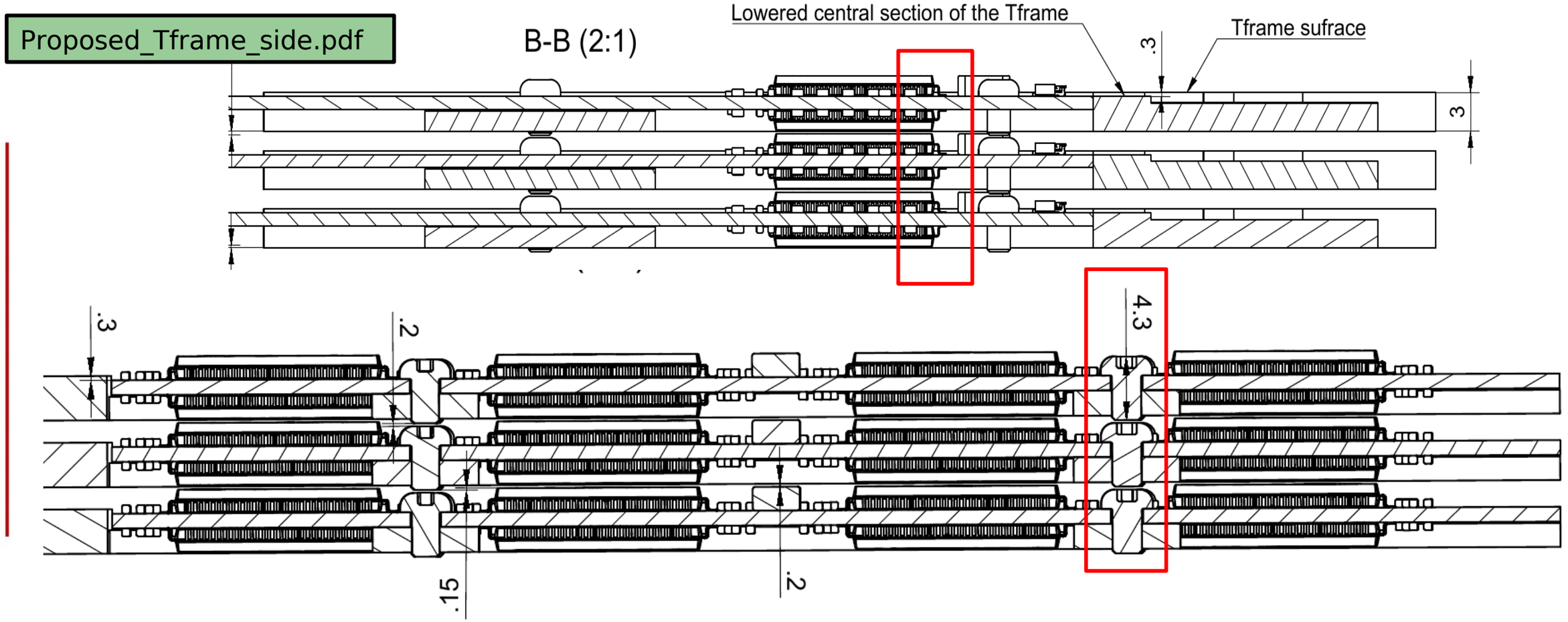
With PCB sunk 0.3mm below top surface of the Tframe, there is no need to lower the central section of the Tframe, but in such case the fanout will touch the Tframe
What will happen with:

- Capacitance?
- Electrical isolation?



FEB design – “Tframe” design

Proposed_Tframe_side.pdf



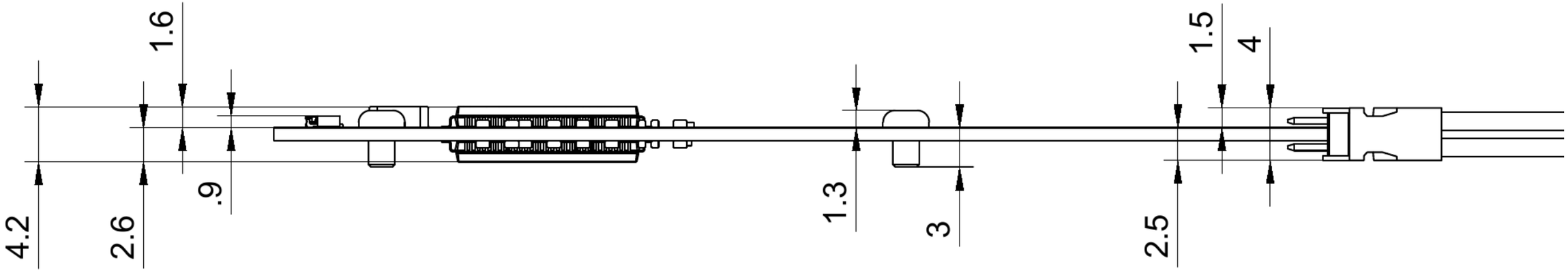
The total length of the M2x3 screw is 4.3mm – 0.2mm space to next layer (**is it enough?**)

Screws do not collide with ASICs as they are placed between them.

Backplane connector also have to be placed between the screws

FEB design – “Tframe” design

ECAL_FEB_Drawing.pdf



The overall thickness of the FEB is **4.2 (+0.1) mm**, determined by the thickness of the PCB and the FLAXE ASIC package**:**

- 1.6 (+0.05) mm up from PCB top surface
- 2.6 (+0.05) mm down from PCB top surface

This gives 0.3 (-0.1) mm gap between the ASICs.

The FEB PCB should be placed in the Tframe in a way that all Tframe elements are within “shadow” of the FLAXE ASICs (4.2 mm)

Summary – questions and topics to discuss

1) What will be the distance between neighboring sensors on the layer?

2) What will be the HV granularity: one supply channel per FEB or one per sensor?

3) What HV can we expect after sensor irradiation?
   Current FEB design assumes HV < 1kV. Is it enough (including safety margin)?

4) Fanout flex length – how much slack we want?

5) Tframe design:
   a) Is the design with tabs / protrusions feasible?
   b) ~~What is minimal radius in the bottom part of the tab?~~
      Resolved: 2mm possible, fine from PCB design point of view
   c) What should be the FEB PCB to Tframe distance (especially bottom edge)?
   d) FEB PCB 0.3mm below the top surface of the Tframe – is it possible?
   e) Can the part of the Tframe in front of the PCB be made thinner?
      Or can the fanout touch this part of the Tframe?
   f) Are the proposed M2 screws acceptable (mainly the 0.2mm distance to next layer)?

6) We need common design repositories server – DESY GitLab is ok?
   a) Can we have the mechanical design (e.g. step files) in DESY GitLab?

7) We need dose and neutron flux estimation for area above sensors in ECAL-p!

Summary – DESY GitLab

1) Login to **gitlab.desy.de** using DESY account or through Helmholtz AAI

2) Ask me or Shan for access to the **LUXE ECAL** group

3) Please keep the order by putting your repositories into proper subgroups

   a) **The <u>ECALp DAQ</u> subgroup is intended for the new design for ECAL-p**

      Please do not put there anything related to the FLAME (testbeam) DAQ

4) I will transfer the whole FLAME DAQ from Github to DESY GitLab into the **FireDAQ** subgroup