

DAK

DAPHNE FRONT
END
BOARD

PPD EED 176998

8 February 2021

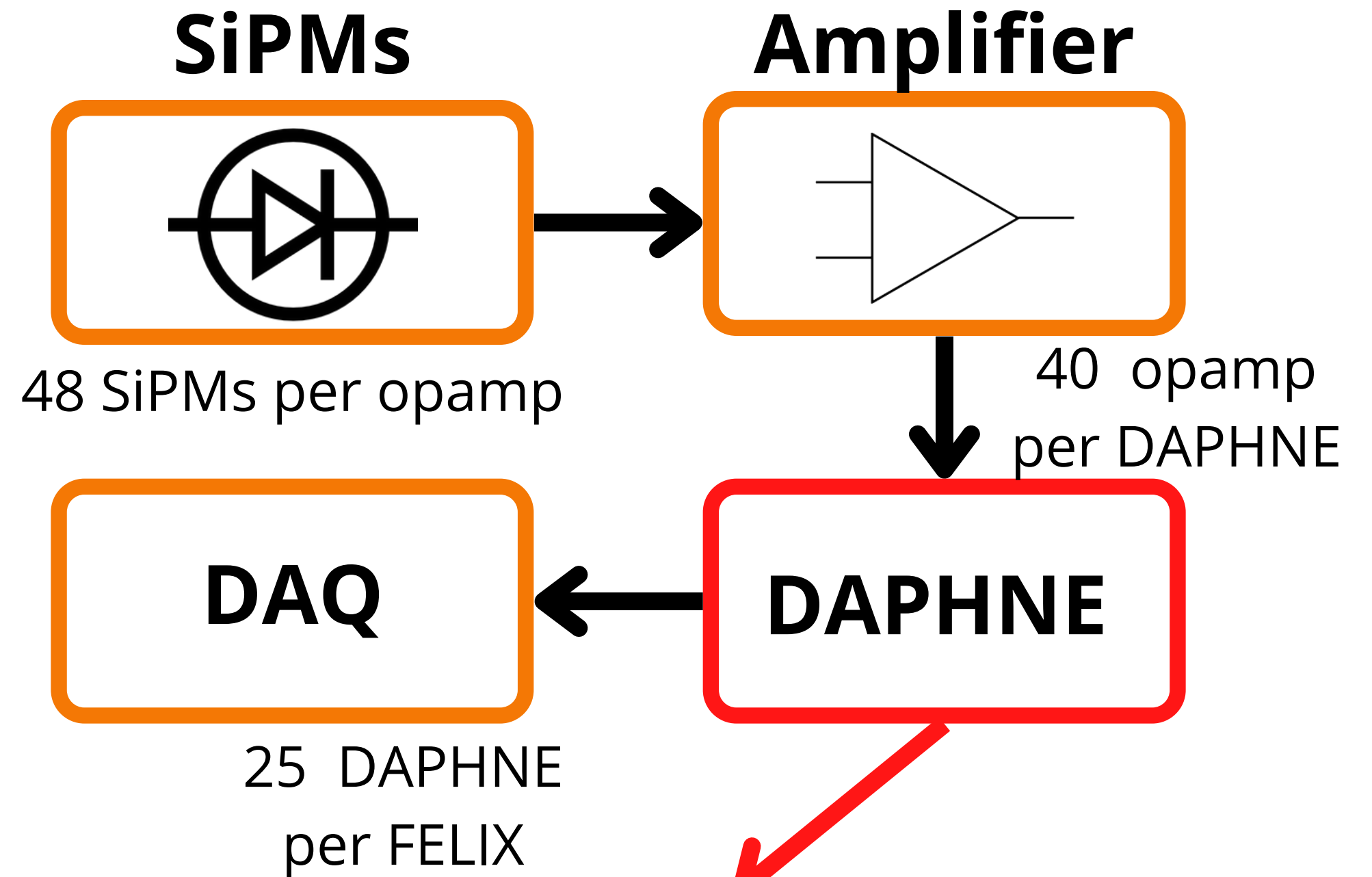
CARLOS BENITEZ MONTIEL

IFIC

DAPHNE

"In simple terms, DAPHNE is a cheap oscilloscope with quite expensive firmware"

Manuel Arroyabe



Hardware Specifications



AFE

The digitization stage is driven by 5 AFEs 5808A by Texas instruments performing a 62.5MSPS, with 8 analog channels at 14 bit resolution each one



FPGA

The FPGA device implemented on DAPHNE is Xilinx Artix-7, model XC7A200T-676.



Micro

Device:
STM32H753
Cortex-M7

Obs:

DAPHNE Provide the Vbias for the SiPMs

UAN

UNIVERSIDAD
ANTIOQUEÑA
Moreno

UNIVERSIDAD

EIA

Ser. Safety Servir

M. Arroyave, E. Rincón



Fermilab

M. Marchán, N. Moiseenko, G. Drake, S. Hansen
T. Shaw, M. Toups, J. Olsen

0005
13813



AGENCIA ESPACIAL
DEL PERU

J. Vega



UNIVERSIDAD
DE ANTIOQUIA

F. Castano



C. Montiel, D. Aranda, E. Cristaldo

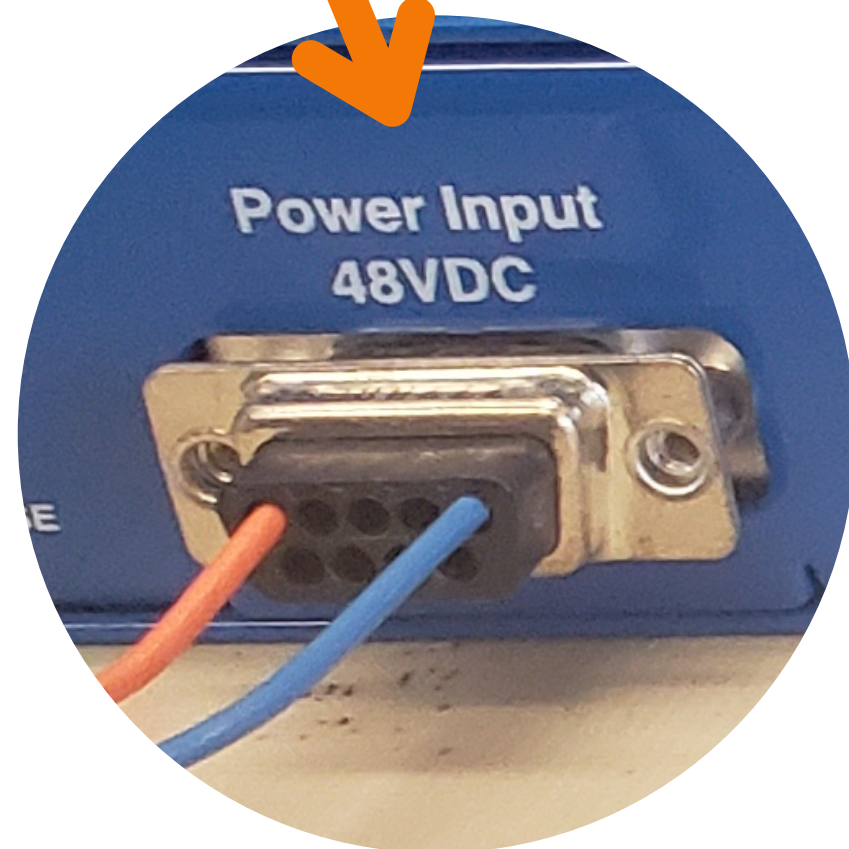
DUNE
DAPHNE FRONT
END BOARD

PPD EED-176998
8 February 2021

Pulse
OH164NL
2017-YC CHINA

Pulse
OH164NL
2017-YC CHINA

DAPHNE Control



DAPHNE GROUPS



Electrical Electronics

Fermilab - USA
UAN - Colombia
NIU - USA



Micro

UAN - Colombia
Fermilab - USA



Firmware

EIA - Colombia
Fermilab - USA
FIUNA/IFIC - Py/Es

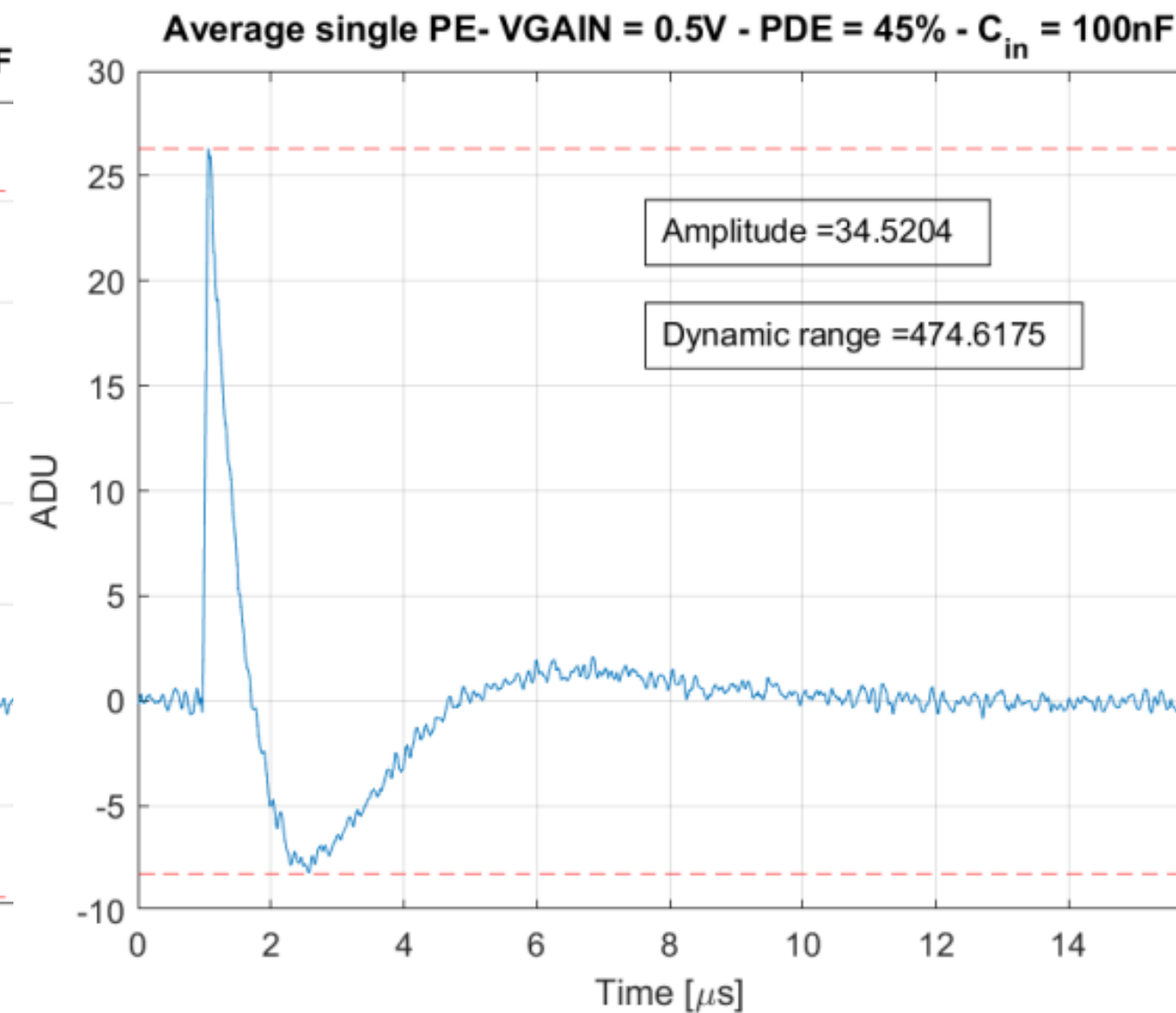
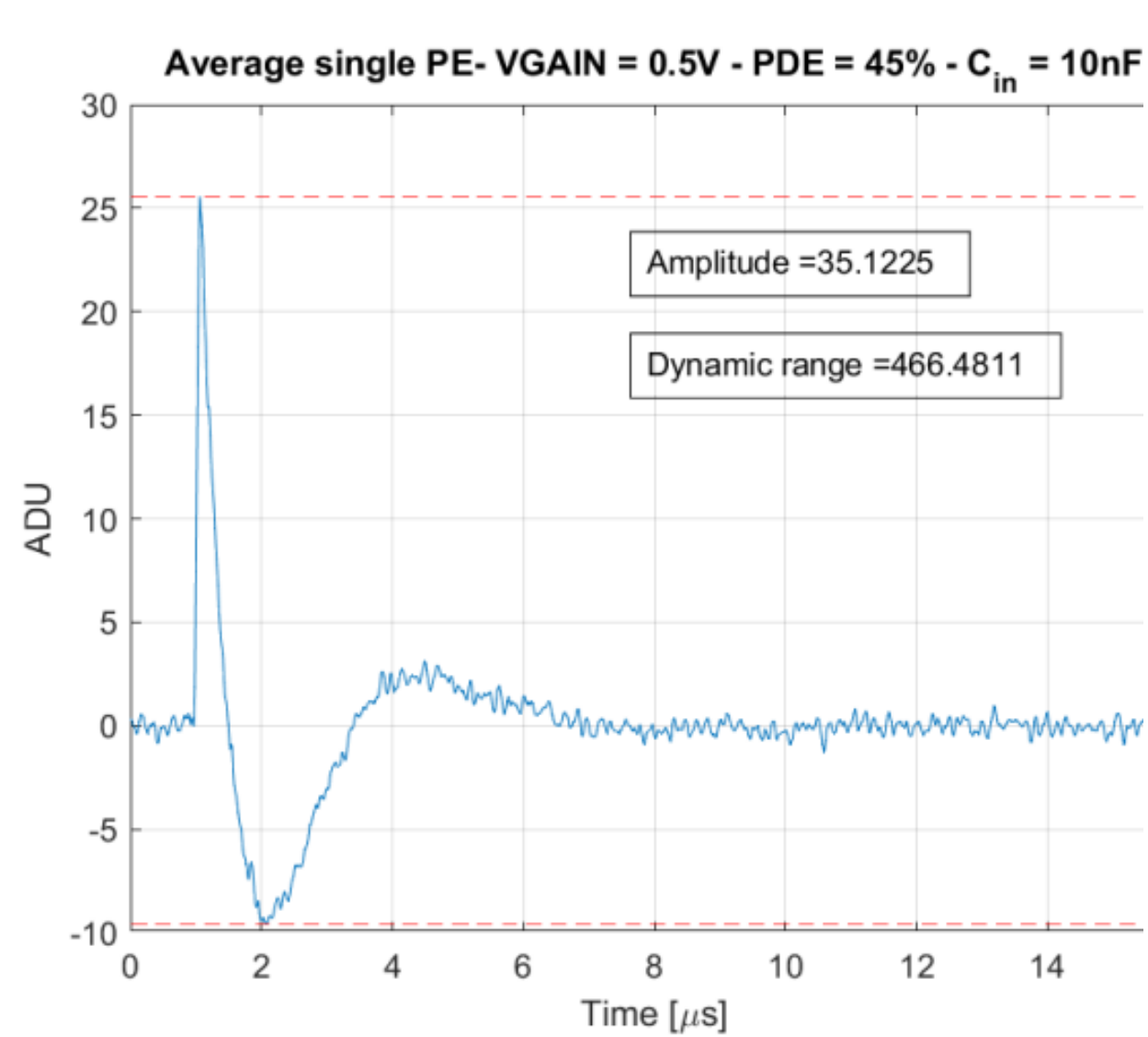
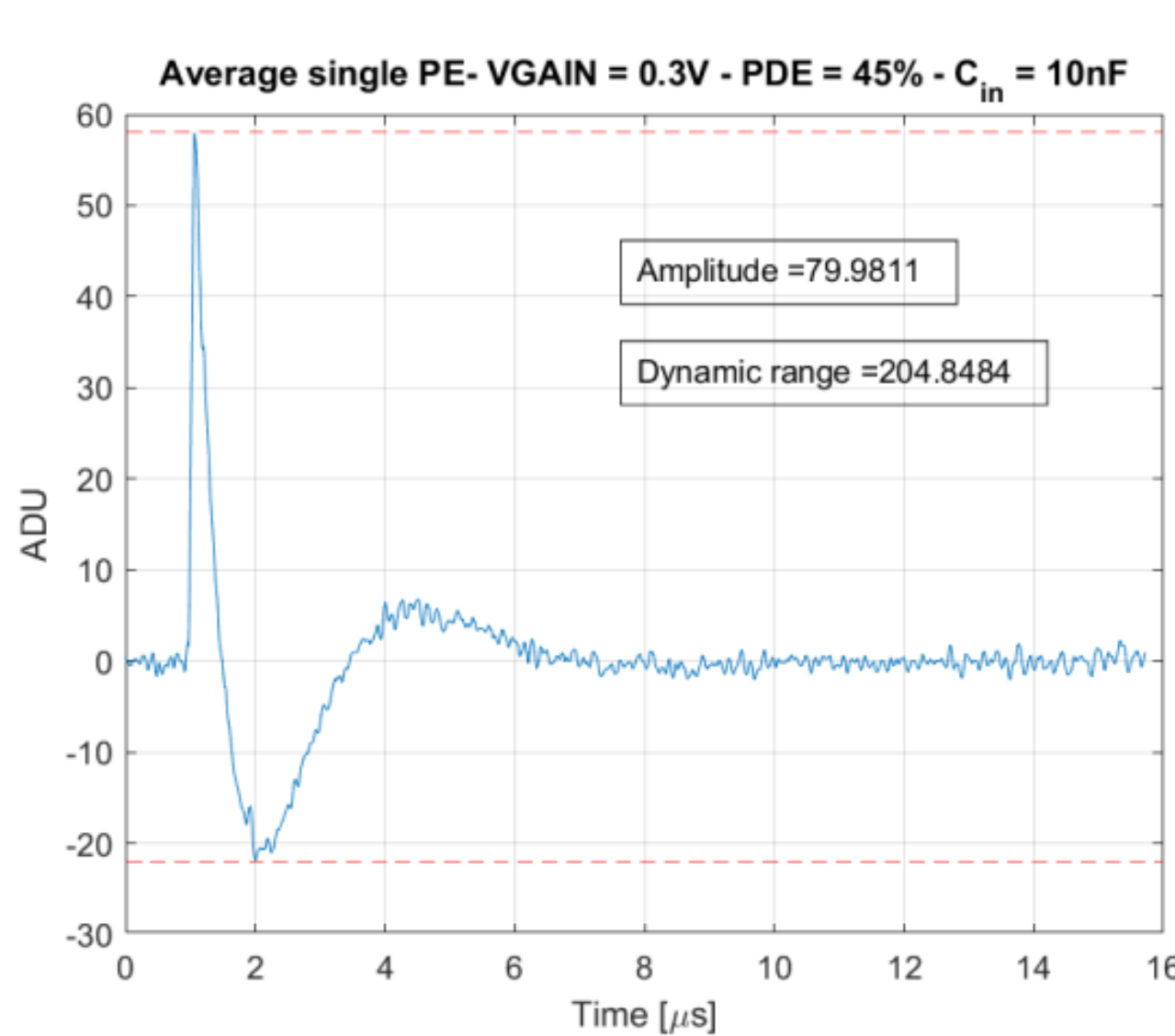


DAQ integration

FIUNA/IFIC - Py/Es
UPENN - USA

Results

From the Amplification group after some modifications on the board

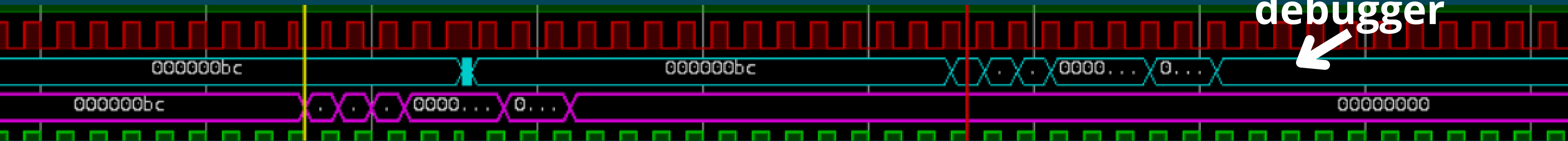


Results From the DAQ firmware group

This is my work!!! =)

DAPHNE Transceiver

debugger



```
(dbt-pyvenv) [nikolica@dhcp-29 dune-daq-felix]$ fdaq -d 0 -t 10
Consume FLX-device data while checking the data (blockheader and trailers),
counts errors including chunk truncation, halts when the memory buffer is near overflowing.
Also counts chunk CRC errors.
```

```
Opened FLX-device 0, firmw FLX712-FM-6chan-1910282359-GIT:dune/v1./2, trailer=32bit block=4K, buffer=1024MB
```

```
**START** using DMA #0 polling
```

Secs	Recvd[MB/s]	File[MB/s]	Total[(M)B]	Rec[(M)B]	Buf[%]	Wraps
1	186.4	0.0	186.4	0	0	0
2	186.3	0.0	372.8	0	0	0
3	186.3	0.0	559.0	0	0	0
4	186.4	0.0	745.4	0	0	0
5	186.4	0.0	931.9	0	0	0
6	186.2	0.0	1118.1	0	0	1
7	186.5	0.0	1304.6	0	0	1
8	186.2	0.0	1490.8	0	0	1
9	186.4	0.0	1677.3	0	0	1
10	186.4	0.0	1863.7	0	0	1

```
**STOP**
```

```
-> Data checked: Blocks 454186, Errors: header=0 trailer=0
```

```
Exiting
```

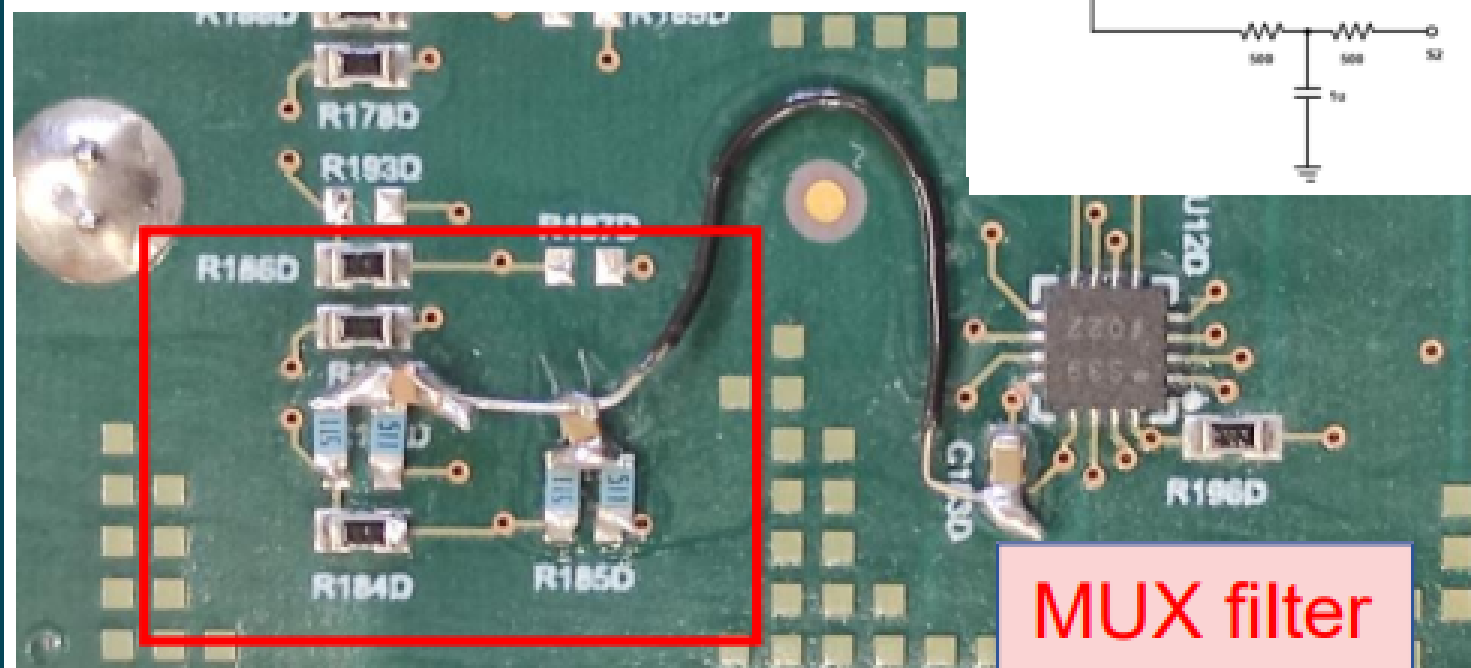
FELIX Receiver
system

Future Works

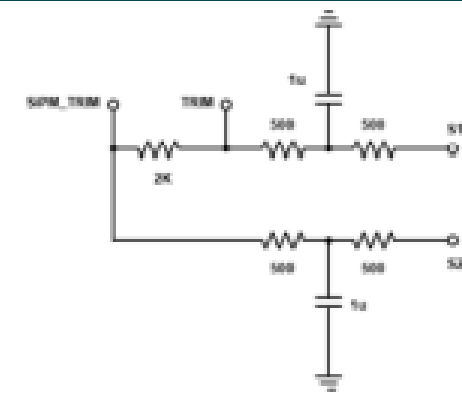
Electrical - Electronics parts

It is necessary to study in more detail the noises introduced by the DAPHNE board. Some of these elements were corrected by Esteban Cristaldo at Milano Bicocca, which will be implemented in the second version of DAPHNE.

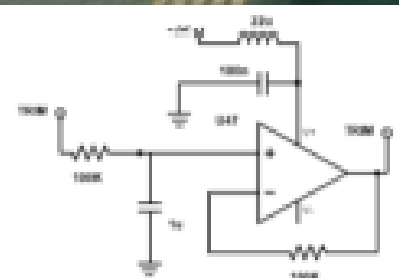
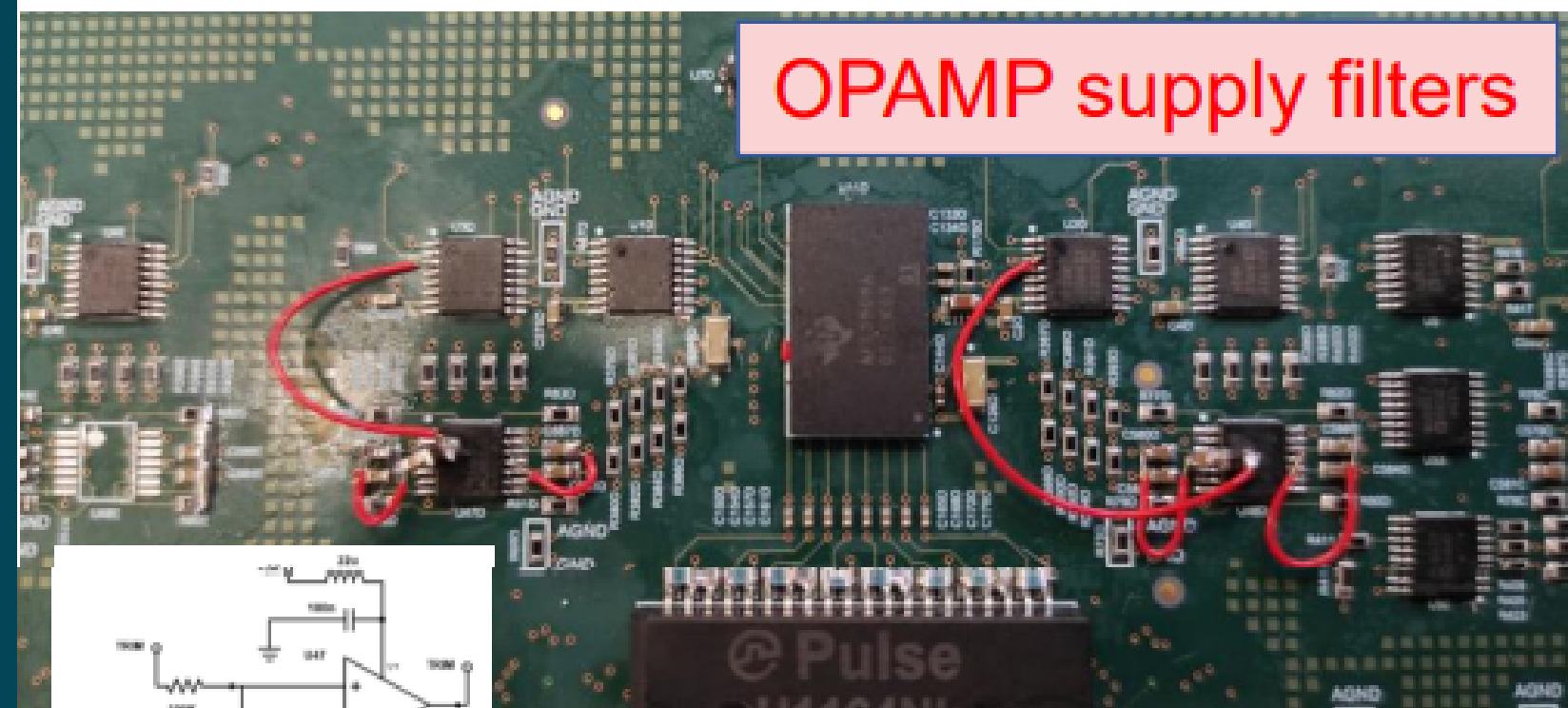
Patch 1



MUX filter



OPAMP supply filters

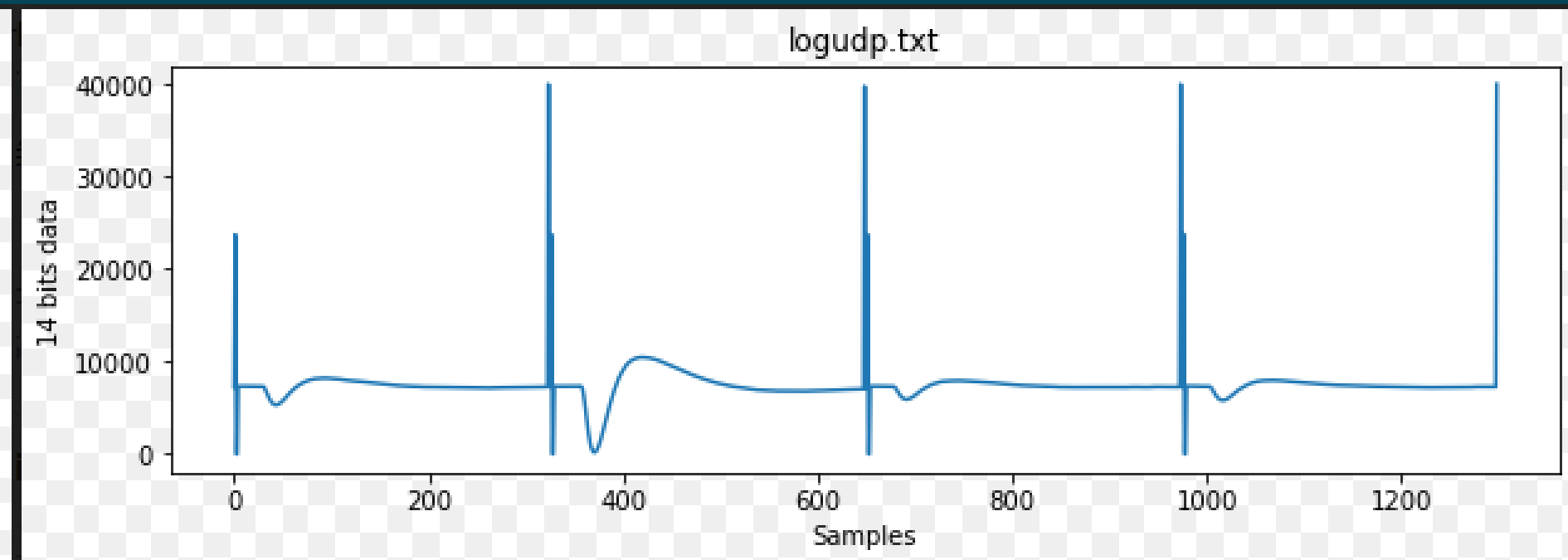
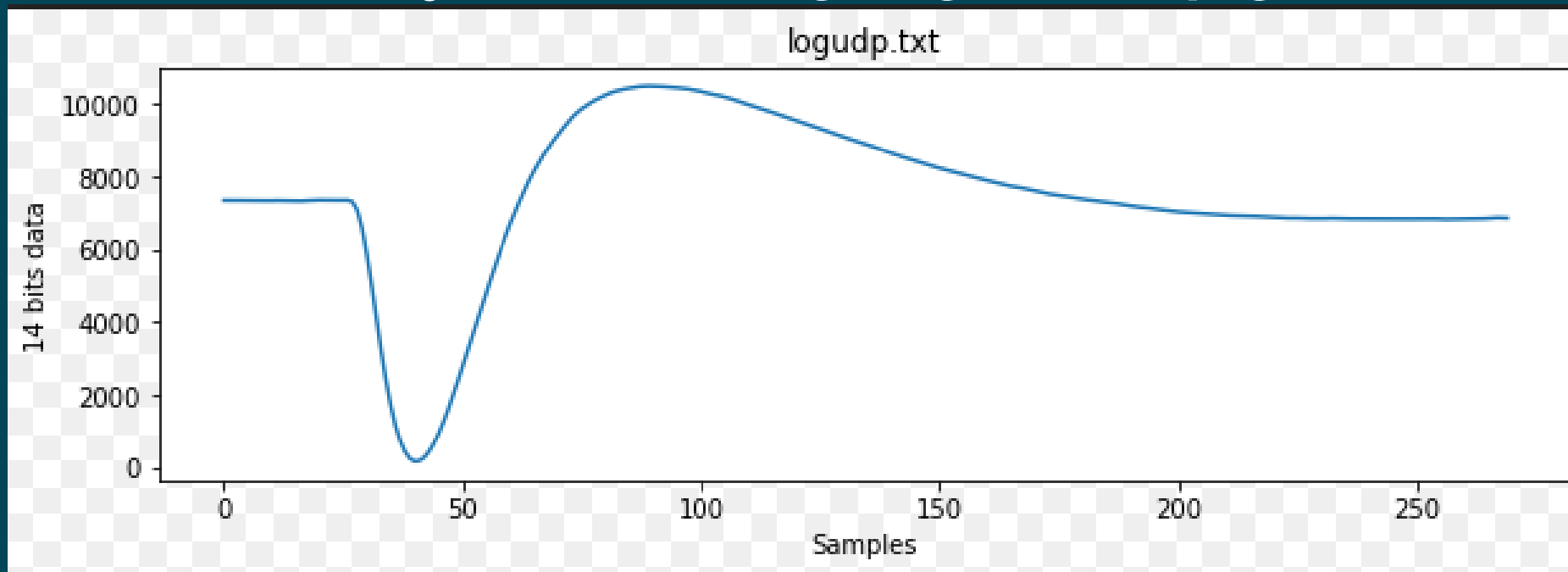


...

Future Works

Firmware

It is necessary to remake the firmware with a unified language, study possibilities of applying digital filters to reduce the $1/f$ noise found by Esteban, study self-trigger options or models adapted for external triggers, rethink the data packaging structure. Study the way to increase the bandwidth by activating the gtp quads that are off, study the feasibility of changing the fpga, etc etc



Future Works

Micro

change the micro for one that adapts to the DAQ requirement and study the compatibility of the libraries made by the institutions.

Possible work at IFIC

All about FPGA

- Study the Digital Filters options and implementation
- Remake a complete Firmware for DAPHNE
- Study different methods of self-trigger
- Study the timing performance of the FPGA for the best work

Esteban (Milano - Bicocca) is willing to work together in terms of Cold Electronic - DAPHNE integration, where we prepare the firmware options for them to test with the amplification systems and study them until the best results are obtained.