Forward Tracker Disks for the DBD

IX Jornadas Futuros Aceleradores
IFIC, Valencia

I. Vila
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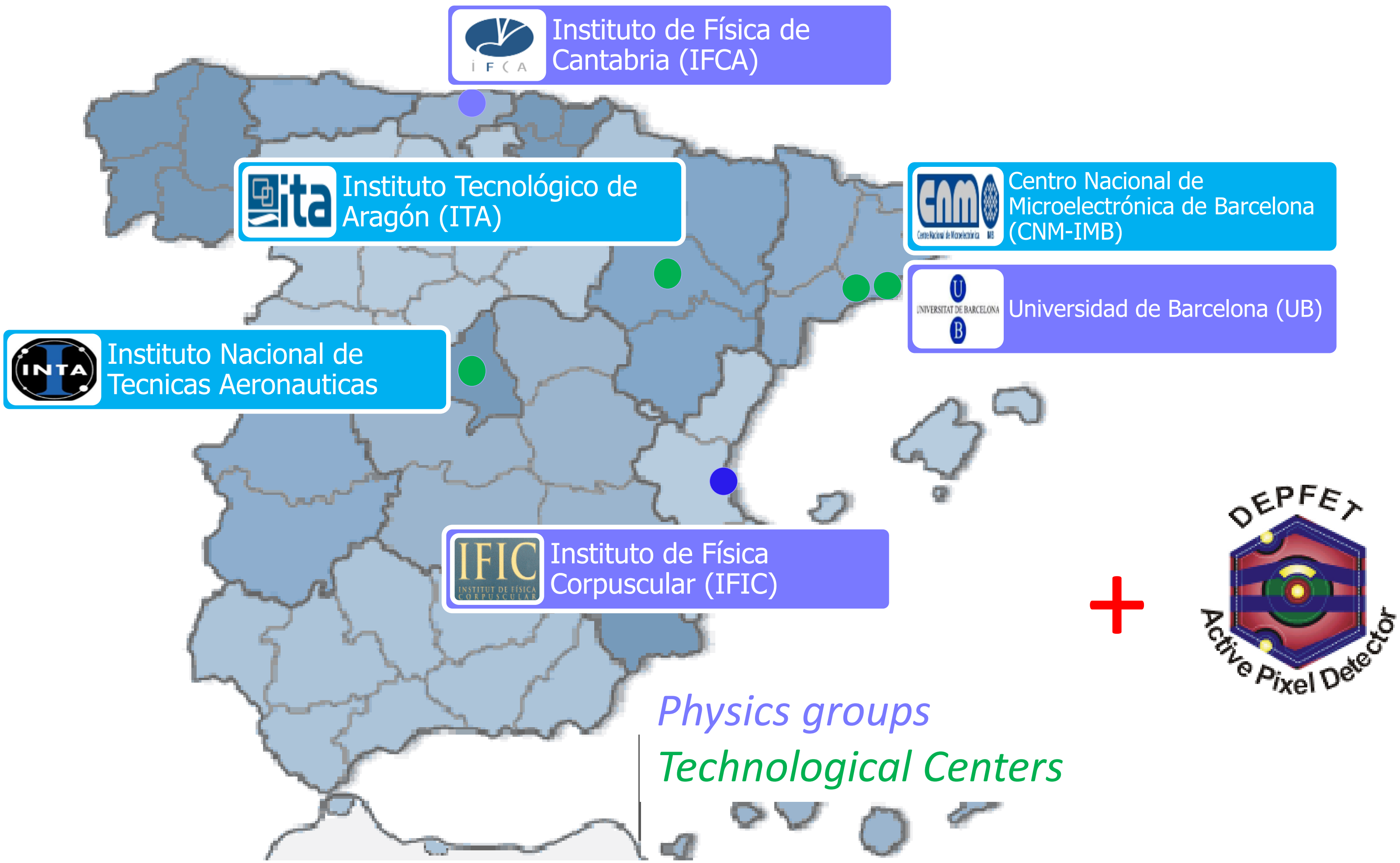
Thanks to F. Arteche (ITA), A. Dieguez (UB), M. Frovel (INTA), D. Moya (IFCA) & M. Vos (IFIC) for their supporting material

FTD community at a Glance

Part of Spanish Network on Future accelerators

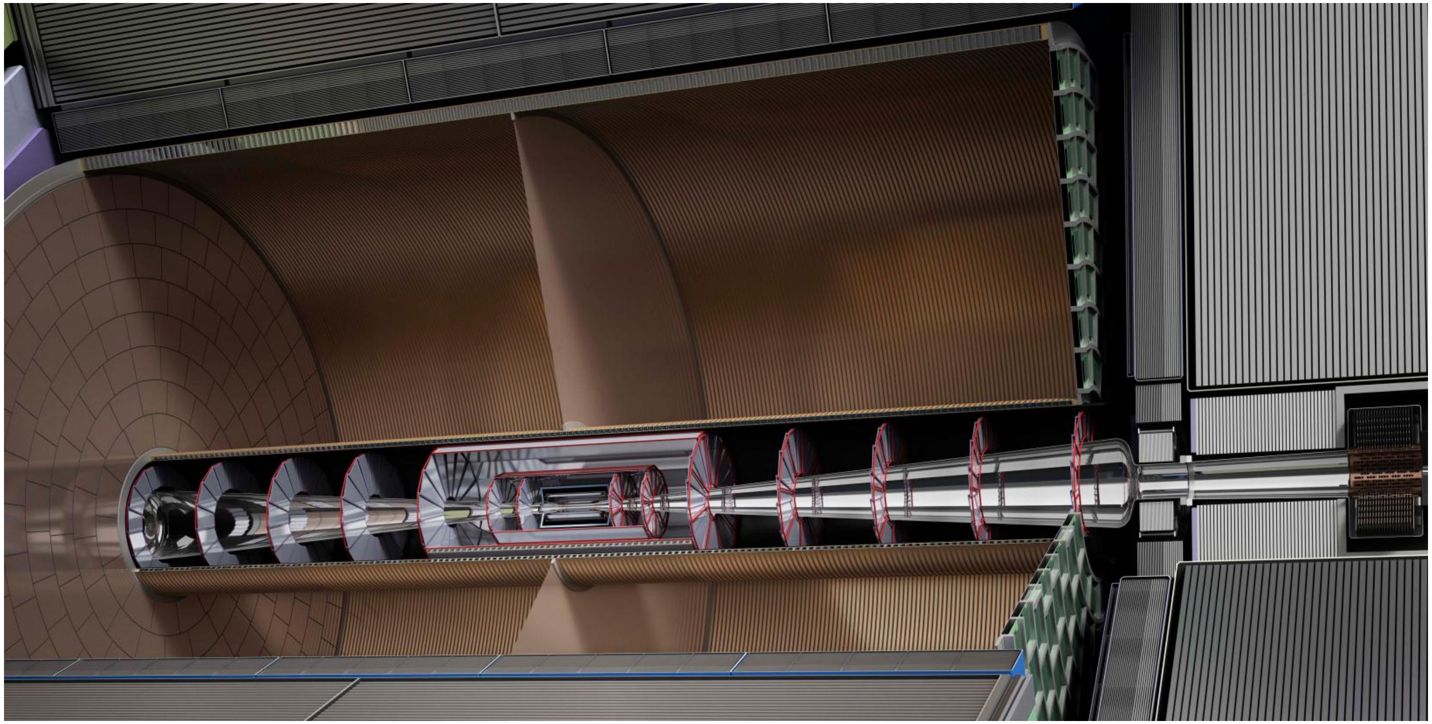


Outline

- FTD baseline design (DBD implementation) :
  - Pixelated disks: DEPFET & CPS
  - Strip Petal design: sensors and hybrids.
  - Mechanics, integration & services
  - Front-end electronics.
  - Power distribution & EMC.
  - Alignment and monitoring.
- Beyond the baseline design (R&D activities).
  - 2D strips sensors, miniaturized position sensors and low noise powering.

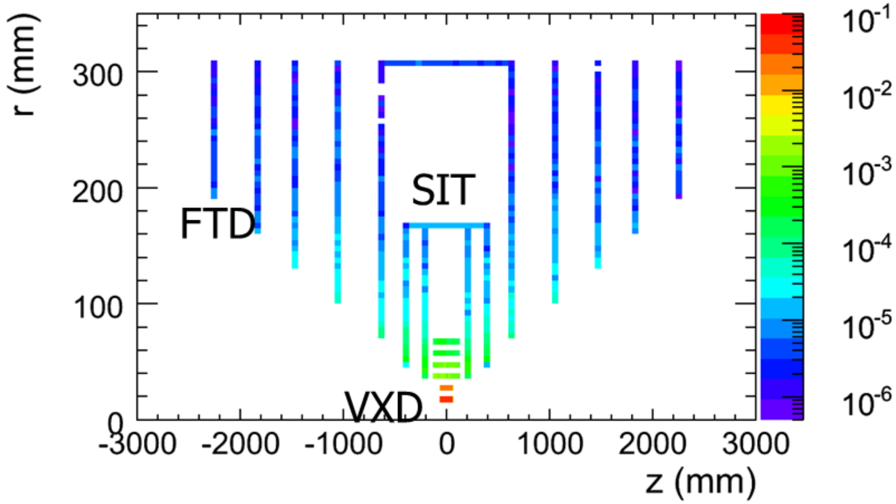
Introduction: baseline design

- Seven layers (disk) covering the forward and backward region between the TPC and the beam pipe.
- Inner two disks (inside thermal enclosure ?) pixelated single layer of silicon sensors and five outer disks equipped with a double layer of strip-based silicon sensors.



Layout optimization: why pixels ?

Pair background



GEANT4 simulation of GUINEA-PIG events by Toni Harlin
(thanks also to A. Vogel and Katarzyna Wichman)

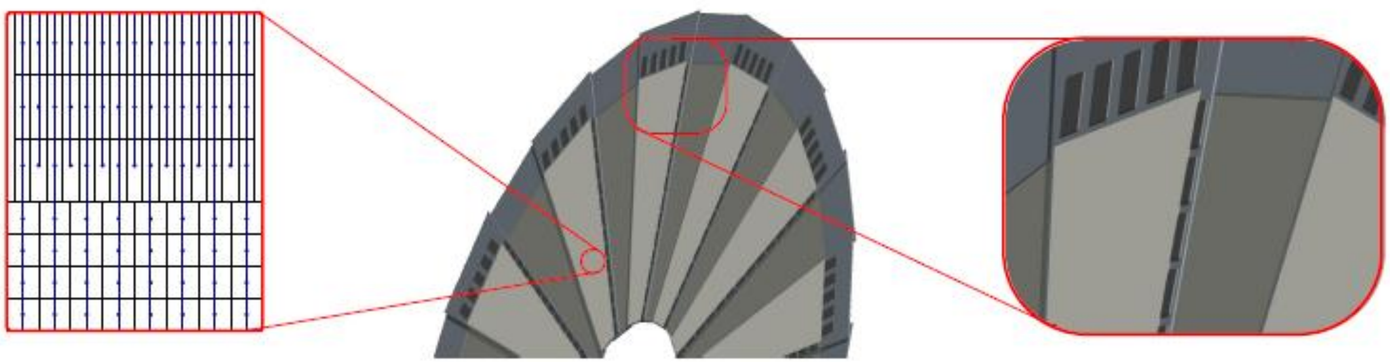
Hit density
($\#/mm^2/BX$)

detector	min	typical	max
VXD 1		$4x10^{-2}$	
VXD 6		$3x10^{-4}$	
FTD1	$<10^{-5}$	$1x10^{-4}$	$2x10^{-3}$
FTD7	$5x10^{-6}$	$7x10^{-6}$	$9x10^{-6}$
SIT 1		$3x10^{-5}$	
SIT 2		$3x10^{-6}$	

Hit density = number of GEANT4 energy deposits per unit area per ILC bunch crossing
Does not take into account the number of channels fired by a single hit

	Typical area sensitive elements	time resolution:
pixel:	$25 \times 25\ mm^2 = 6.25 \times 10^{-4}\ mm^2$	100 BX
strips:	$50\ mm \times 10\ cm = 0.5\ mm^2$	1 BX

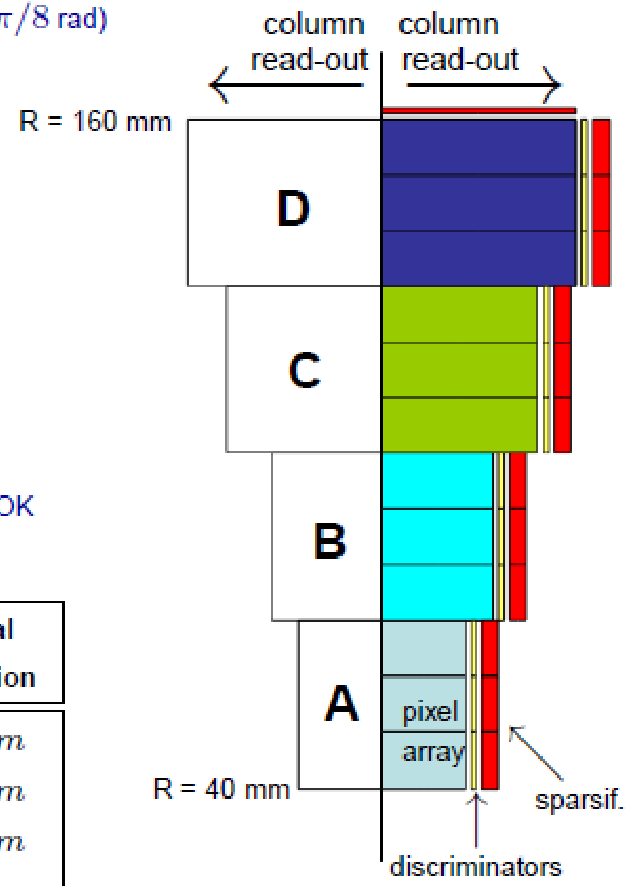
Pixelated disks: DEPFET implementation



- Adaptation of the barrel ladder concept.
- To cope with the strongly increasing background levels towards the smallest R values. Radially three pixel dimensions are used:
  - 25 □um in the innermost region; 50 um for 6 cm < R < 8 cm; 100 □um for R > 8 cm.
- Rphi resolution from 3-5 um depending of the radius

Pixelated disks: CMOS Implementation

- 16 petals made of 4 sensors (50 μm thin) on station front & back ($\Delta_\phi = \pi/8$ rad)
  $\Rrightarrow$ 4 impact positions per track traversing end-cap ($\sim$ 0.5 % X_0/station)
- Sensors' sensitive area: from 30×28 to 30×64 mm^2
- Each sensor combines 2 sub-arrays read out on opposite sides
- Each sub-array composed of 1152 columns of 480 pixels
- Column // read-out via pairs of rows (200 ns/per pair) $\Rrightarrow$ $t_{r.o.} \sim 50\ \mu s$
- Binary charge encoding and integrated data sparsification
- Instantaneous power: 2.4 W/chip $\Rrightarrow$ $\lesssim$ 10 W/petal
  $\Rrightarrow$ $P^{inst.}_{endcap} \sim 600$ W $\Rrightarrow$ $\overline{P}_{endcap} \sim$ O(10) W $\Rrightarrow$ air cooling OK

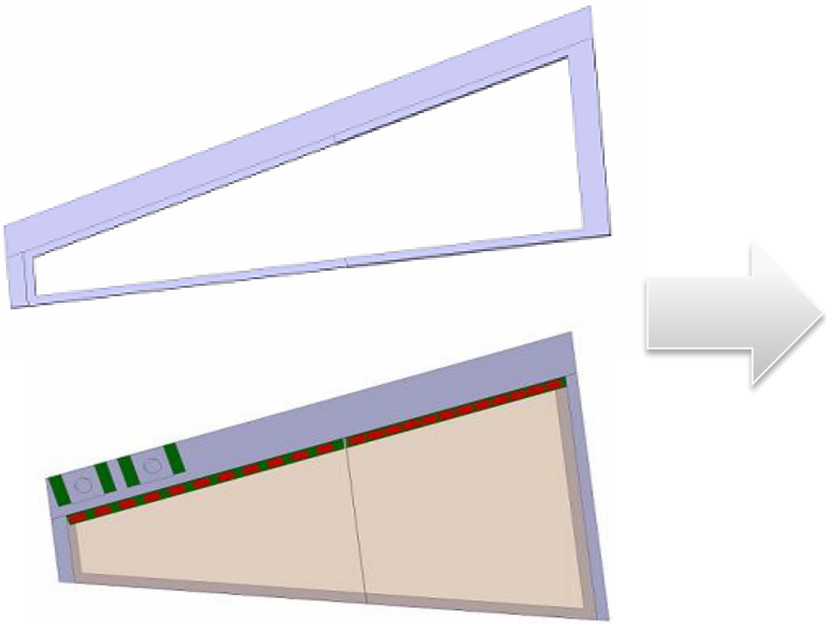


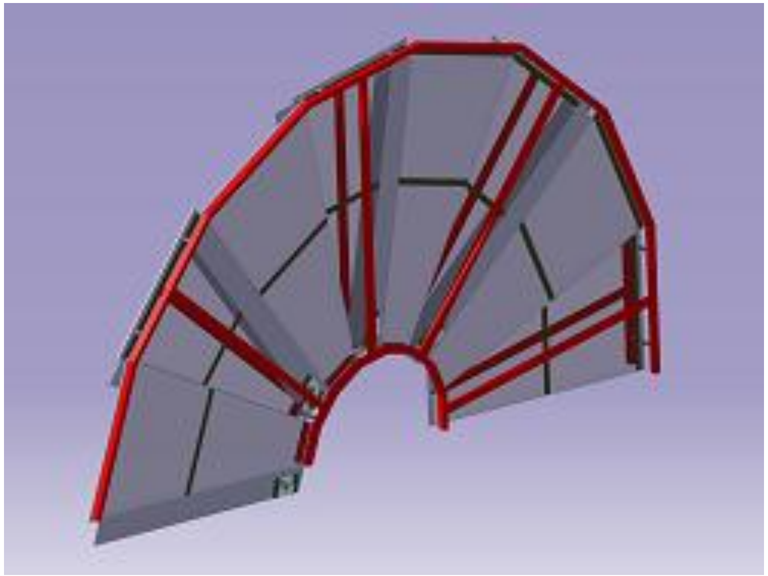
Sensor	R_{min} - R_{max}	column length	pixel dimensions	spatial resolution
A	40-70 mm	14 mm	26×29 μm^2	$\lesssim 6\ \mu m$
B	70-100 mm	20 mm	26×42 μm^2	$\lesssim 7\ \mu m$
C	100-130 mm	26 mm	26×54 μm^2	$\lesssim 8\ \mu m$
D	130-160 mm	32 mm	26×67 μm^2	$\lesssim 9\ \mu m$

- **Pending questions:** ⁎ Stitching ? ⁎ Challenging system integration

Strip pixels: Module design & Support

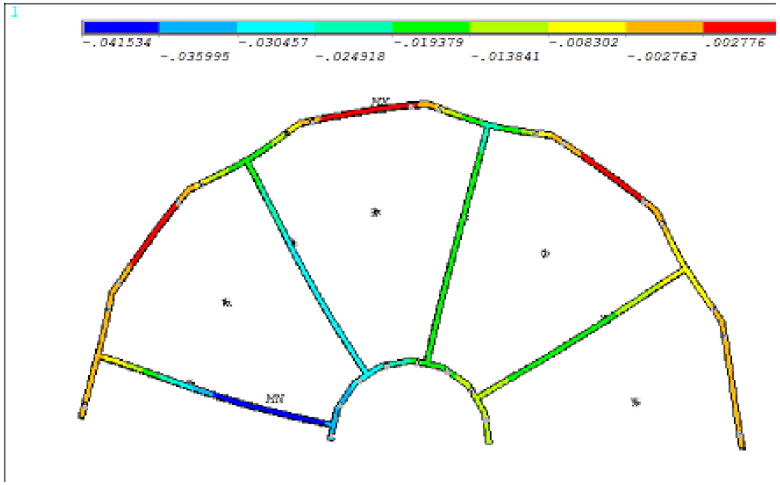
- Baseline sensor: conventional microstrip sensor with integrated signal routing in a second metal layer.
- Baseline operational unit: petal (sensor+standard hybrid board(s) with readout, powering and data link circuitry.





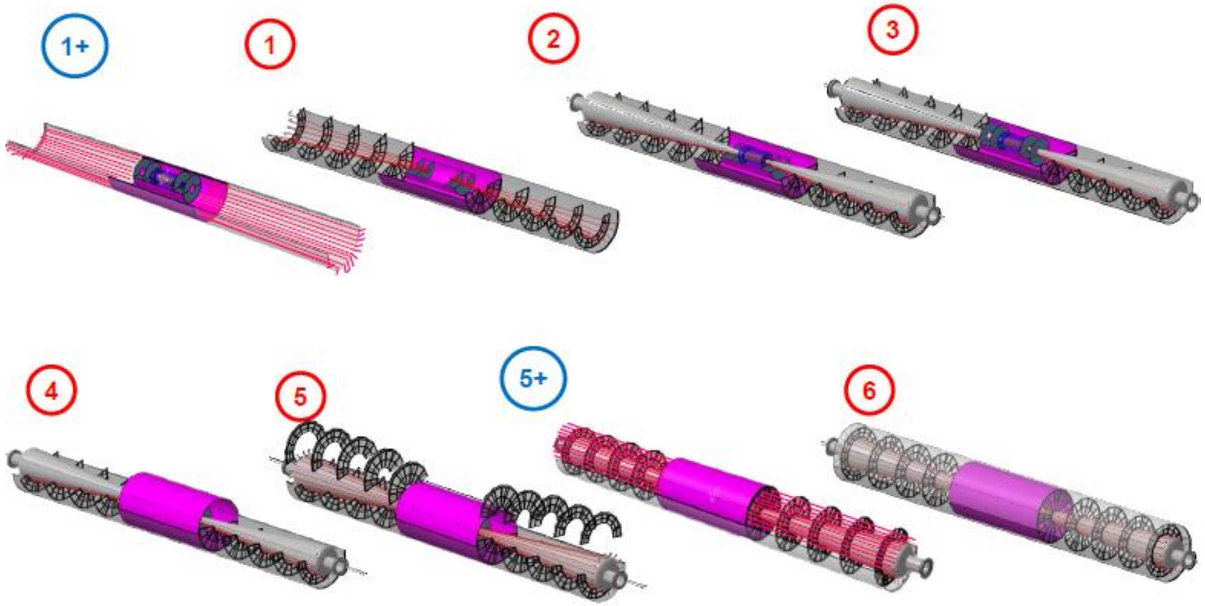
FEA Studies: Stability, Rigidity and Thermal managemente studies

- Still in a preliminary phase.
- Defining the fixation points a its nature.
- Building the thermal model.
- Thermal loads: Quantifiying the thermal sources (R/O chips, optical link, power devices, sensors,…).
- Thermal material characteristic (condutivity, CTE,…)



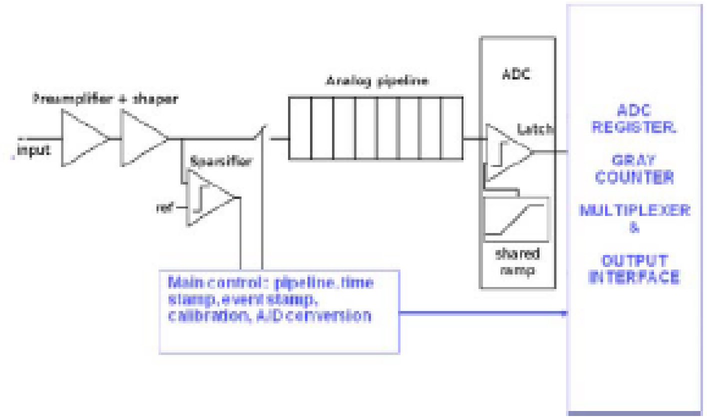
Mechanics: Integration and Services

- Cabling requirements available for strips FTD.
- Cabling required by pixel FTD extrapolated from VTX.
- Assembly & Integration procedure of FTD fixed.



Front End Electronics

- In AIDA-WP9 a readout chip for Si-microstrips for ILD is being developed by UB with 65nm process
  - ✓ Designed:
    - *T indep current source*
    - Amplifier in the preamplifier
    - Preamplifier, shaper
  - ➢ *To be designed*
    - Analog pipeline, Ramp or SAR ADC,
    - Discriminator, sparsifier, digital logic, I2C/SPI, LVDS, …



Concurrent designs with 65nm process:

- 65nm process is used in the development of the DHP together with Bonn Univ. in the framework of DEPFET collaboration for Belle II
  - ✓ Designed, fabricated and tested:
    - *T indep current sources, current-mode DAC*
  - ➢ *Designed*
    - T sensor

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Powering schemes

- The amount of current required by Strip-FTD is around 650 A
- The ILC accelerator has a duty cycle of 0.5%
  - 1 ms bunch train every 200ms
- If the power demanded by the FEE is synchronized with the bunch train, it helps save energy
  - Dissipated energy will be lower
- The total Strip-FTD current demanded per bunch crossing (a peak current) is 650 A
  - Average current 6.5 A. per cycle (no bunch–no power) .
- However several important issues have to be considered during the design of the power system:
  - Transient phenomena
  - EMI phenomena

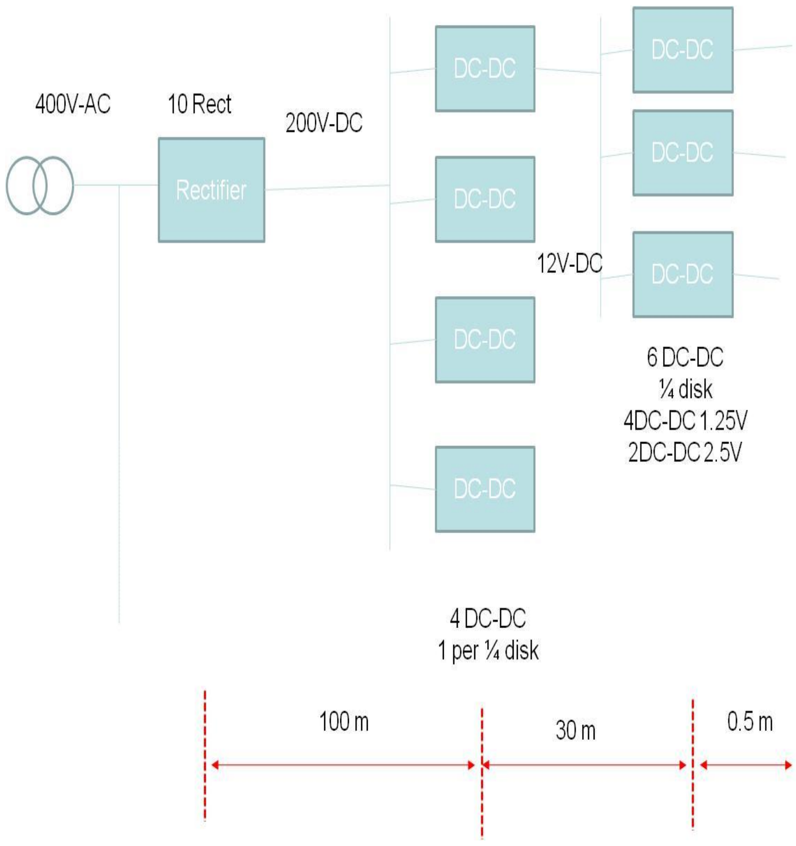
Powering schemes (2)

- All these phenomena have an impact on the design of the power supply distribution system
  - Topology
  - Cooling and material budget
- There are several topologies that may be implemented in the FTD.
  - **DC-DC-based power distribution (baseline)**
  - Supercapacitor based power distribution (beyond baseline)
  - Each of them has advantages and disadvantages
  - Both systems are under study.

Powering schemes: DC-DC-based Power System

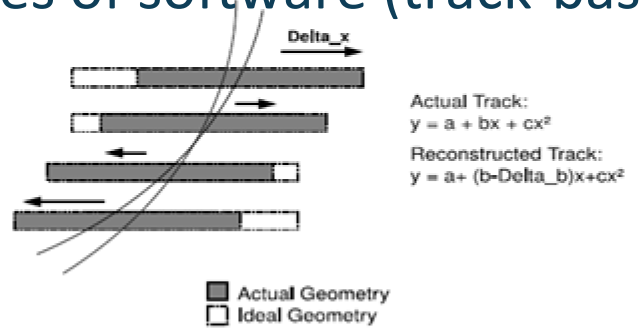
- To absorb transients related to power pulsing system.
  - Keep transients locally at FEE level.
  - Low currents before DC-DC due to converter ratio

    Low transients
- Synergy with SLHC and new DC-DC hard-Rad design.
  - HF noise & Rad issues



Real Time Structural and Environmental Monitoring

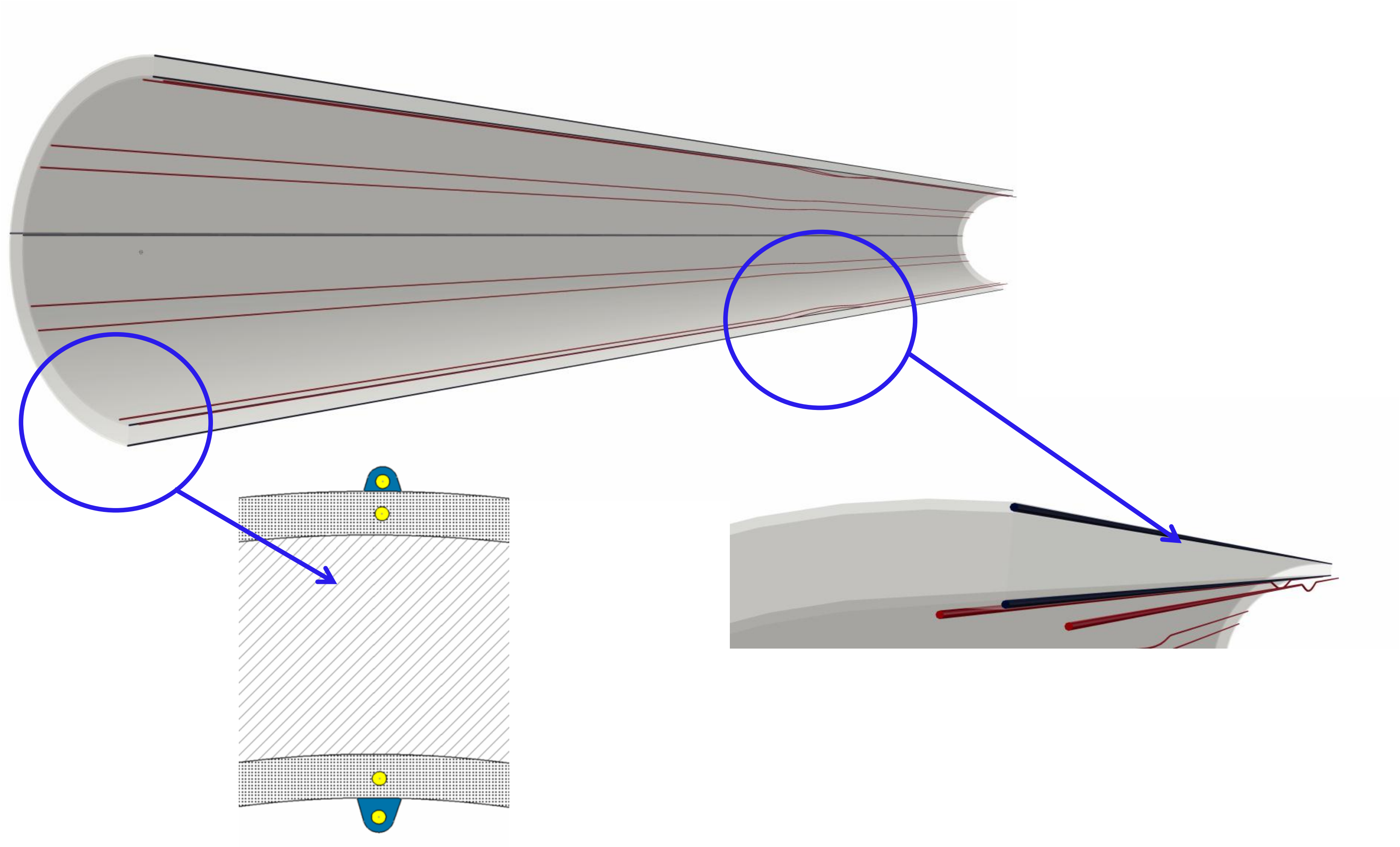
- Current and future silicon systems need for:
  - Real-time monitoring of environment variables: temperature, humidity, CO_2, magnetic field, etc.
  - Real time structural monitoring: deformations, vibrations (push & pull operation), movements.
- Conventional monitoring technologies based on electric relatively bulky transducers with low multiplexing capability, low granularity, and cooper readout and powering lines (conductive EM noise propagation lines).
- First lesson from LHC detectors: position and deformation monitors must cover the weak modes of software (track-based) alignment algorithms.



_Introduction to OFS

- Well know monitoring technologies in aeronautics and civil works based on optical fiber sensors (OFS)
- Distributed strain & temperature sensors are conventionally used for structure health monitoring : *SMART structures*
- Other OFS: dosimetry, humidity, B field, acceleration, etc.
- In aeronautics (embedded or bonded) on the of the CFRP composite (for instance, plane radar radome)

Instrumentation of the CFRP cover (Inner Detector Supporting Cylinder)

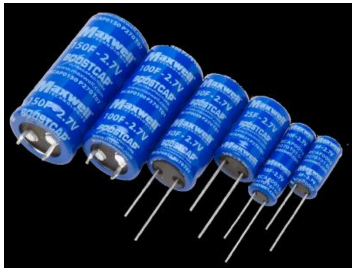


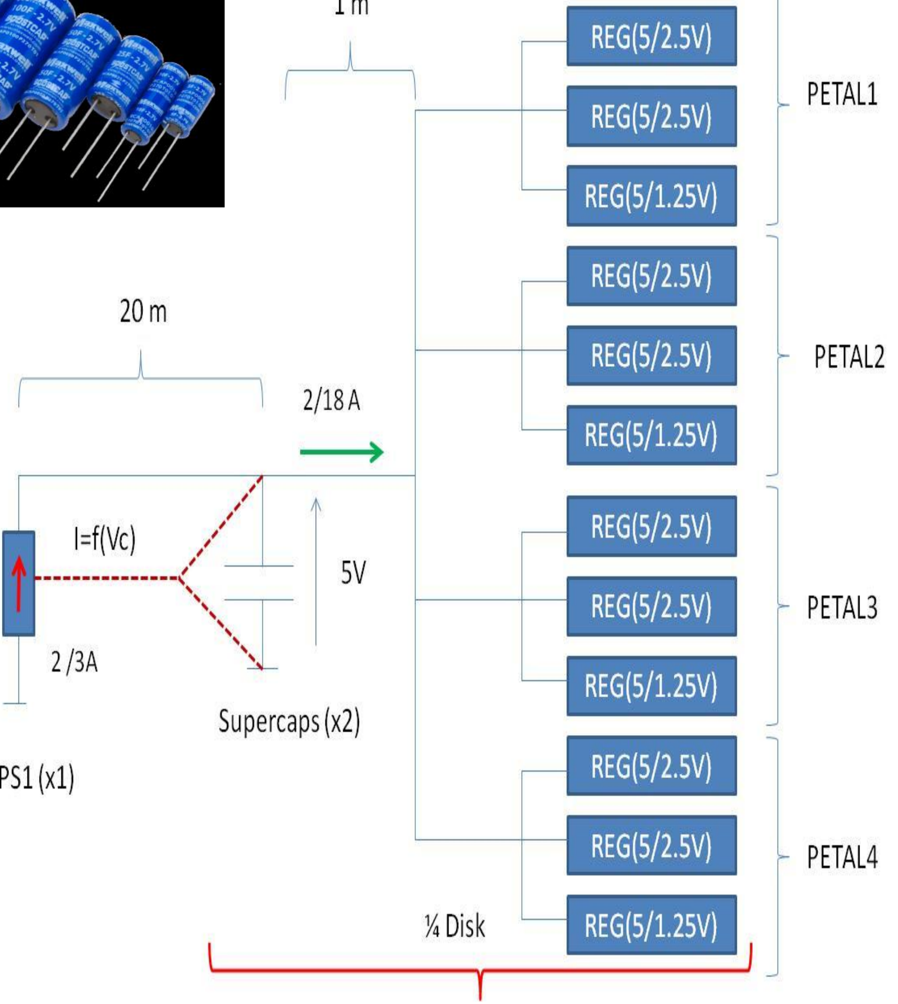
Beyond the baseline

- R&D lines to enhance the detector performance.
- Noiseless and lighter power supply based on supercapacitors.
- Strip sensors providing 2D information:
  - Further radial segmentation of the strips.
  - Resistive collecting electrodes for charge division method implementation in strips.
- Real time position monitoring:
  - Displacement sensors based on FOS FBG sensors.
  - Laser-based position monitoring

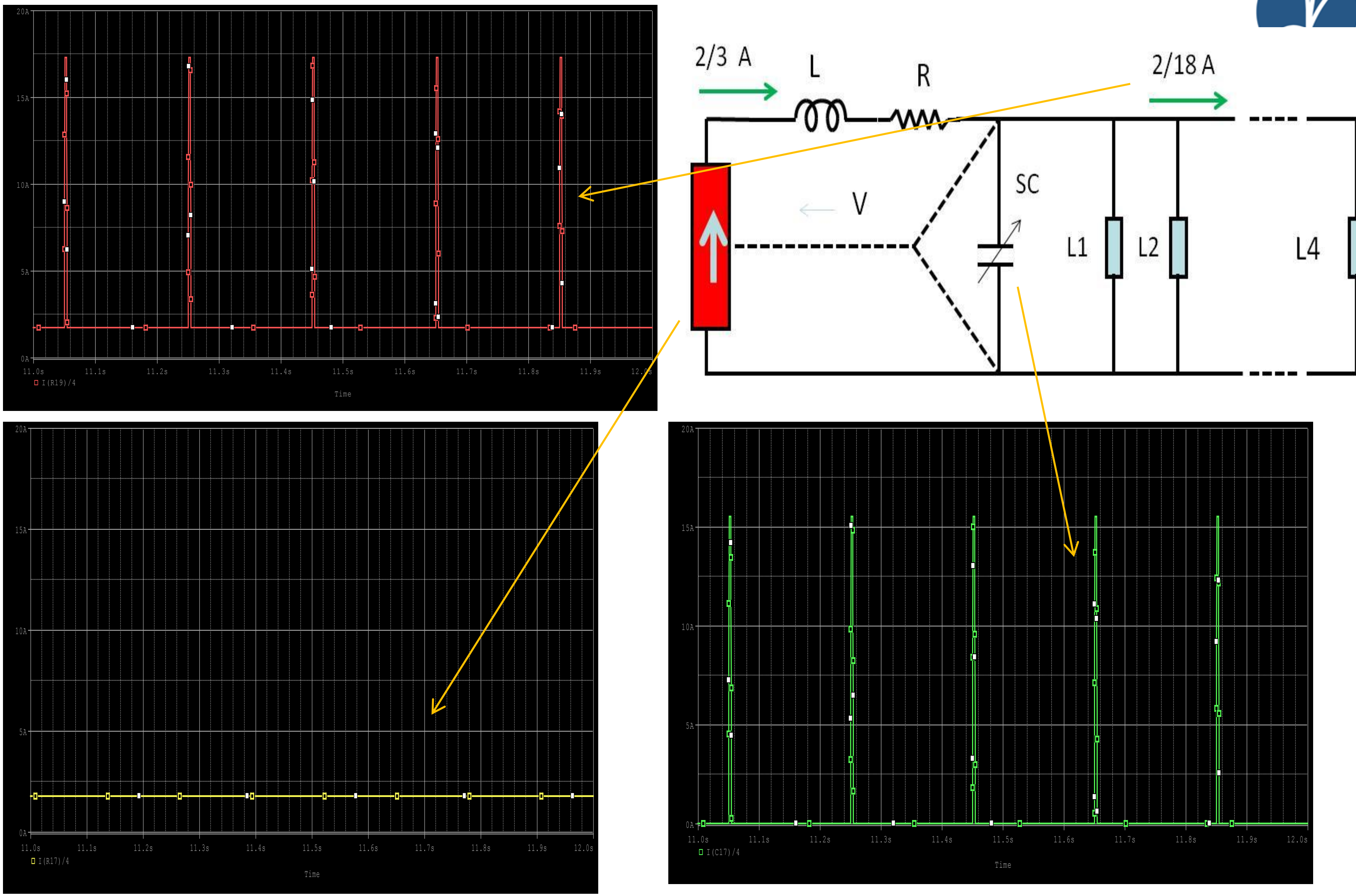
Powering schemes: Supercapacitor based PS

– This power system is based on :
  - **Supercapacitors**
    Pulse power
  - **LV regulators**
    Stabilize FEE voltage
  - **Current source**
    supercapacitor voltage controlled
– To absorb transients related to power pulsing system.
  - Keep transients locally at FEE level.





Powering schemes: Supercapacitor based PS

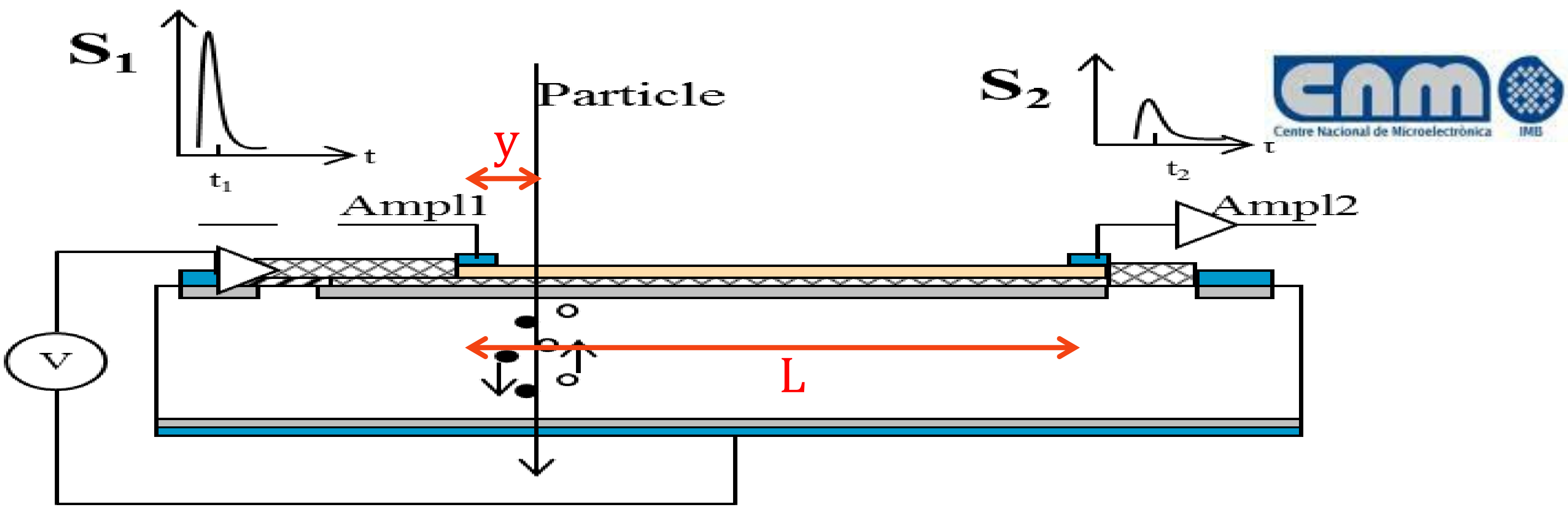


Powering schemes: Supercapacitor based PS

- The most important element is the supercapacitor.
  - It is new for HEP but not for industrial applications
- There are two elements that have to be analyzed in detail for HEP applications
  - Radiation issues
  - Cycling issues.
- Radiation issues
  - Type of radiation: Gamma & electrons
  - Total dose : around 2 MRad.
- Cycling issues (Reliability).
  - Supercapacitor should be able to operate more that 10 million cycles per year
- A detailed test plan is on going to study both effects

Charge-Division Concept in ustrip Sensors

- Charge division used in wire chambers to determine the coordinate along the sensing wire.
- Same concept with conventional microstrips with slightly resistive electrodes (doped polysilicon)



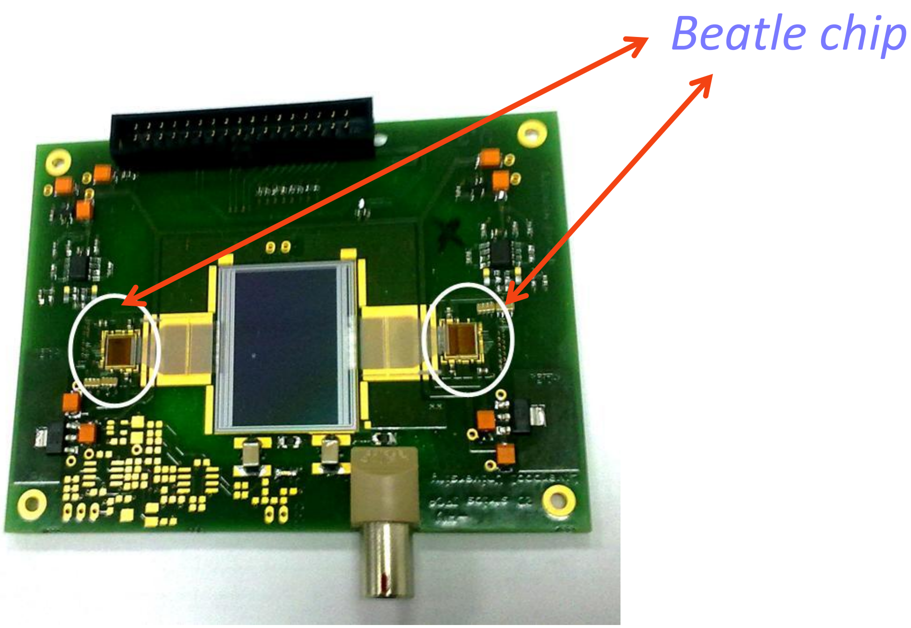
$$\text{Fractional Position} \equiv y/L = S2/(S1+S2)$$

New Prototypes from CNM

– One year ago very promising results on CNM's first prototypes with integrated on sensor signal routing for single-end readout (affected by parasitic couplings, see later in this talk).

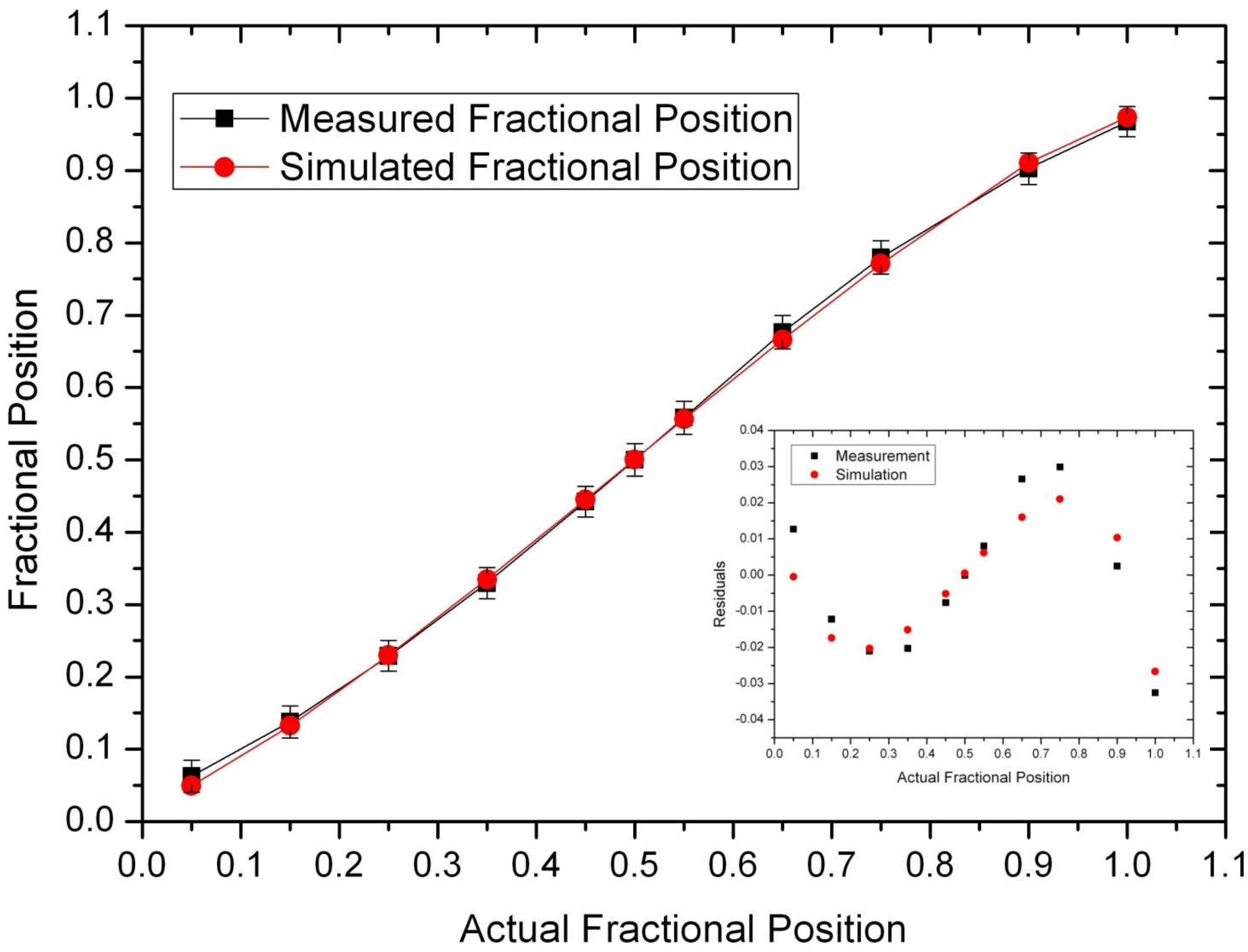
– Now presenting results on two new prototypes with double-end readout.

Strip:
  length =20 mm
  width =20 um
Pitches:
  Implant=80 um
  readout= 80 um
Electrode:
  R/um = 2.8 Ohms/um
  R/um = 12.2 Ohms/um

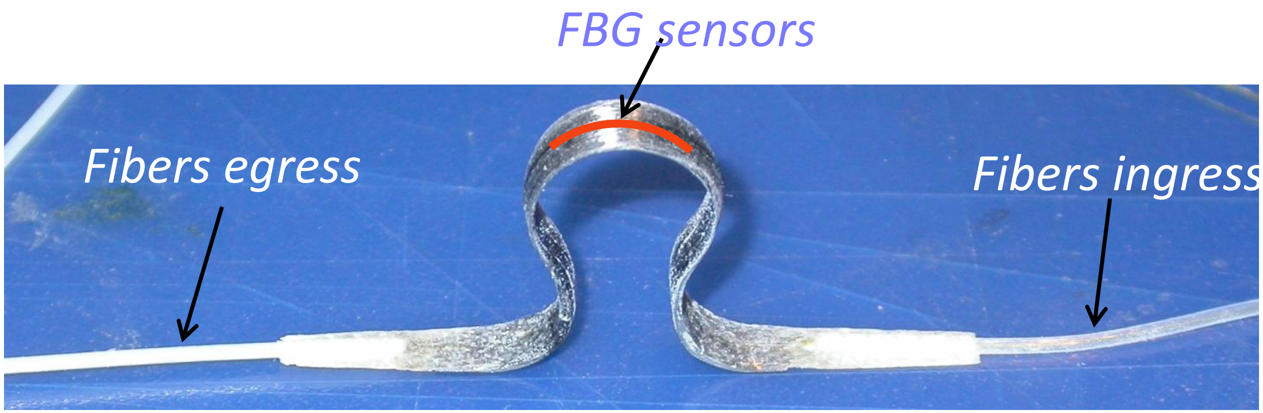


Data vs. Simulation: Fractional position (1)

– High resistivity sensor: 12.2 Ω/µm, RC = 450ns



Miniaturized ultra-light linear position transducer



- Two sensors are positioned in the outer and inner layer of the omega (point of maximum strain / maximum resolution)
- One sensor in the middle layer to compensate temperature (point of minimum strain)
- The temperature can be compensated with the difference in the measurement of bottom and top sensor)

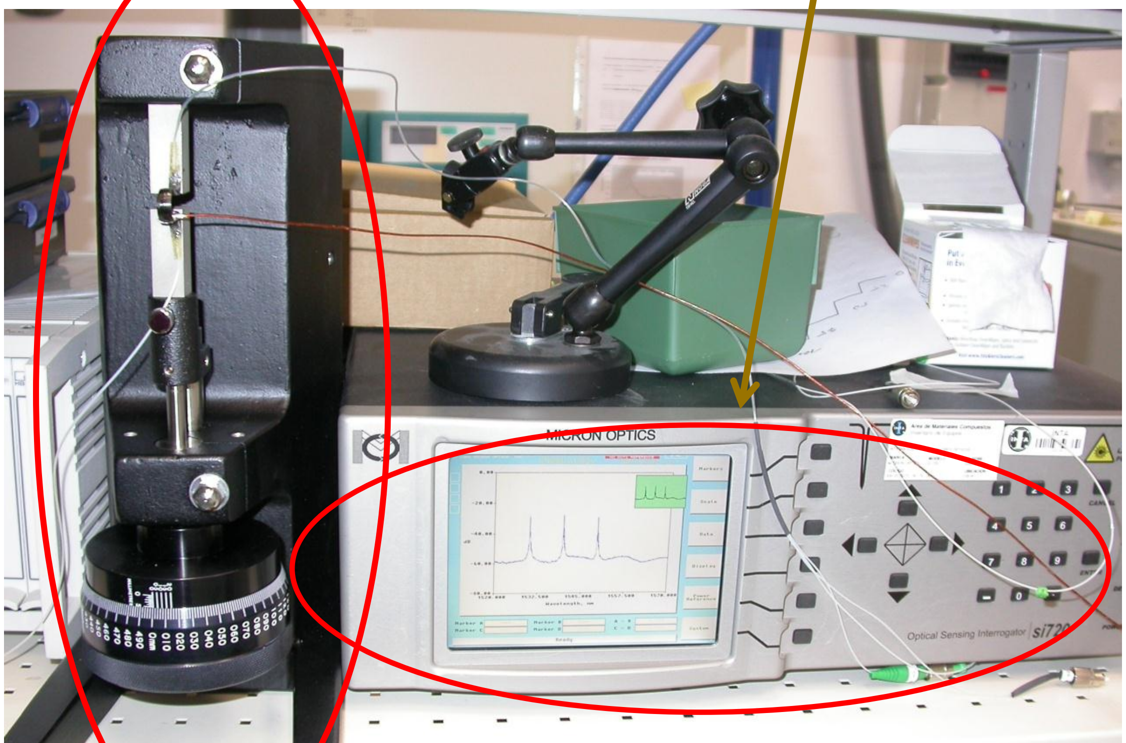
Results on first Omega Prototypes

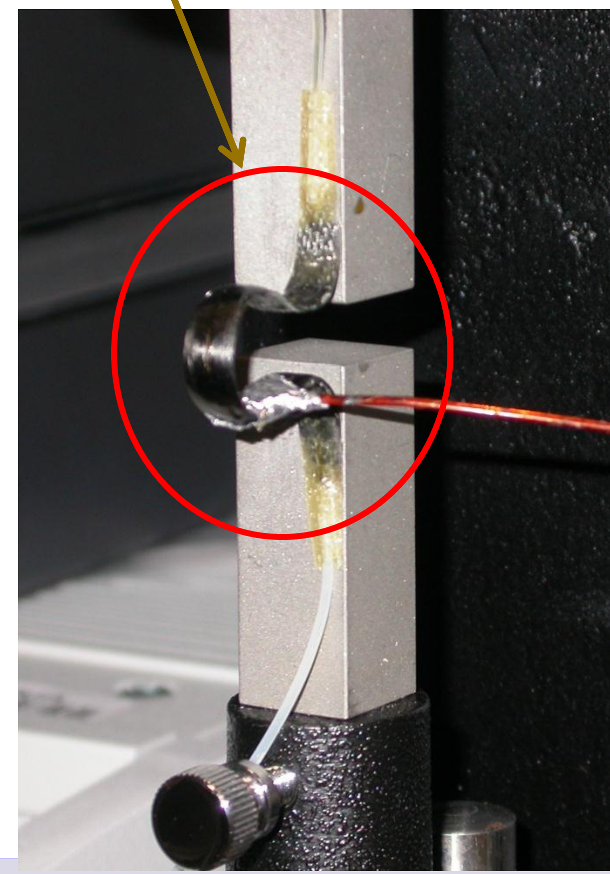
Micrometric Stage

FBG sensor

interrogation unit

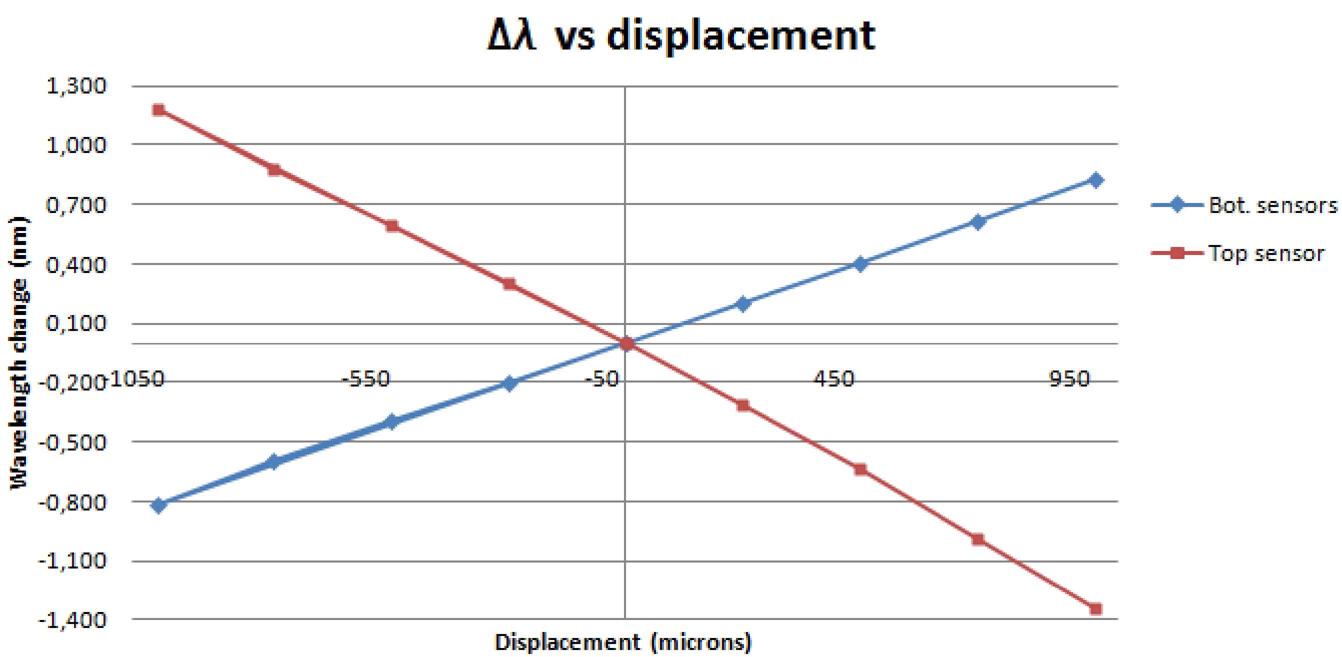
Omega





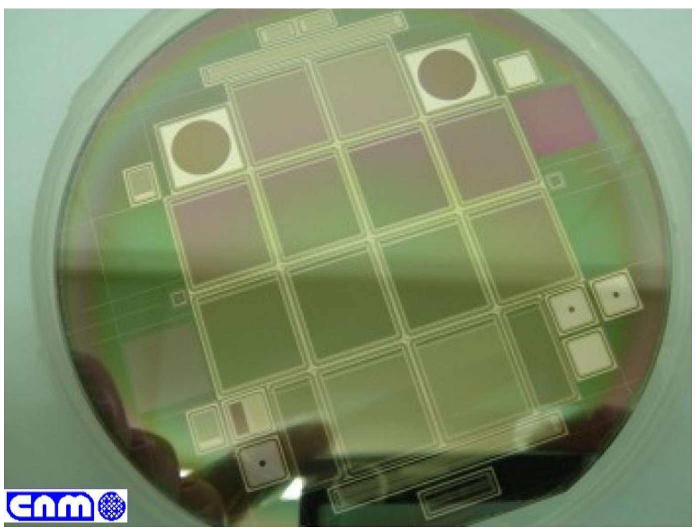
_Omega First measurements

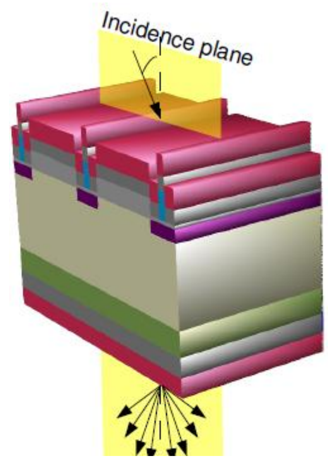
- The obtained displacement resolution is of 0.5 um
- The relation is lineal in the range +1mm to -1 mm
- The temperature can be compensated by difference between the top and bottom sensor
- The omega will be tested in Santander again to measure the reaction and have redundancy in the results obtained.

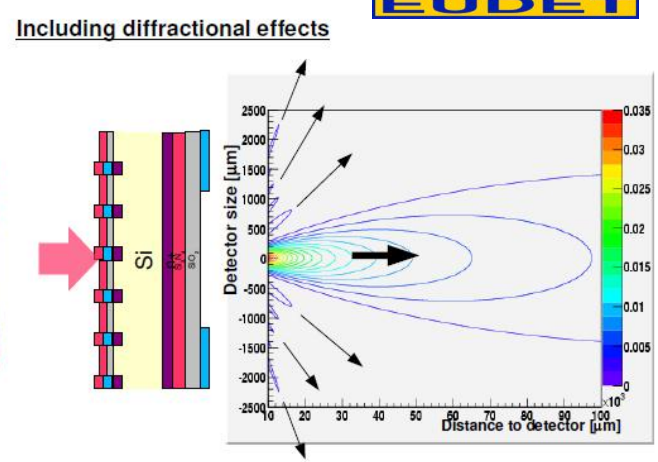


Real time Relative position monitoring of FTD forward-backward halfs (2)

- Optical optimized strip sensors developed within EUDET FP7 proyect (transparency tunned using the estándar fabrication process)







Summary

– Baseline design based on 100% standard and available technologies.

– Additional R&D lines on:
  - Front-end electronics
  - Power supply (Supercapacitors based)
  - 2D resistive strip sensors
  - FOS-based Miniaturized hard-rad linear displacement transducers.
  - Semitransparent alignment strips sensors.

GRACIAS

BACK UP

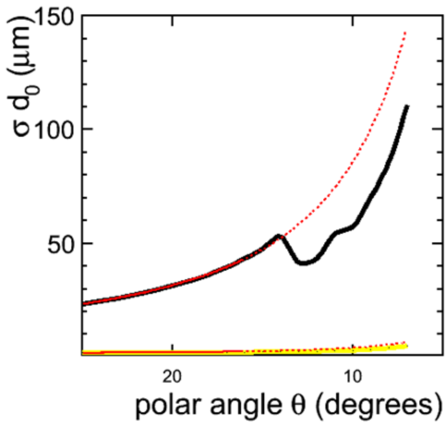
Layout Optimization: fast simulation

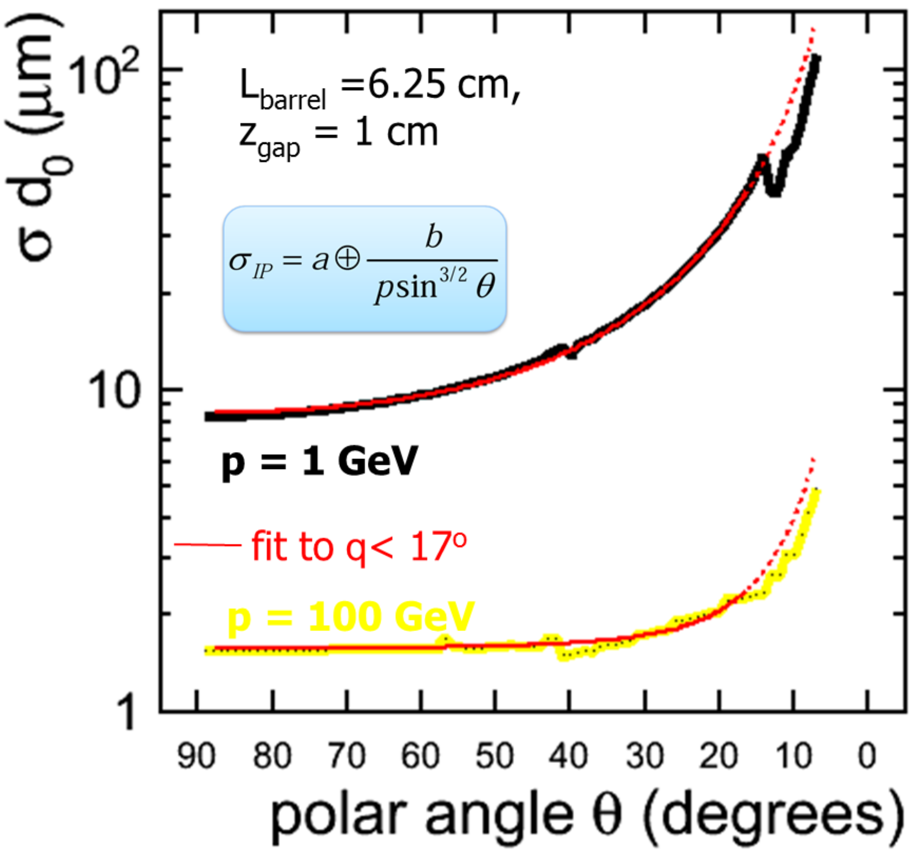
Transverse impact parameter resolution

Transverse impact parameter resolution vs. polar angle

Barrel-dominated part well-described by the standard formula.

Deviations in the very forward region (as expected)





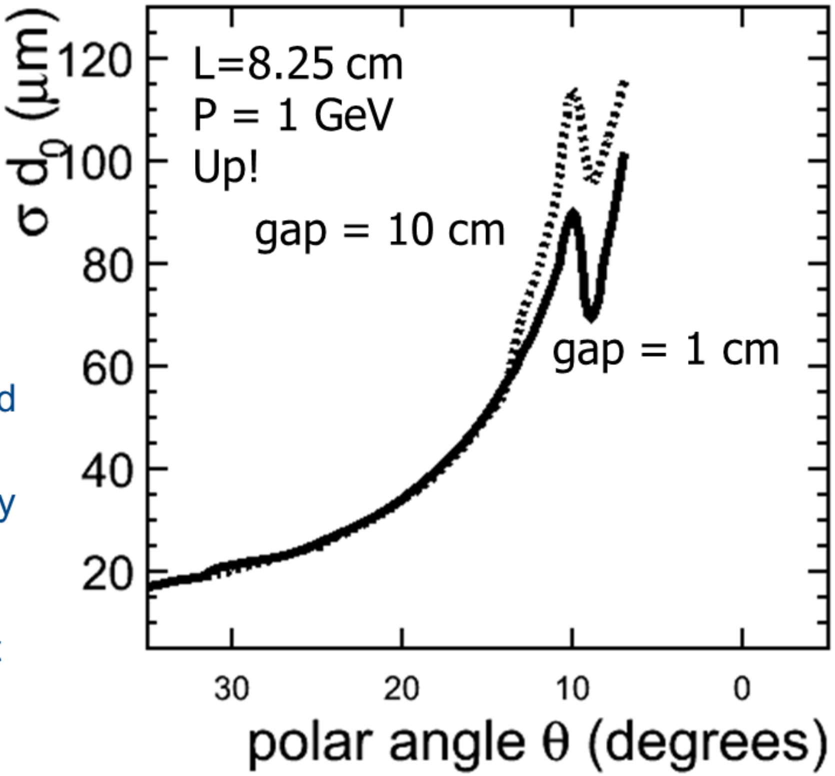
Zgap between the FTD1 and VTX

Comparison z_{gap}

Minimize the gap! *

But: if we route the services along the beam pipe, the forward vertexing performance is terrible and essentially insensitive to z_{gap}

* In ILD the distance between VXD and innermost FTD is close to 10 cm. This clearance is motivated by the possibility to fit in a VXD cryostat. If a “cold” VXD technology is chosen, a short gap implies one has to install the innermost disks inside the cryostat.



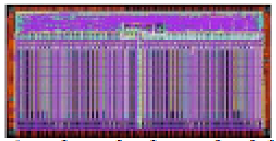
Front-end Electronics: new approach

FPA2008-04122-E | FPA2008-05979-C04-02 | AIDA

2007 | 2008 | 2009 | 2010 | 2011

Start of collaboration with IN2P3
Design of the digital part

SiTR-88-130UMC

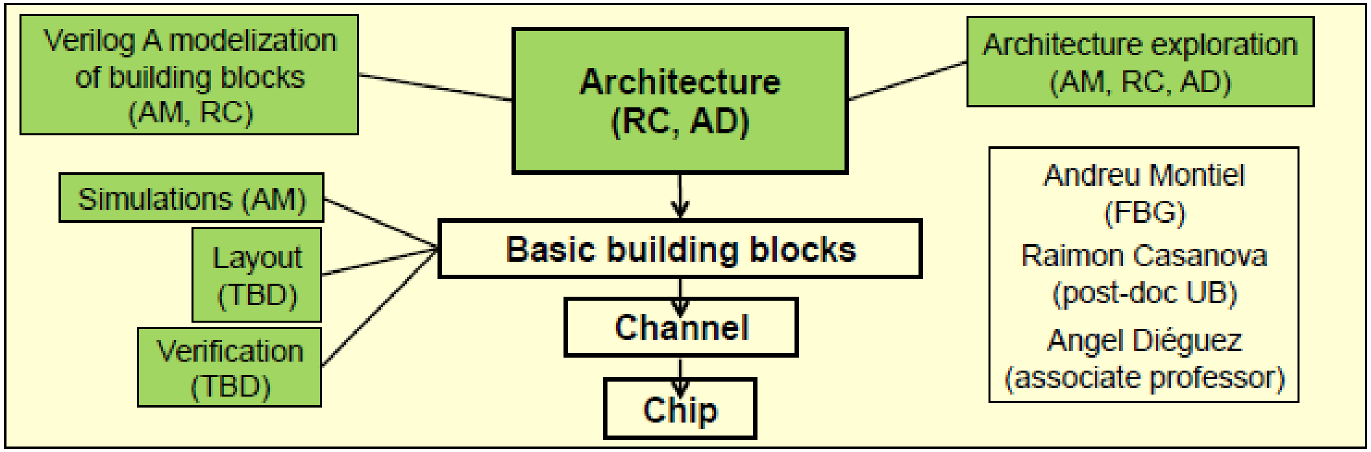


(1st mixed signal chip)

Definition of new architecture

the 128 ch Si-FE ASIC

Complete new design (responsability of UB)



AIDA

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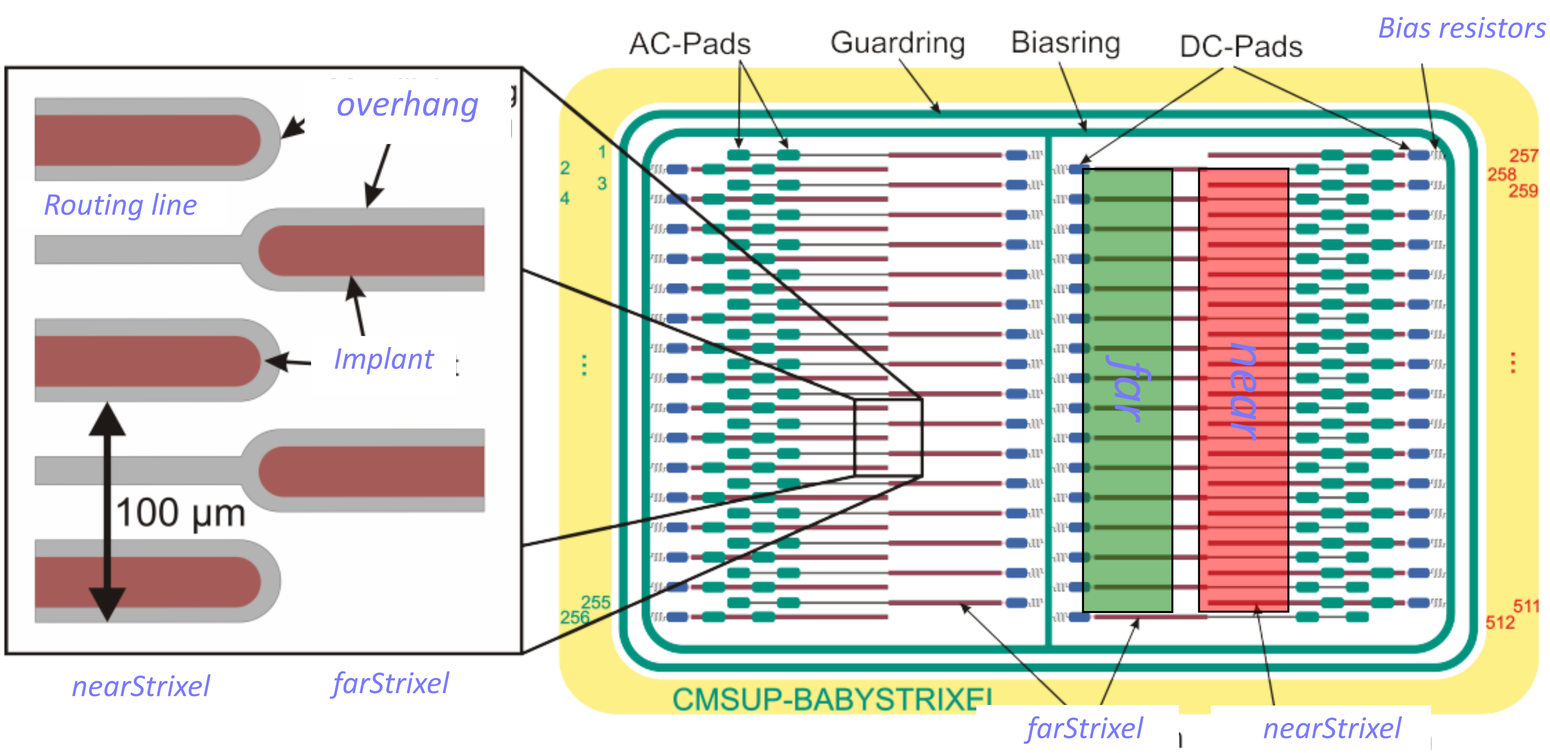
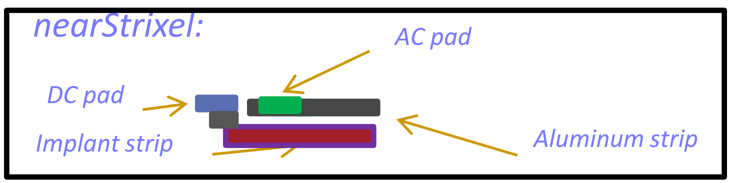
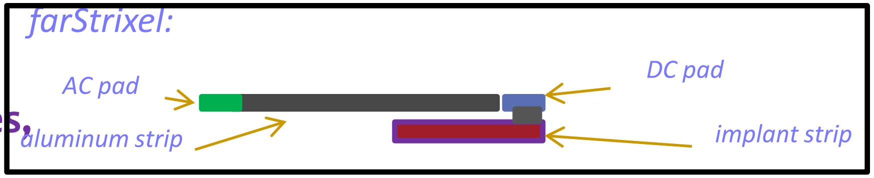
Stripxels – schematic overview



- *increases granularity by a factor of 4*
- *readout at the sensor edges*
- *Distinguish between near and far region (nearStrixel / farStrixel)*



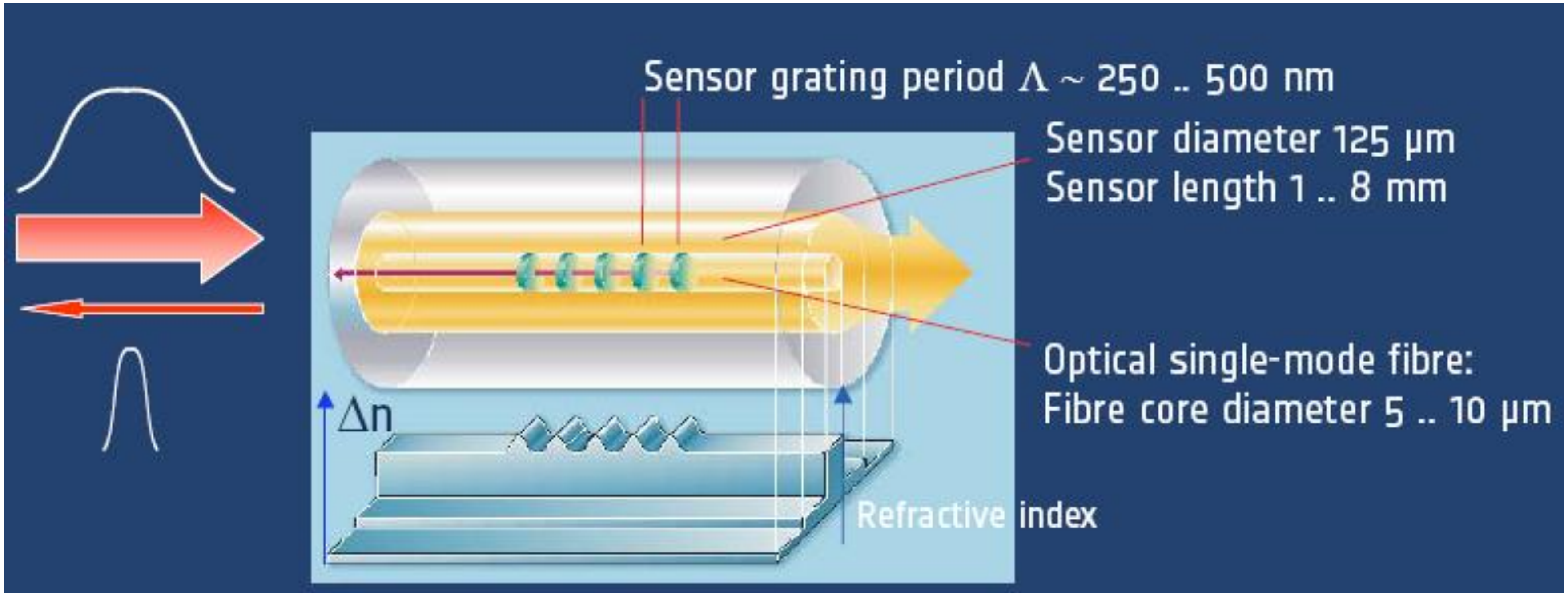


2.1 Powering schemes: DC-DC-based Power System

- Example (1/4 disk) : Power values per group:
  - Routing inside each petal:
    - 6 DC-DC converters
      - 4 DC-DC (12V - 2.5V)
      - 2 DC- DC (12V- 1.25V)
    - Max out current per DC-DC less than 3 A (low transients)
    - Short cabling – Less than 1 meter (low voltage drop)
  - Outside petal (1 cable per ¼ disk)
    - 1 DC-DC per power group
      - 200V – 12V
    - Max out current per DC-DC less than 3 A
      - Transients attenuated by the DC-DC
  - Outside experiment
    - 1 AC-DC per disk
      - 400V 50 Hz – 200V DC
    - Max current per cable less than 1 A

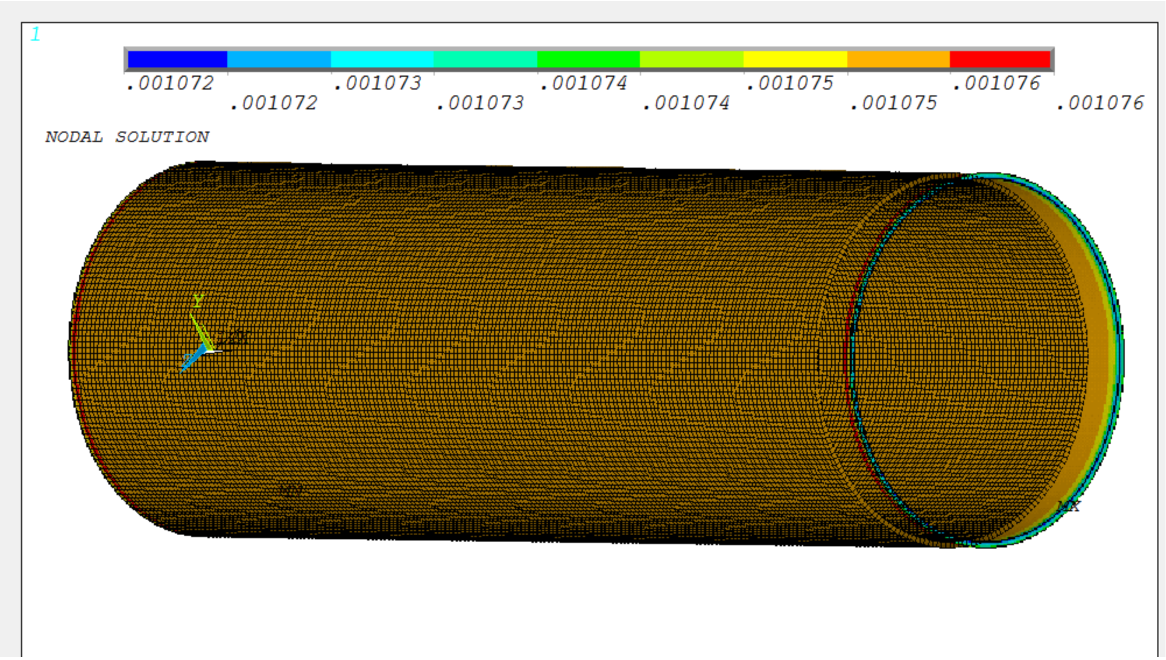
Fiber Bragg Grating Optic Sensor 101

– Keep in mind: Physically, FGB sensors have a section of an optical fiber with a length of few millimeters.



Monitoring of CFRP cover deformation

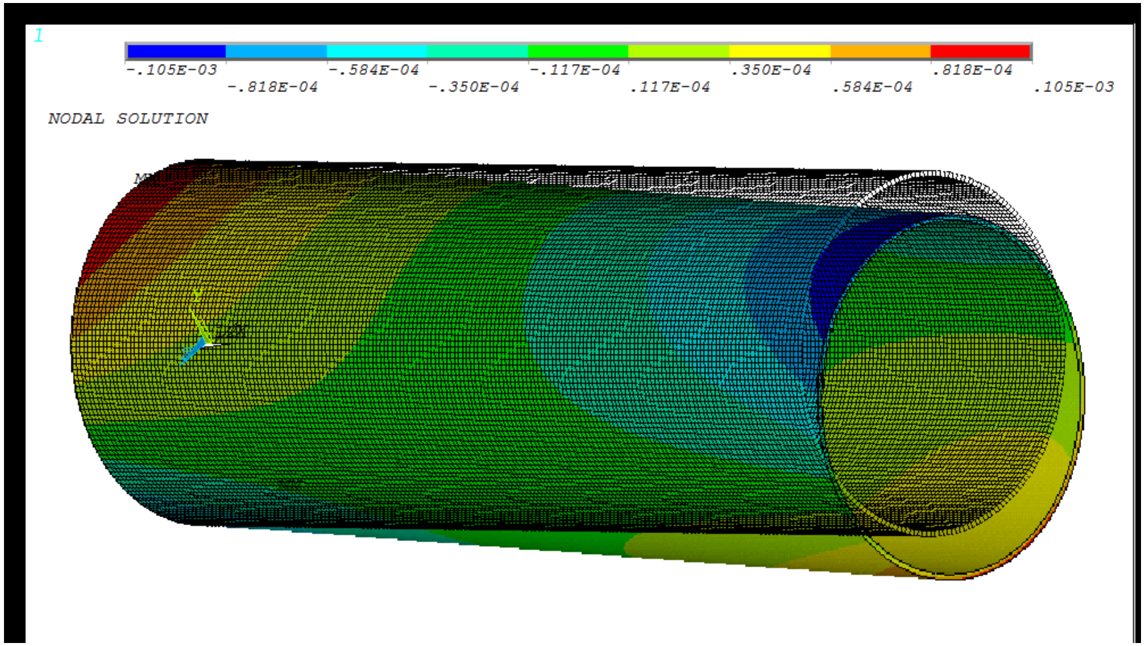
– Name of the game: extract cover deformations out of FBG readout.



Z(mm)	0	60	120	180	240	300
20	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03
465	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03
910	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03	1,075E-03

Monitoring of CFRP cover deformation (2)

– Relative movement between cylinder end flanges.

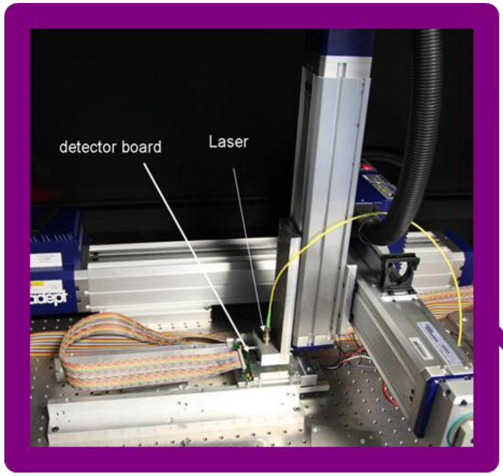


Z(mm)	0	60	120	180	240	300
20	-1,535E-06	-8,455E-05	-1,535E-06	8,302E-05	8,302E-05	9,294E-12
465	-1,979E-07	-1,725E-10	-5,479E-15	6,246E-15	-1,500E-14	5,559E-06
910	-1,500E-06	8,112E-05	8,112E-05	-1,500E-06	-8,112E-05	-3,840E-05

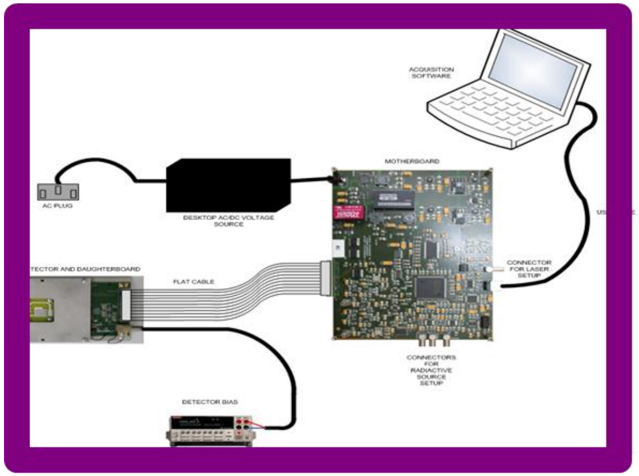
FOS for environmental and structural monitoring industry driven technology

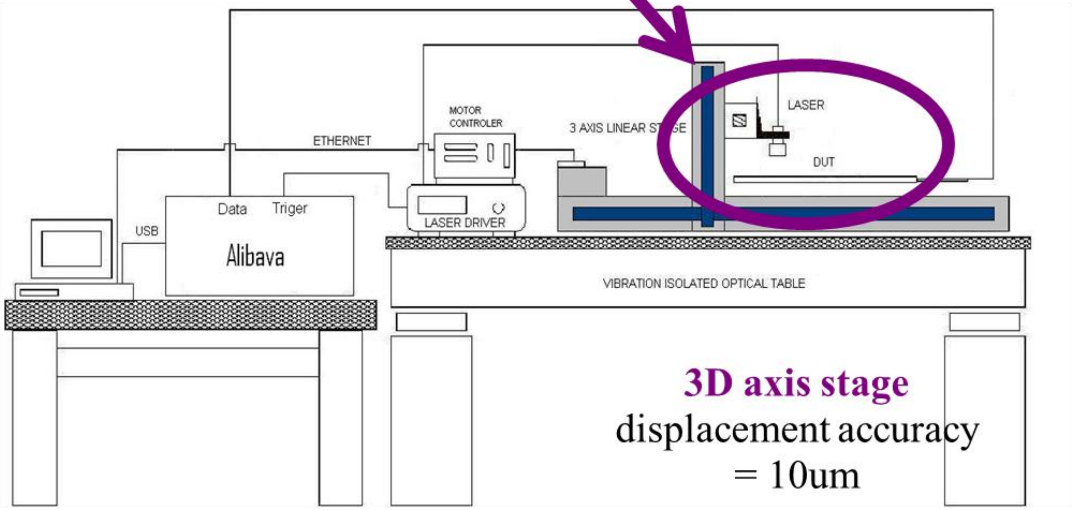
NIR laser test stand

ALIBAVA DAQ system
* Beetle readout chip
* 256 channels
* peaking time ~ 25 ns
* S/N ~ 20 (standard and non irradiated detectors)



Pulsed DFB laser λ=1060nm
- gaussian beam spot width ≈ 20 μm
- rise time 2ns
- **total charge ≈ 5-10 MIPs**



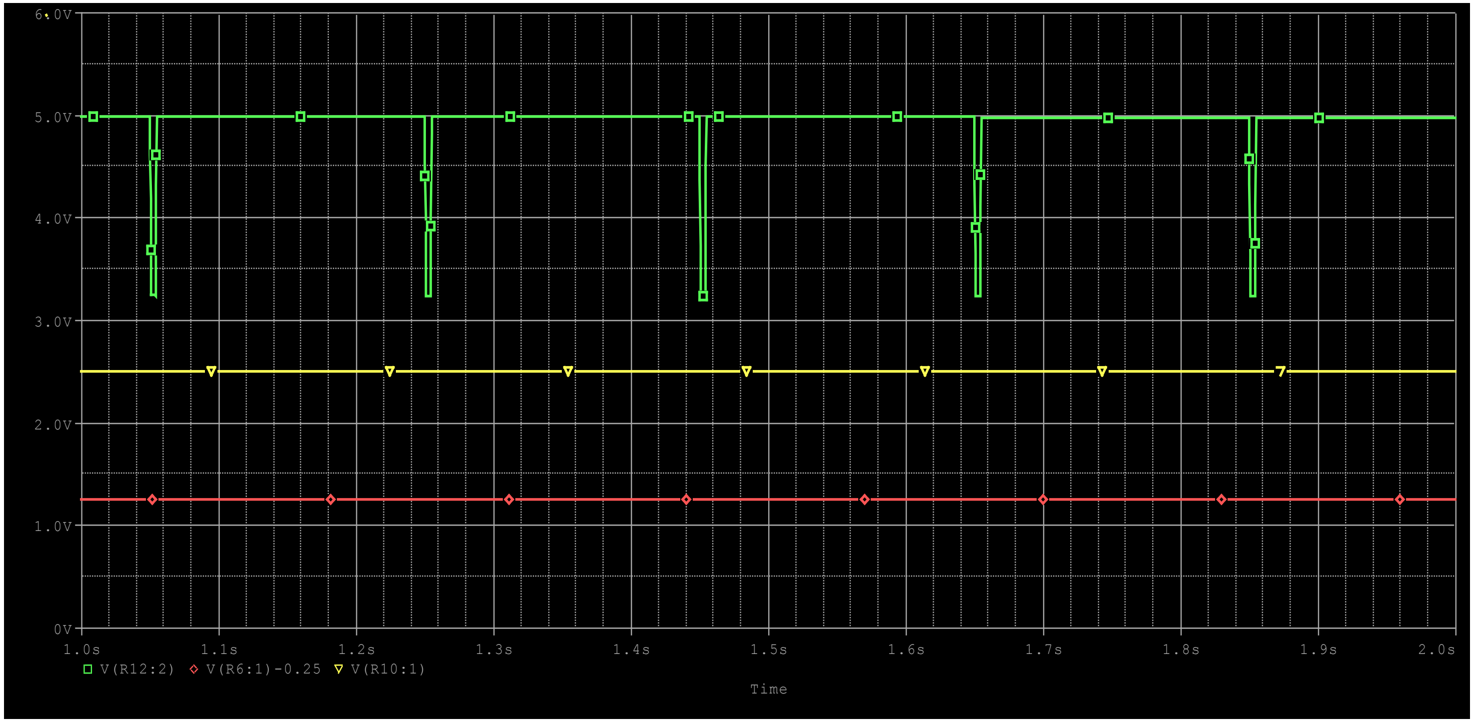


3D axis stage
displacement accuracy = 10um

Powering schemes: Supercapacitor based PS

- Each pulse generates a voltage dip
  - It is mainly influenced by the ESR of the supercapacitor

    Line impedance, too.
- Transient can be easily absorbed by the LV regulator
  - It should be a RAD tolerant component



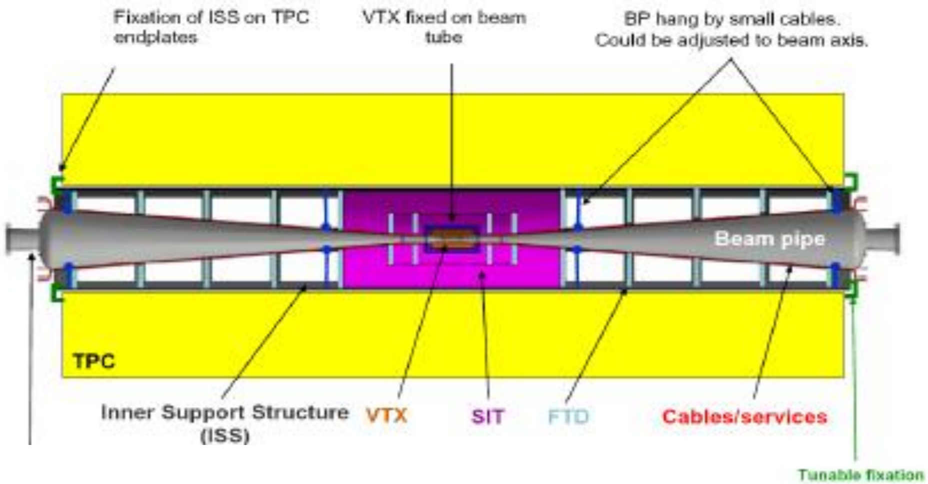
Powering schemes: Supercapacitor based PS

- Power values per ¼ disk (power group)
  - Routing inside each petal
    - 3 Regulators
      - 2 REG (5V -2.5V) / 2.92 A Pk – 0.29A
      - 1 REG (5V- 1.25V) / 1.42 A Pk – 0.15A
    - Max out current per petal (16 petals) – 4.34 A / 0.434A)
    - Short cabling – Less than 1 meter (low voltage drop) ?
    - 2 Supercapacitors per (1/4 disk) – C=75 F / V=5 V / Imax=18 A /Imin=2
  - Outside petal - ¼ disk
    - 1 Cable per disk
    - Max out current per cable around 2/3 A (defined by FEE)
  - Outside experiment
    - 1 Current source per ¼ disk
      - IDC = 2/3 A
- A similar number of HV cable will be considered to keep the same granularity
  - 1 HV cable and HV power unit per ¼ disk

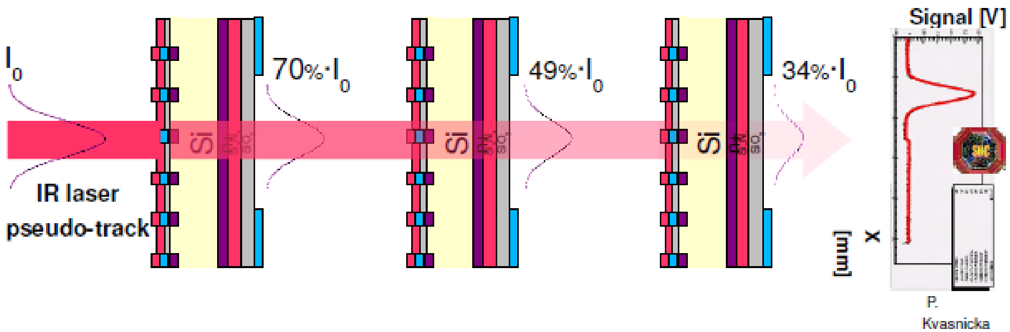
Future plans for power issues

- A comparative analysis of power dissipation of both DC-DC based and supercapacitor based power systems
- Supercapacitor option :
  - Radiation effects on supercapacitor : Test campaign
  - Reliability issues : Power cycling effects
- DC-DC option:
  - It is planned to follow the CERN group development of RAD and magnetic field tolerant DC-DC converters.
  - Power cycling effects

Real time Relative position monitoring of FTD forward-backward halfs.



- Laser tracks can be used by a hardware system to align the tracker



- First implemented by AMS I, then AMS II and CMS