Latest depleted CMOS sensors developments in the CERN RD50 collaboration

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on behalf of the CERN RD50 collaboration.

Outline

- CERN RD50 depleted CMOS activities.
- RD50 depleted CMOS device development roadmap.
- RD50-MPW2 device main characteristics.
- Measurements of RD50-MPW2 test structures.
- Characterization of RD50-MPW2 active matrix.
- RD50-MPW3 device design overview.
- Summary and outlook.

CERN RD50 depleted CMOS activities

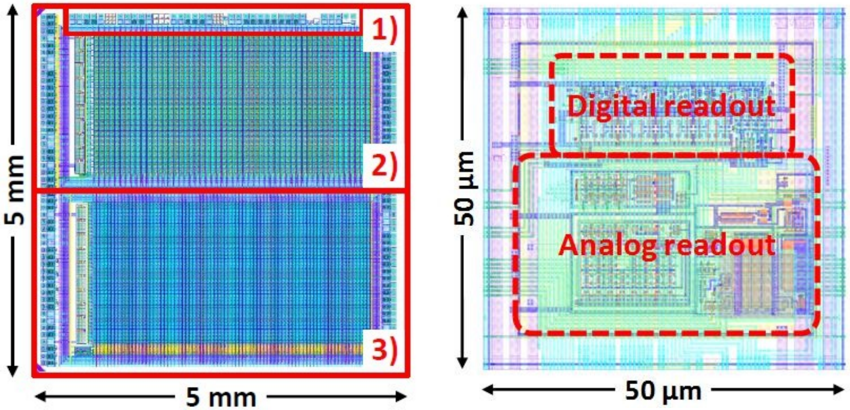
- **CERN RD50 collaboration.**
  - International collaboration with more than 300 members.
  - Aimed at developing and characterizing radiation-hard semiconductor devices for high luminosity colliders.
  - R&D carried out in new structures (3D, LGAD, Depleted CMOS, etc.): see talks from E. Curras (D06) and J. Duarte (B02) for more info about LGAD and 3D developments within RD50.
- **Depleted CMOS sensors** have a huge potential for future experiments in physics: **high priority in RD50.**
- **RD50 has a program** to develop and study these sensors.
- **Activities included.**
  - TCAD simulations.
  - ASIC design.
  - DAQ development.
  - Device performance evaluation.
- **Resources involved.**
  - ~ 36 people.
  - ~ 12 institutes.

RD50 depleted CMOS device development roadmap

- **All devices developed as MPW in the 150 nm HV-CMOS process from LFoundry: large collection electrode.**

To gain expertise, test the process and test novel designs.

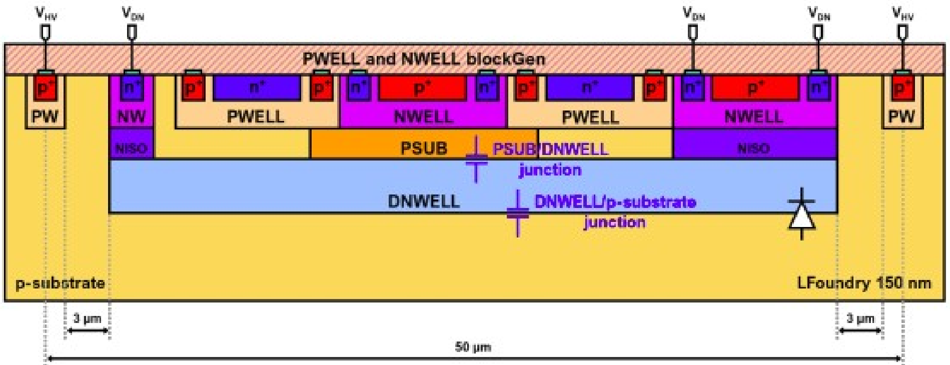
- **RD50-MPW1: submitted 11/2017 and received 04/2018.**
  - Size of 5 mm x 5 mm. Thickness of 280 µm.
  - 2 different substrate resistivities (500 Ω·cm and 1.9 kΩ·cm).
  - Two independent pixel matrices (50 µm and 75 µm) with analog and digital readout embedded in sensing area.
  - Test structures for e-TCT, C-V and I-V measurements.



RD50-MPW1 floor plan (left) and pixel detailed view (right)

Pixel I_{leak} found too high and V_{BD} lower than expected. Crosstalk in some digital readout lines from pixels.

- **Focus on the pixel and analog readout design in a small prototype with same technology.**
  - Control of structures added by LFoundry for fabrication.
  - Improved guard ring scheme at chip edge.
  - Improved pixel corner geometry (rounded) and more P-substrate/deep n-well spacing to increase breakdown voltage.
  - Improved readout amplifier design with faster output rate.



RD50-MPW1 pixel cross section

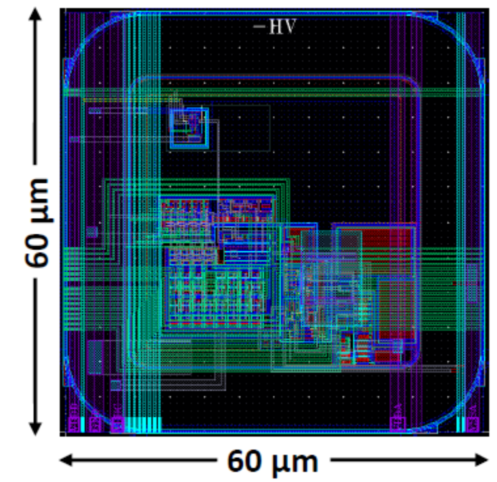
Reported by E. Vilella, Vertex 2019

RD50 depleted CMOS device development roadmap

To implement methods to minimize the leakage current and improve amplifier rate.

- **RD50-MPW2: submitted 01/2019 and received 02/2020.**
  - Reduced size.
  - 4 different substrate resistivities.
  - Small pixel matrix with analog readout embedded in sensing area.
  - Test structures for e-TCT, C-V and I-V measurements.

Measurements with RD50-MPW2 reported in this talk

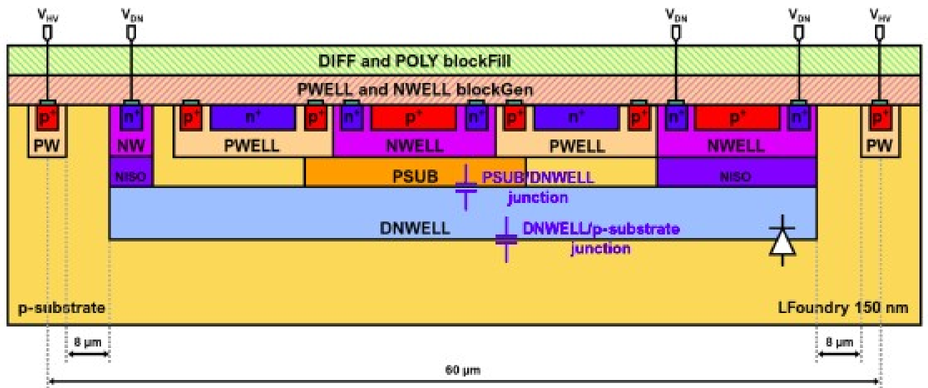


RD50-MPW2 pixel detailed view

To improve the digital readout and avoid crosstalk issues detected in RD50-MPW1.

- **RD50-MPW3: to be submitted in 01/2021.**
  - Same size as RD50-MPW1.
  - At least one pixel matrix with same pixel as in RD50-MPW2.
  - Analog and digital readout embedded in sensing area.

RD50-MPW3 design overview reported in this talk



RD50-MPW2 pixel cross section

RD50-MPW2 main characteristics

- **MPW** in the **150 nm HV-CMOS process** from **LFoundry**: **large collection electrode**.
- **Size** of **3 mm x 2 mm**. **Thickness** of **280 µm**.
- **Substrate** available in **4 different resistivities: 10 Ω·cm, 0.5-1.1 kΩ·cm, 1.9 kΩ·cm** and **>2 kΩ·cm**.
- **80 samples** of **each resistivity**.
- **Chip contents**.

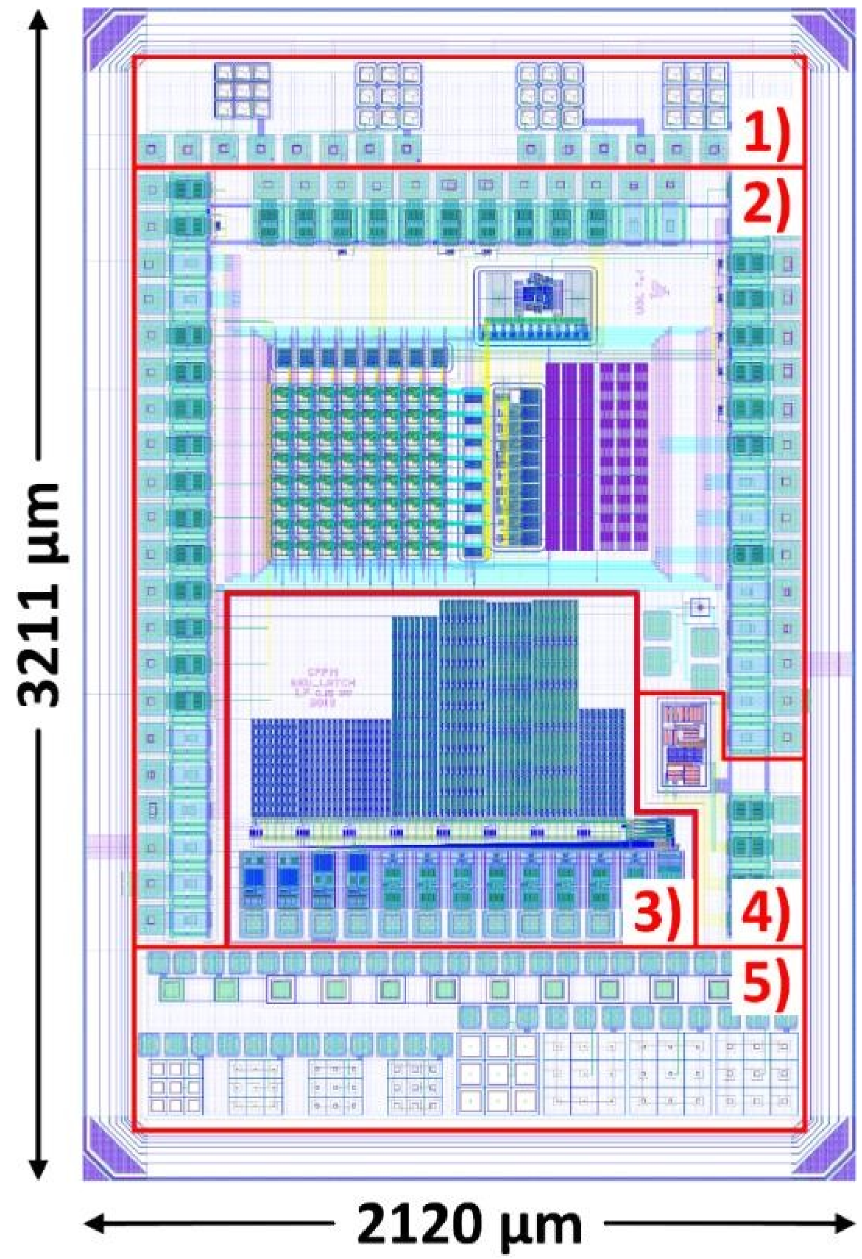
1) **Test structures** with **depleted CMOS pixels**.

2) **Matrix** of **8 x 8 depleted CMOS pixels** of **60 µm** with **embedded analog readout**.

3) **SEU tolerant array.**

4) **Bandgap voltage reference.**

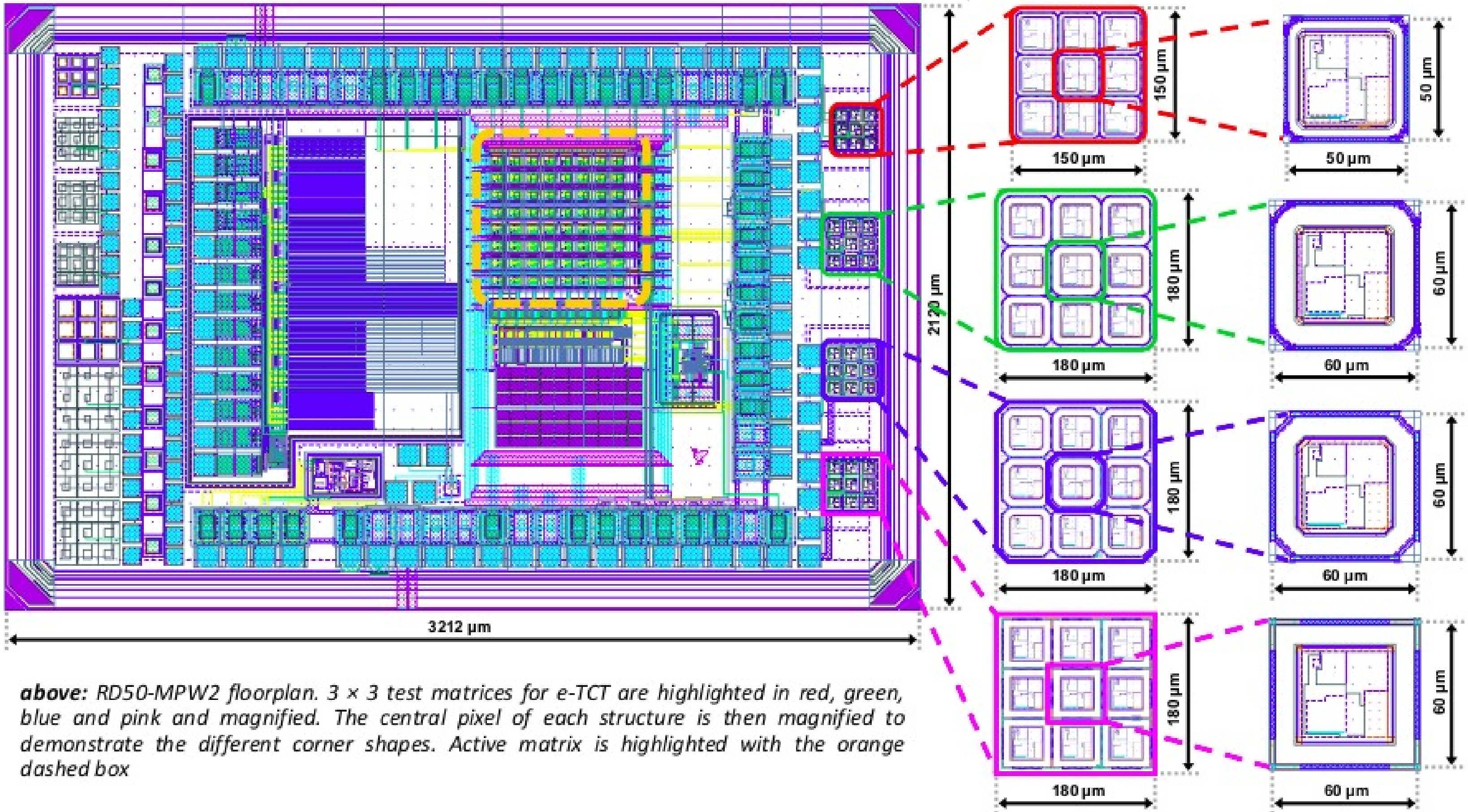
5) **Test structures** with **SPADs** and **depleted CMOS pixels.**



RD50-MPW2 floor plan

RD50-MPW2 test structures measurements: I-V ($\Phi_{eq} = 0$)

- **RD50-MPW2 different test matrices characteristics.**



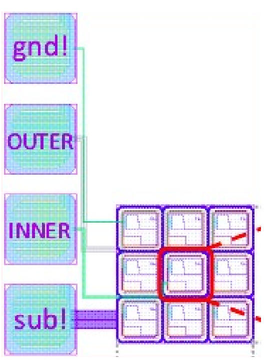
Test matrix 1 for e-TCT
- **50 µm × 50 µm** pixel
- 3 µm electrode spacing
- **Rounded** corners
- (Similar to RD50-MPW1)

Test matrix 2 for e-TCT
- **60 µm × 60 µm** pixel
- 8 µm electrode spacing
- **Rounded** corners
- (Geometry shared with the pixels in the active matrix)

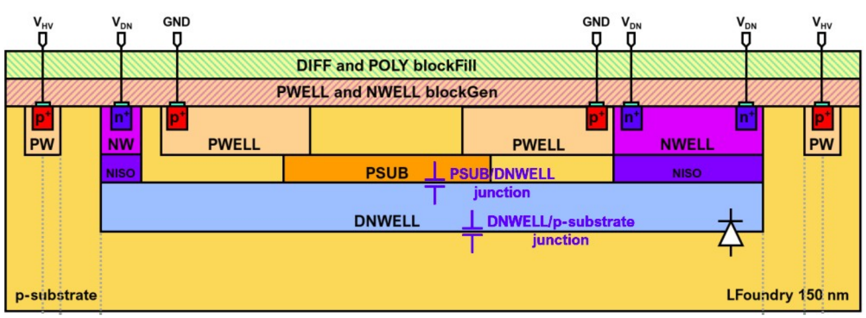
Test matrix 3 for e-TCT
- **60 µm × 60 µm** pixel
- 8 µm electrode spacing
- **Chamfered** corners

Test matrix 4 for e-TCT
- **60 µm × 60 µm** pixel
- 8 µm electrode spacing
- **Squared** corners

above: *RD50-MPW2 floorplan. 3 × 3 test matrices for e-TCT are highlighted in red, green, blue and pink and magnified. The central pixel of each structure is then magnified to demonstrate the different corner shapes. Active matrix is highlighted with the orange dashed box*



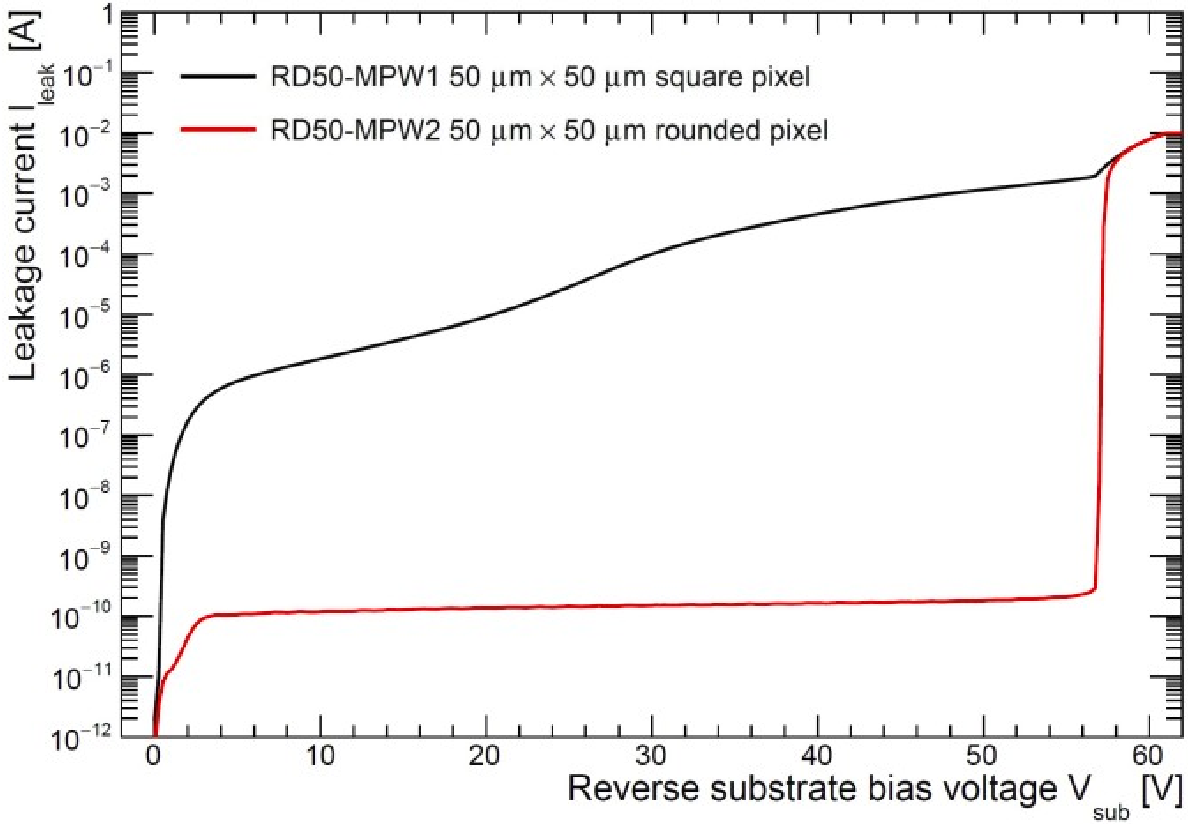
- **Pad connections for I-V:**
  - gnd! = 0 V
  - OUTER = floating
  - INNER = 0 V
  - sub! = -HV



RD50-MPW2 test structure pixel cross section.

RD50-MPW2 test structures measurements: I-V ($\Phi_{eq} = 0$)

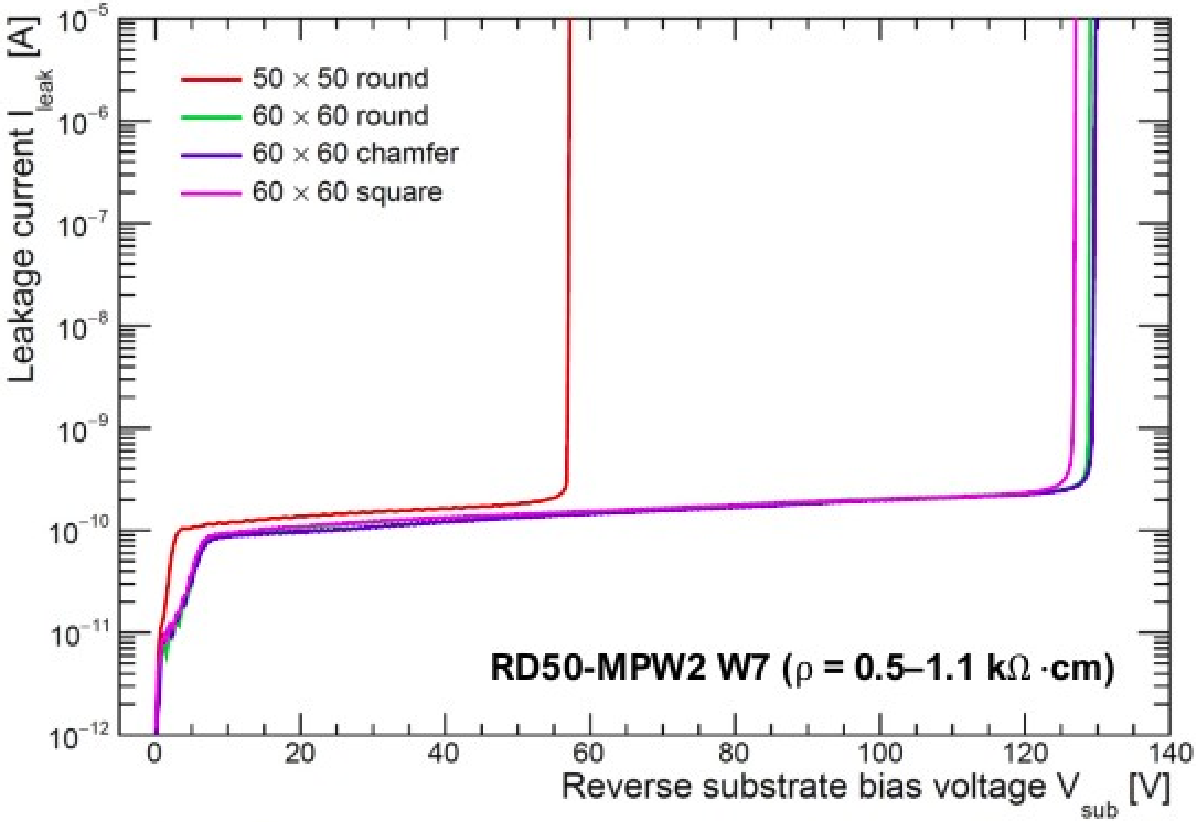
- **RD50-MPW2 comparison with RD50-MPW1: test matrix 1 measurements.**



- **I-V measurements.**
  - ρ = 0.5-1.1 kΩ·cm.
  - 50 μm x 50 μm pixel.
  - 10 mA compliance.
  - T = 20 °C.

- **RD50-MPW2 I_{leak} reduced by many orders of magnitude with respect to MPW1.**

- **RD50-MPW2** measurements of **all test matrices**.



- **I-V measurements.**
  - ρ = 0.5-1.1 kΩ·cm.
  - All pixel types.
  - 10 μA compliance.
  - Same pad connections.
  - T = 20 °C.

- **Similar I_{leak} for all matrices.**
- **RD50-MPW2 V_{BD}.**
  - **Increases** with **electrode spacing.**
  - **Corner shape** can further **increase V_{BD}.**

RD50-MPW2 test structures measurements: I-V ($\Phi_{eq} = 0$)

- **RD50-MPW2** measurements of **all test matrices**: I_{leak} and **breakdown voltage V_{BD}.**

	1st matrix (round 3 µm)			2nd matrix (round 8 µm)			3rd matrix (hexagonal 8 µm)			4th matrix (square 8 µm)		
	Vbd (Icomp)	Vbd (k)	Vbd (ILD)	Vbd (Icomp)	Vbd (k)	Vbd (ILD)	Vbd (Icomp)	Vbd (k)	Vbd (ILD)	Vbd (Icomp)	Vbd (k)	Vbd (ILD)
0.5-1.1 kΩ·cm 8 samples Icomp= 100 nA	57.5 V 1.83 V	55.25 V 2.12 V	55.25 V 2.12 V	120.75 V 5.23 V	119 V 5.45 V	119 V 5.45 V	120.25 V 4.71 V	118.5 V 4.50 V	118.5 V 4.50 V	118.5 V 5.83 V	117.5 V 5.1 V	117.5 V 5.1 V
1.9 kΩ·cm 7 samples Icomp = 100 nA	57.43 V 2.22 V	54.86 V 2.27 V	54.86 V 2.27 V	119.34 V 3.08 V	117.37 V 3.08 V	117.37 V 3.08 V	120.86 V 3.24 V	119.14 V 3.44 V	119.14 V 3.44 V	115.43 V 3.78 V	113.43 V 2.99 V	113.43 V 2.99 V
>2 kΩ·cm 8 samples Icomp = 100 nA	54.75 V 1.83 V	53.25 V 1.03 V	53.25 V 1.03 V	119.5 V 3.5 V	117.5 V 3.5 V	117.5 V 3.5 V	120.75 V 2.12 V	118.75 V 2.12 V	118.75 V 2.12 V	114 V 5.01 V	112 V 5.01 V	112 V 5.01 V
	Mean (upper value) and standard deviation (lower value) of Vbd for the samples measured											

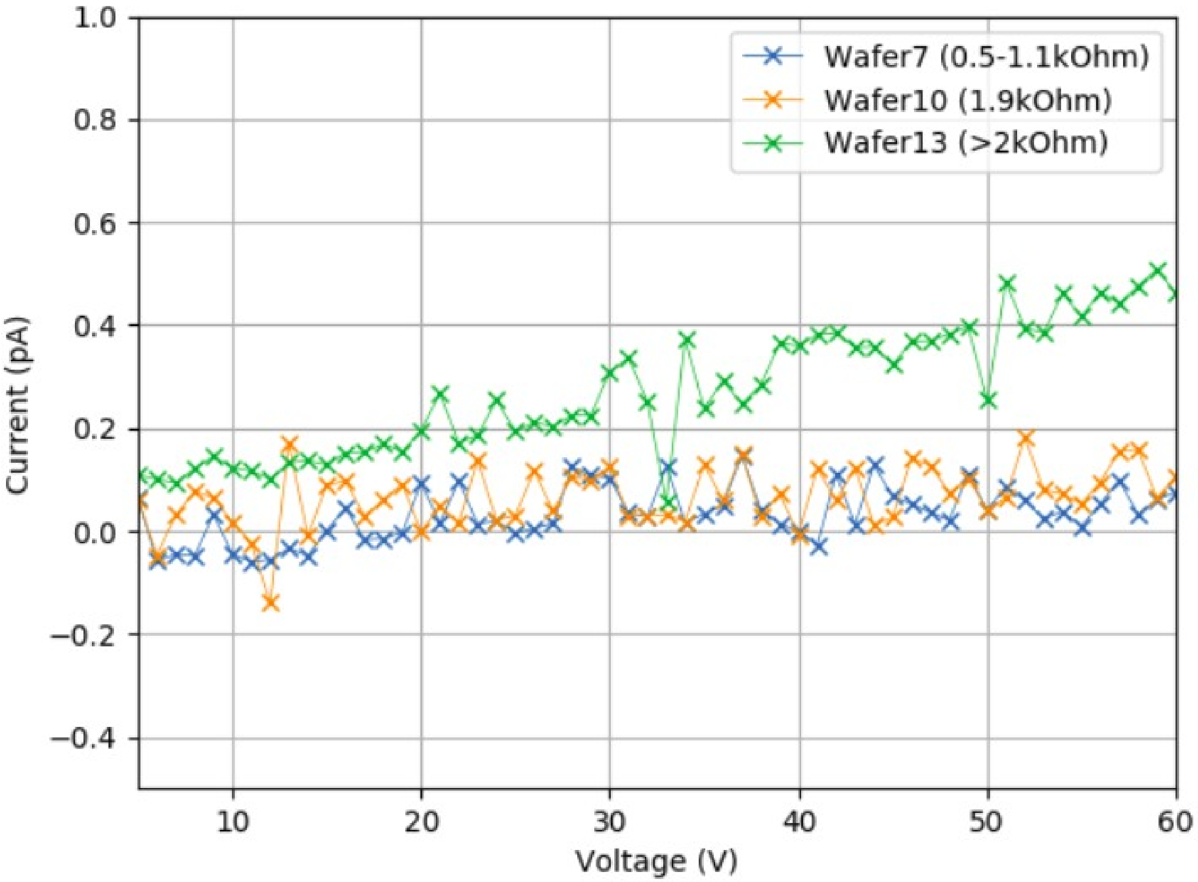
- **I-V measurements.**
  - ρ = 0.5-1.1 kΩ·cm, 1.9 kΩ·cm and > 2 kΩ·cm.
  - All pixel types.
  - 100 nA current compliance
  - Same pad connections.
  - T = 20 °C.

- **Two parameters calulated to determine V_{BD}.**
  - $k = (dI/dV)/(I/V)$
  - $ILD = [d\ln(I)/dV]^{-1} = [(1/I)\cdot(dI/dV)]^{-1}$
- **Vbd (I_{comp}): V for I_{comp}.**
- **Vbd (k): V for maximum k.**
- **Vbd (ILD): V for minimum ILD > 0.**

- **RD50-MPW2 V_{BD} increases with electrode spacing and corner shape can influence as well.**
- **I_{leak} increases with substrate resistivity.**

RD50-MPW2 test structures measurements: I-V (Φ_{eq} = 0)

- **RD50-MPW2 test matrix 2**: precise **leakage current I_{leak}** measurement of **a pixel**.

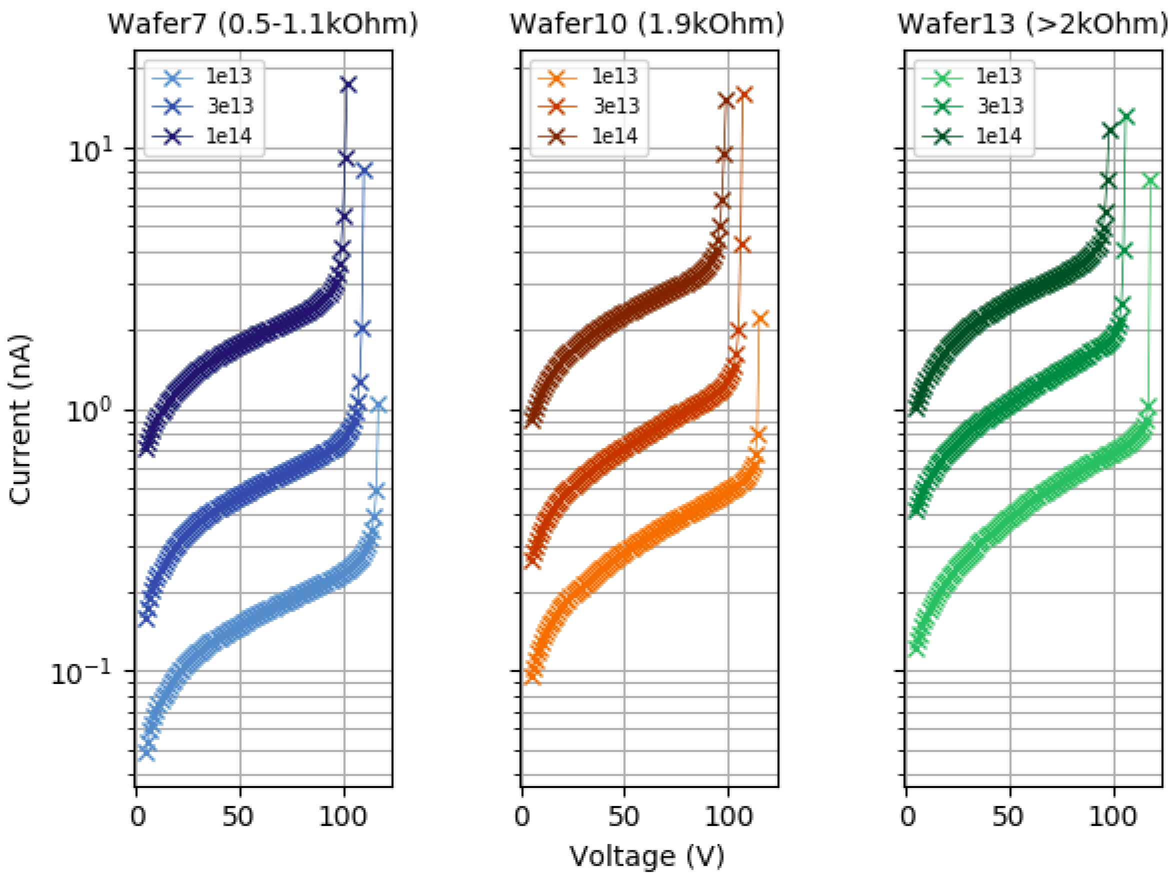


- **I-V measurements.**
  - ρ = 0.5-1.1 kΩ·cm, 1.9 kΩ·cm and > 2 kΩ·cm.
  - Only matrix test matrix 2.
  - T = 20 ˚C.
- **Pad connections.**
  - gnd! = GND.
  - OUTER = GND (guard ring).
  - INNER = GND (through ammeter).
  - sub! = -HV.
- **Current of central DNWELL/p substrate junction is measured using the additional ammeter.**

- **Leakage current I_{leak} below 1 pA.**

RD50-MPW2 test structures measurements: I-V ($\Phi_{eq} > 0$)

- **RD50-MPW2 test matrix 2**: **I-V** in **irradiated devices**.

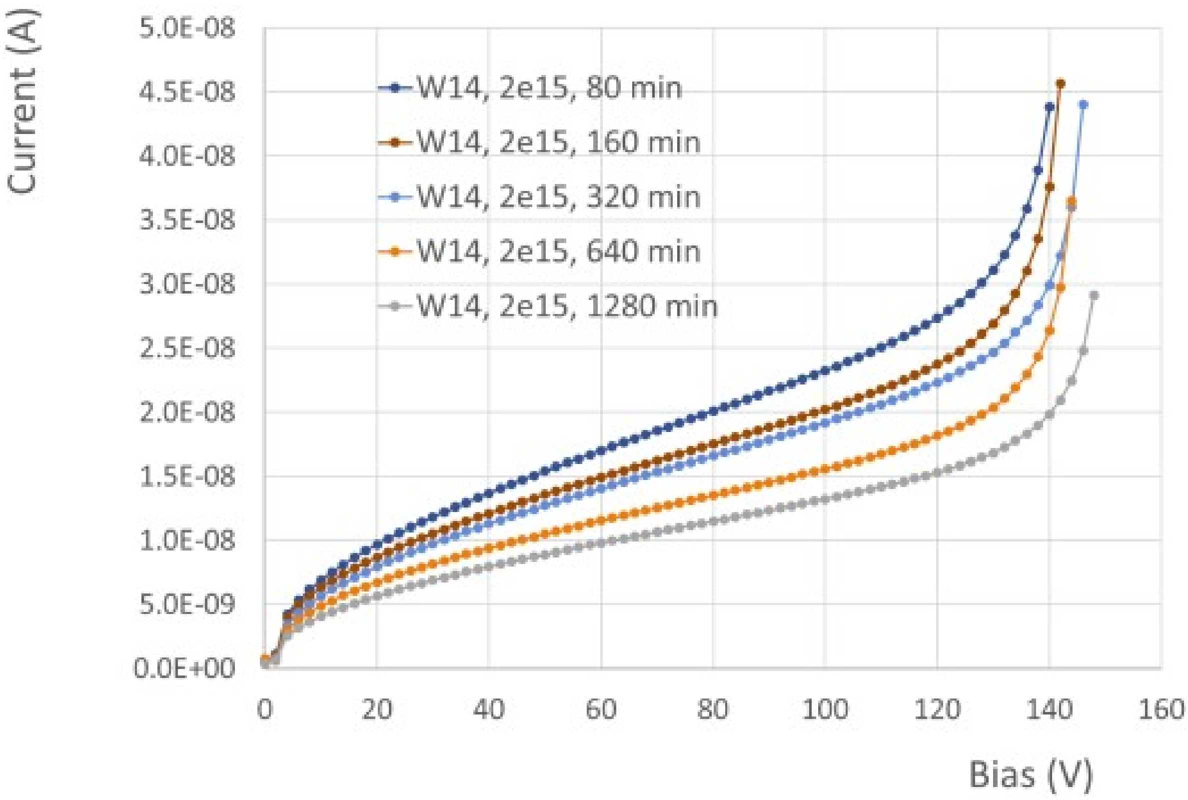


- **Irradiation to a range of neutron equivalent fluences Φ_{eq} up to $1{\cdot}10^{14}$ 1 MeV $n_{eq}{\cdot}cm^{-2}$.**
  - No annealing**.**
- **I-V measurements.**
  - ρ = 0.5-1.1 kΩ·cm, 1.9 kΩ·cm and > 2 kΩ·cm.
  - Only matrix test matrix 2.
  - T = 20 °C.

- **Leakage current I_{leak} increases with Φ_{eq}.**
- **V_{BD} decreases with Φ_{eq} and similar for all ρ.**

RD50-MPW2 test structures measurements: I-V (Φ_{eq} > 0)

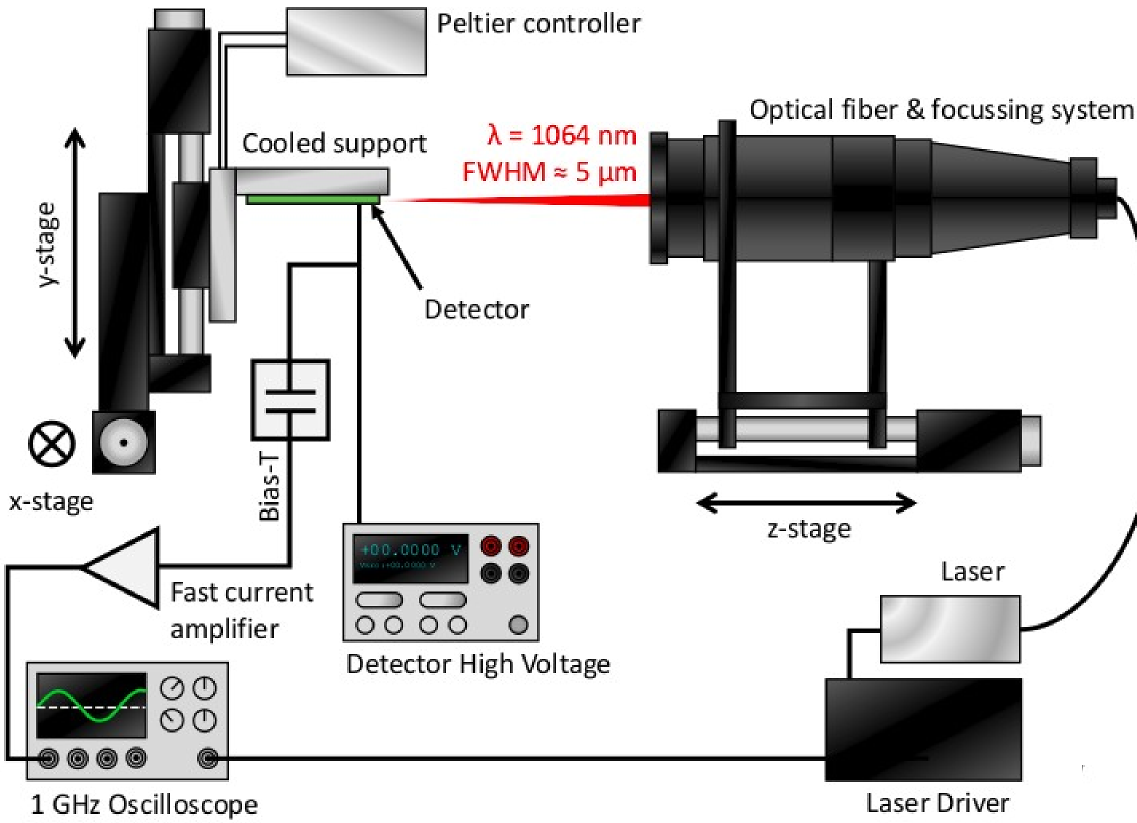
- **RD50-MPW2 test matrix 2**: **I-V** in **irradiated devices**.



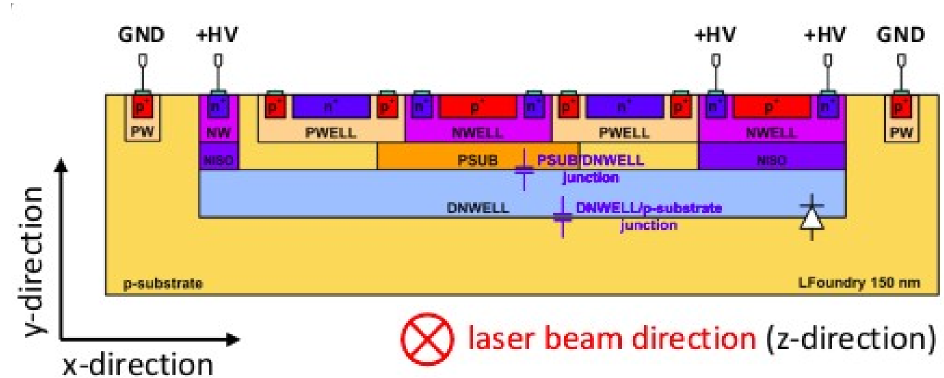
- **Irradiation to a range of neutron equivalent fluence $\Phi_{eq} = 2 \cdot 10^{15}$ 1 MeV $n_{eq} \cdot cm^{-2}$.**
  - Different annealing time steps at 60 °C.
- **I-V measurements.**
  - ρ > 2 kΩ·cm.
  - Only test matrix 2.
  - T = 20 °C.

- **Leakage current I_{leak} decreases with annealing time: current anneals as expected for silicon.**
- **V_{BD} tends to increase with annealing time.**

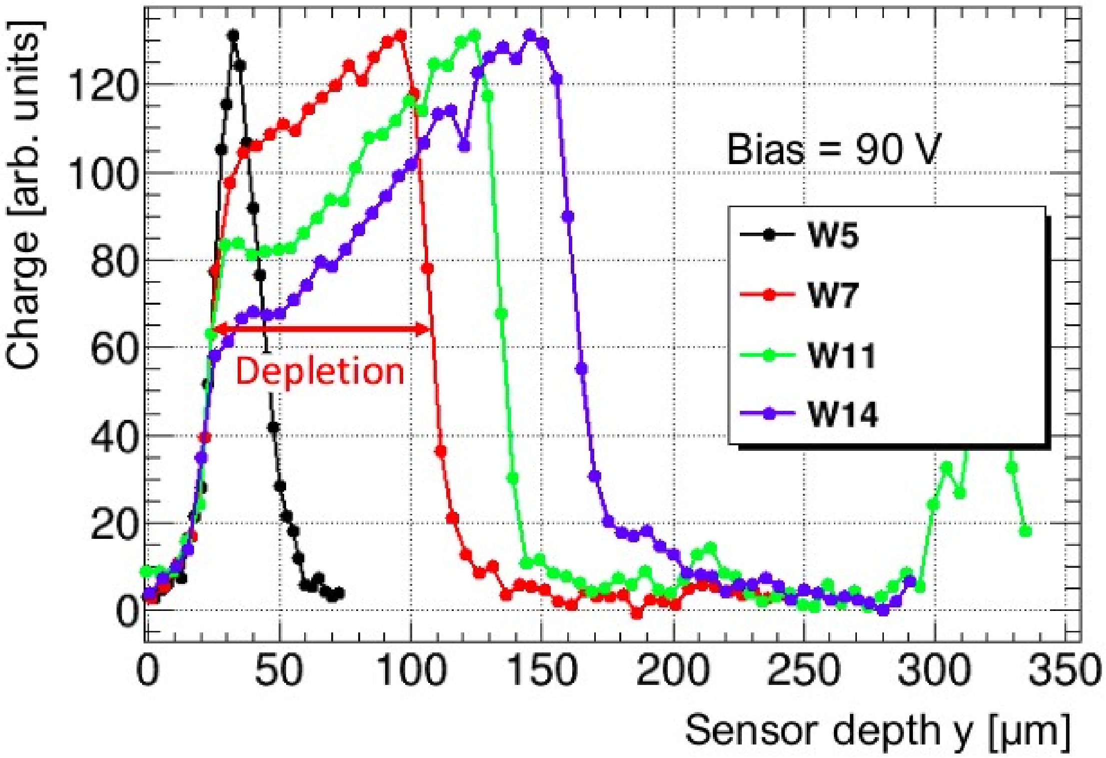
- **RD50-MPW2 e-TCT experimental setup.**



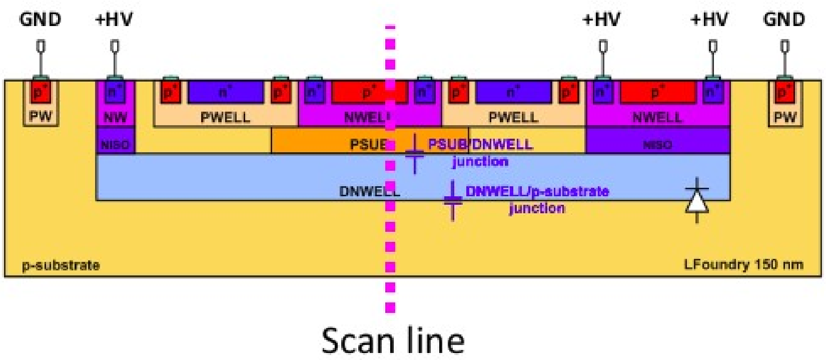
- **e-TCT measurements.**
  - Beam diameter in the silicon FWHM ≈ 5 µm.
  - Width of light pulses ≈ 300 ps and repetition rate 500 Hz.
- **Only test matrix 2.**
- **T = 20 °C.**
- **Connection scheme.**
  - INNER = +HV.
  - sub! = GND.



- **RD50-MPW2 e-TCT measurements**: charge collection profiles.

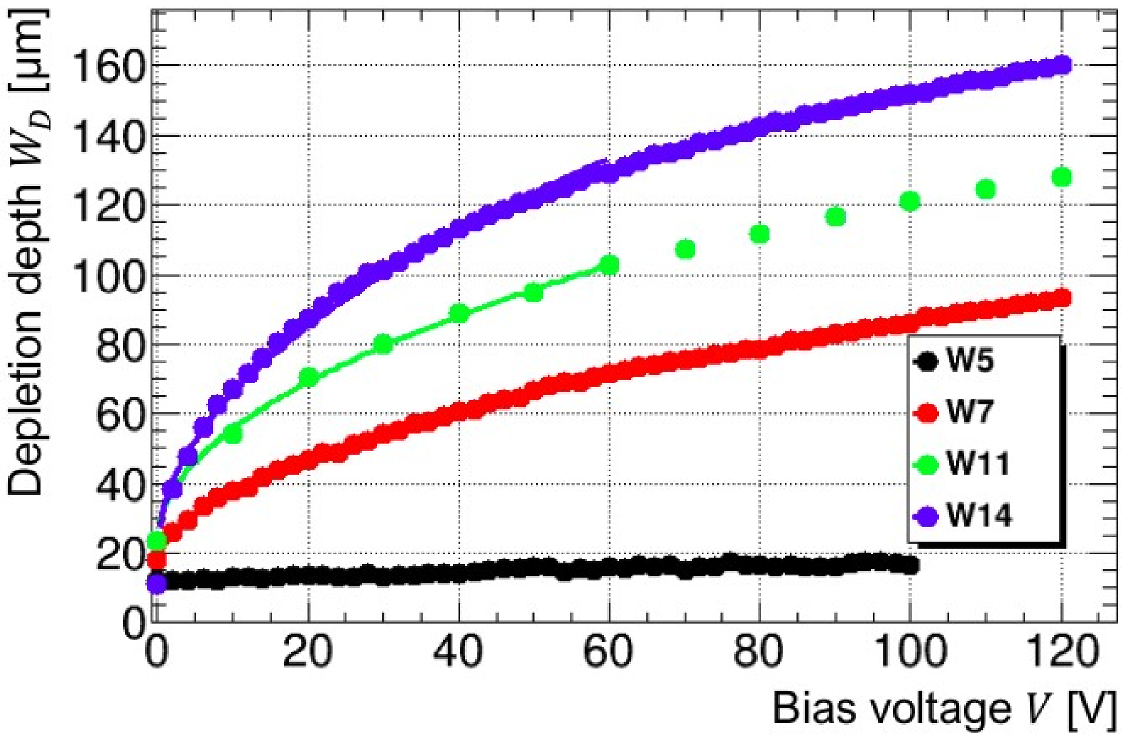


- **e-TCT measurements.**
  - Wafers 5, 7, 11, 14 (10, 500-1100, 1900, >2000 Ω·cm nominal ρ, respectively).
  - Bias up to 120 V
  - (W5 up to 100 V, breakdown at ≈ 105 V).
- **Charge collection profiles.**
  - Scan across of central pixel.
  - Profiles normalized to same maximum.



RD50-MPW2 test structures measurements: e-TCT ($\Phi_{eq} = 0$)

- **RD50-MPW2 e-TCT measurements**: depletion depth W_D and effective doping concentration N_{eff}.



Fit:

$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e_0 N_{eff}} \cdot V}$$

Free parameters:

W_{D_0} = width of charge collection profile at 0 V bias voltage

N_{eff} = effective doping concentration

Constants:

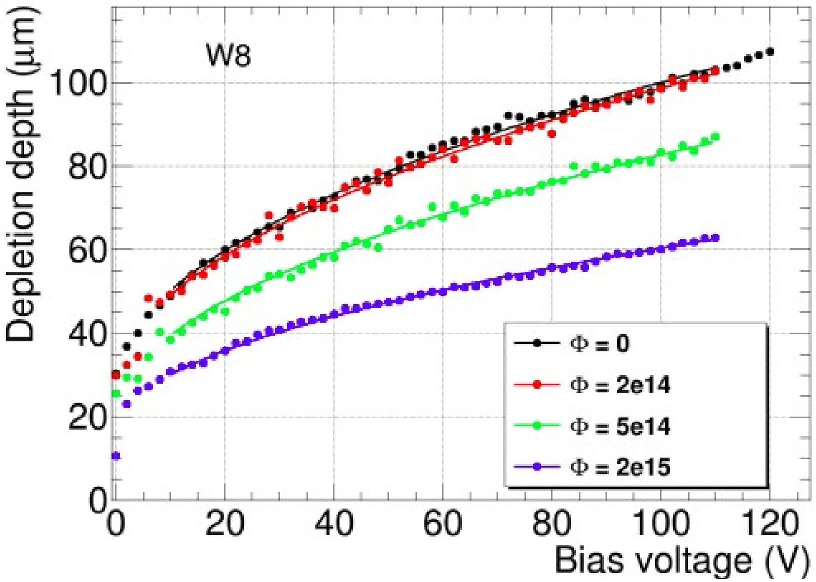
ε_0 = permittivity of free space

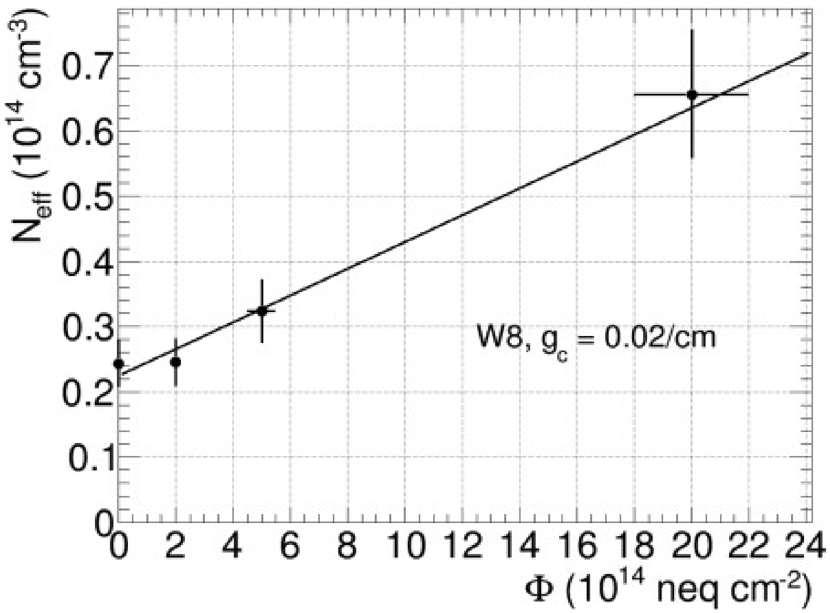
ε_{Si} = relative permittivity of silicon

e_0 = elementary charge

Wafer	N_{eff} [cm^{-3}] ($0 < V < 60$)	ρ [Ω·cm]	Nominal ρ [Ω·cm]
W5	$3.2 \cdot 10^{15}$	4	10
W7	$2.4 \cdot 10^{13}$	500	500-1100
W11	$1.2 \cdot 10^{13}$	1100	1900
W14	$5.9 \cdot 10^{12}$	2200	>2000

- **RD50-MPW2 e-TCT measurements**: **depletion depth W_D** and **effective doping concentration N_{eff}** with **irradiated devices**.





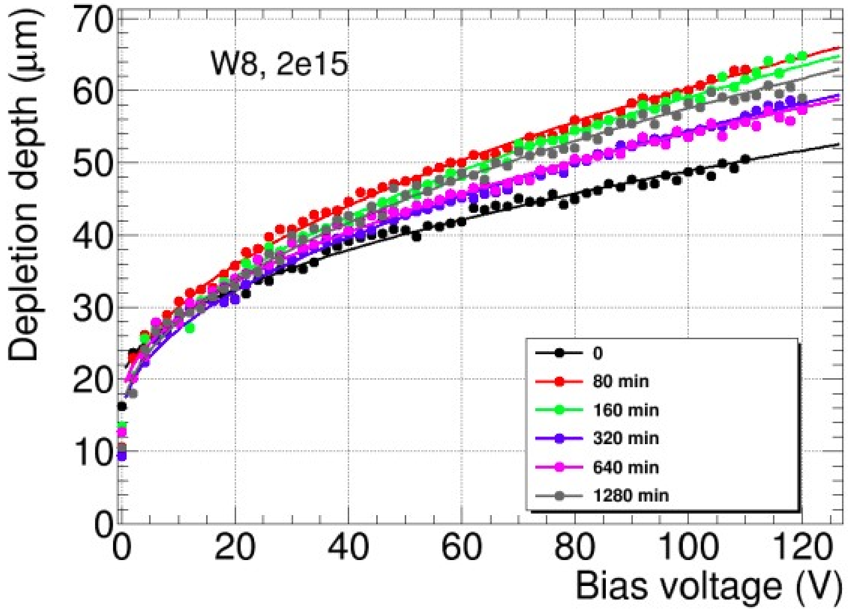
- **Irradiation to a range of neutron equivalent fluences Φ_{eq} up to $2 \cdot 10^{15}$ 1 MeV $n_{eq} \cdot cm^{-2}$.**
  - No annealing**.**
- **e-TCT measurements.**
  - Wafer 8 (0.5-1.1 kΩ·cm nominal ρ).
  - Bias up to 120 V.
- **Neff extracted from fit 0 < V < 120.**

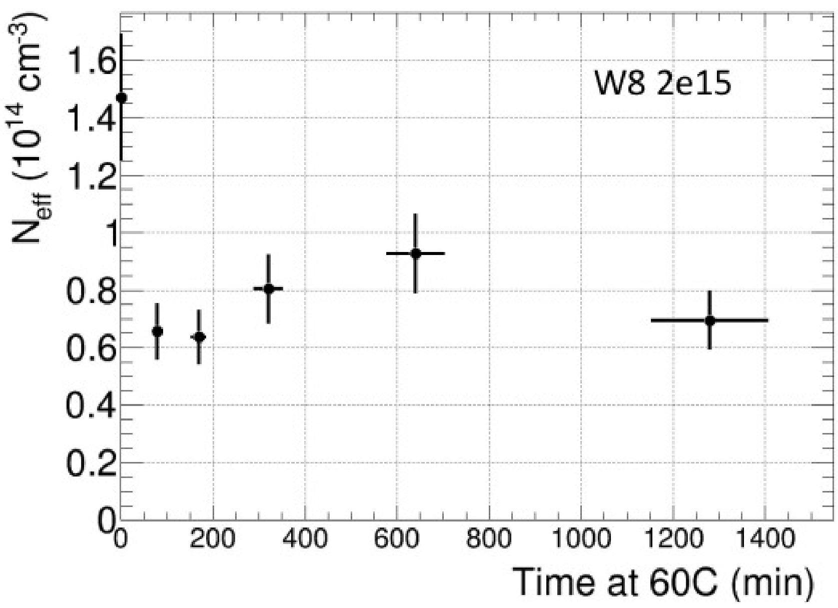
Fit:

$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e_0 N_{eff}} \cdot V}$$

- **N_{eff} increases with fluence.**
  - $N_{eff} = g_c \cdot \Phi_{eq}$.

- **RD50-MPW2 e-TCT measurements**: **depletion depth W_D** and **effective doping concentration N_{eff}** with **irradiated devices**.





- **Irradiation to a range of neutron equivalent fluences Φ_{eq} 2·10 [15] 1 MeV n_{eq}·cm^{-2}.**
  - Different annealing time steps at 60 °C.
- **e-TCT measurements.**
  - Wafer 8 (0.5-1.1 kΩ·cm nominal ρ).
  - Bias up to 120 V.
- **Neff extracted from fit 0 < V < 120.**

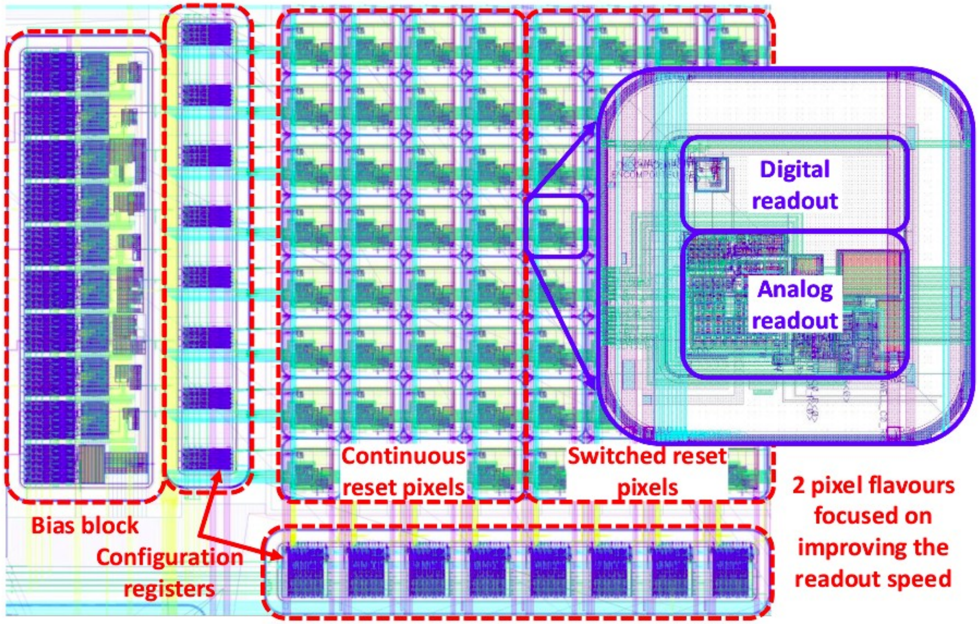
Fit:

$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{Si}\varepsilon_0}{e_0 N_{eff}} \cdot V}$$

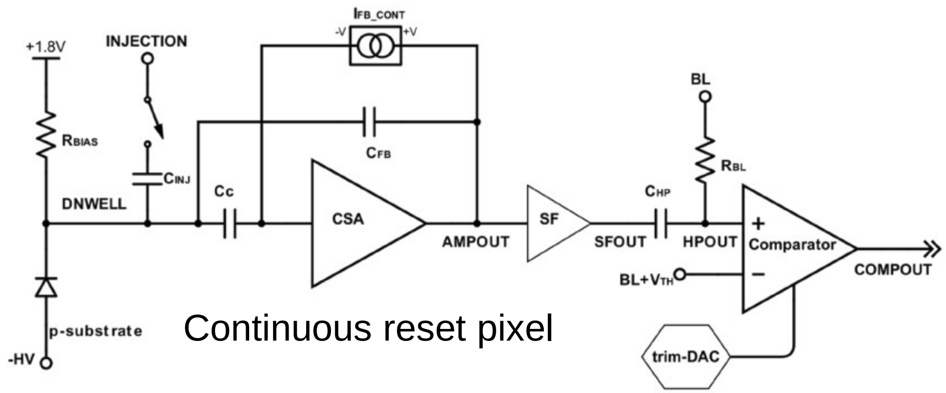
- **Significant effect of the first annealing step (80 minutes).**
- **Not much change after longer annealing times.**

Characterization of RD50-MPW2 active matrix ($\Phi_{eq} = 0$)

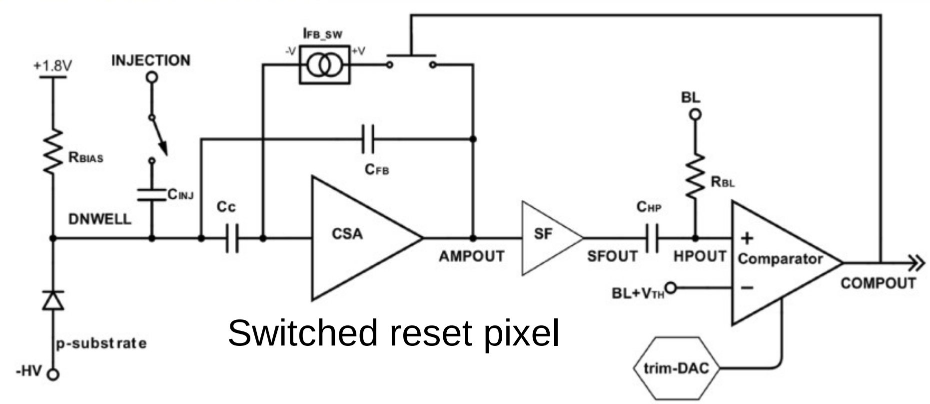
- Matrix of **depleted CMOS pixels (60 µm x 60 µm)** with **analog embedded readout.**
- **Two flavours** of **analog readout.**
  - Columns 0-3**: continuous** reset pixels**.**
  - Columns 4-7**: switched** reset pixels**.**
- **Bias block: generates** the **bias voltages** to set **transistors DC operating points.**
  - 9 channels.
  - 6-bit current DAC and current mirror.
- **Configuration registers: bias block DACs, pixel trim-DACs** and **pixel output enable.**



Active pixel matrix floorplan



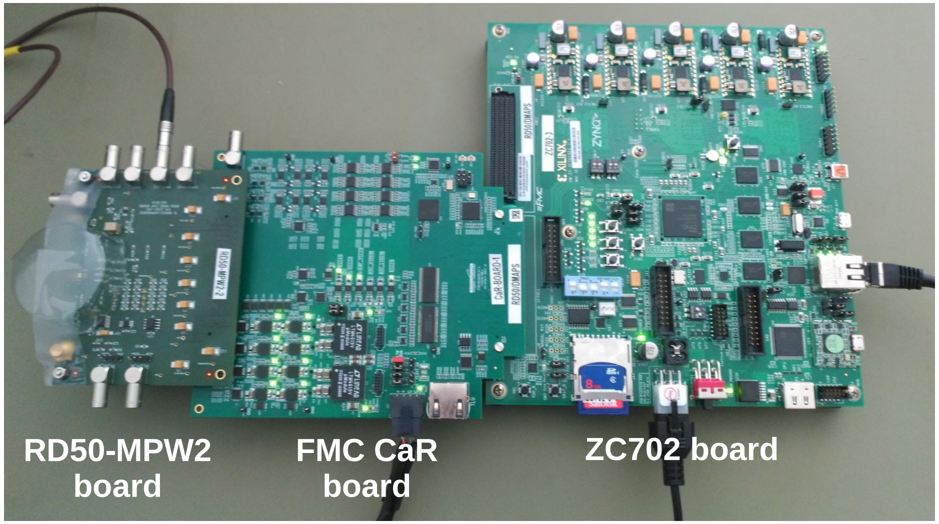
Continuous reset pixel

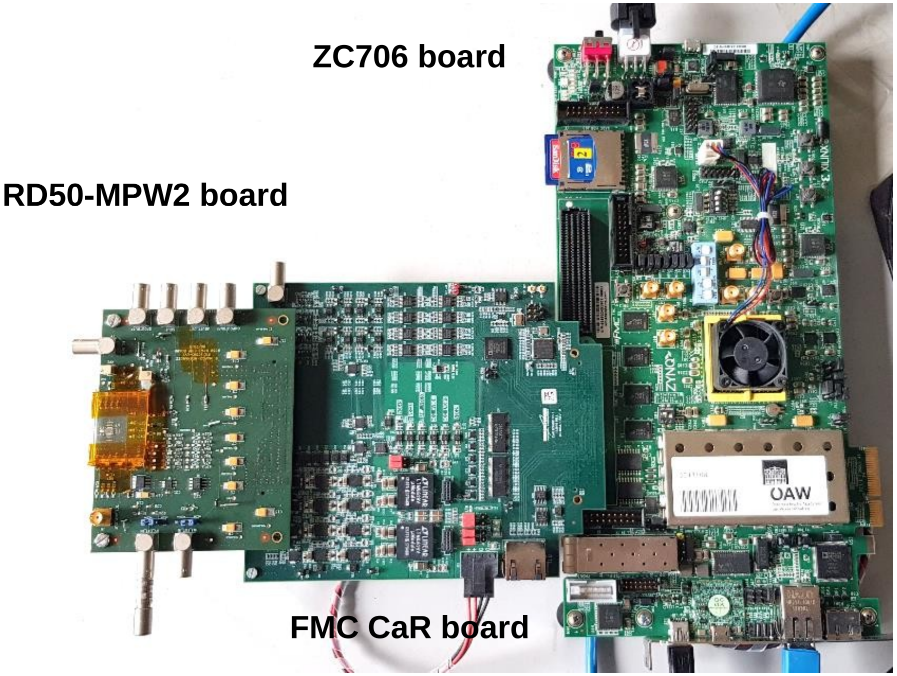


Switched reset pixel

Characterization of RD50-MPW2 active matrix ($\Phi_{eq} = 0$)

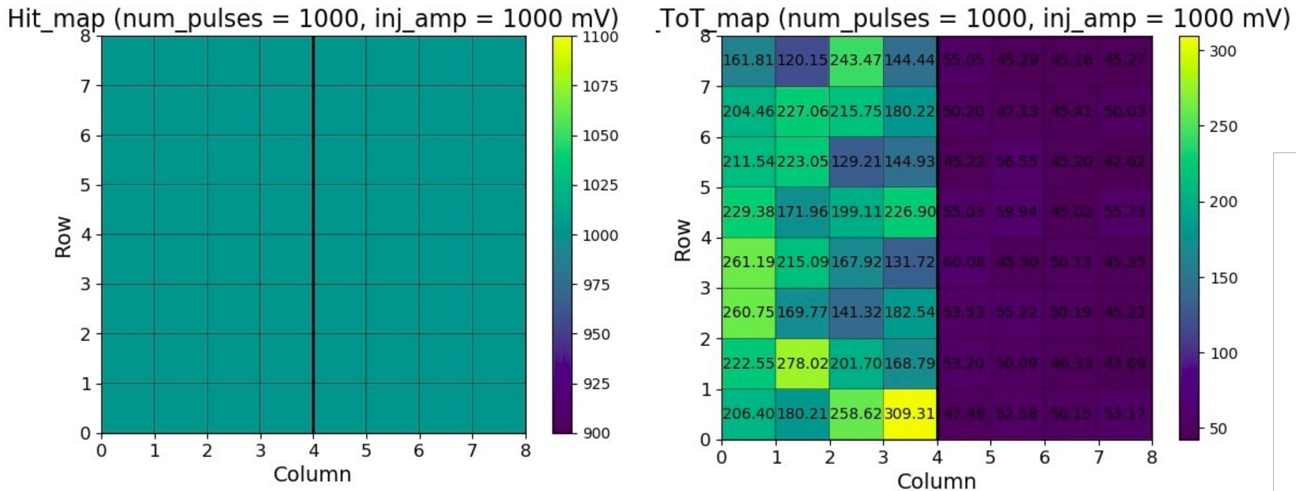
- **Specific DAQs** developed for **RD50-MPW2 active matrix characterization.**
- **SoC development cards** used (Xilinx ZC702/ZC706).
- **FMC CaR board** (from Caribou DAQ).
- **Custom RD50-MPW2 chip board.**
- **Custom VHDL blocks, Linux and C/Python scripts.**
- **SSH from host PC.**
- **Effort** to **converge** with **Caribou Peary firmware/software.**



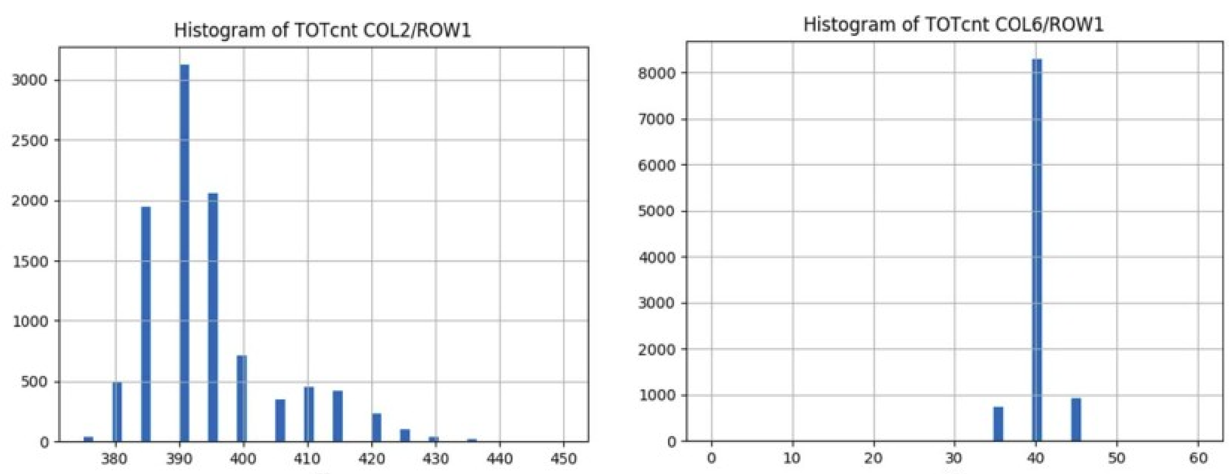


More info: C. Irmler, 36th RD50 Workshop.

- **RD50-MPW2 active matrix measurements** with **in-pixel calibration circuit**: **hitmaps, mean ToT maps** and **ToT histogram for a pixel**.



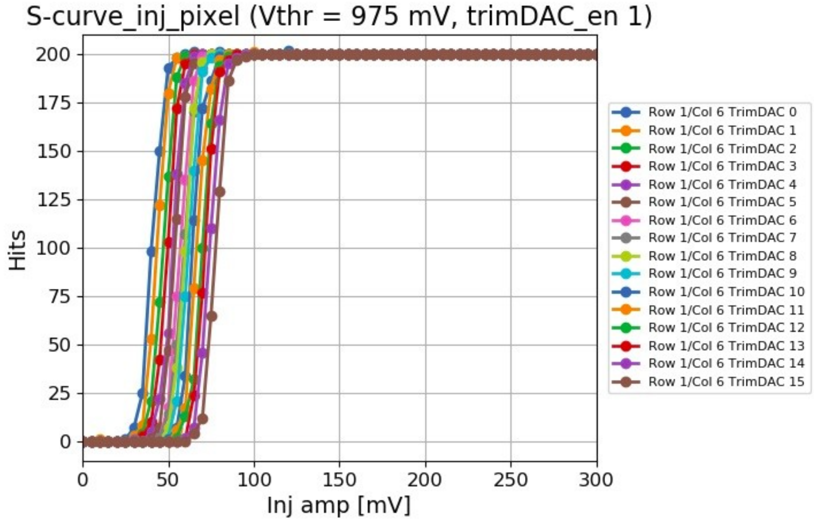
Full matrix hit map (left) and **mean ToT map (right)** for comparator threshold 990 mV. **1000 pulses injected** of amplitude 1000 mV



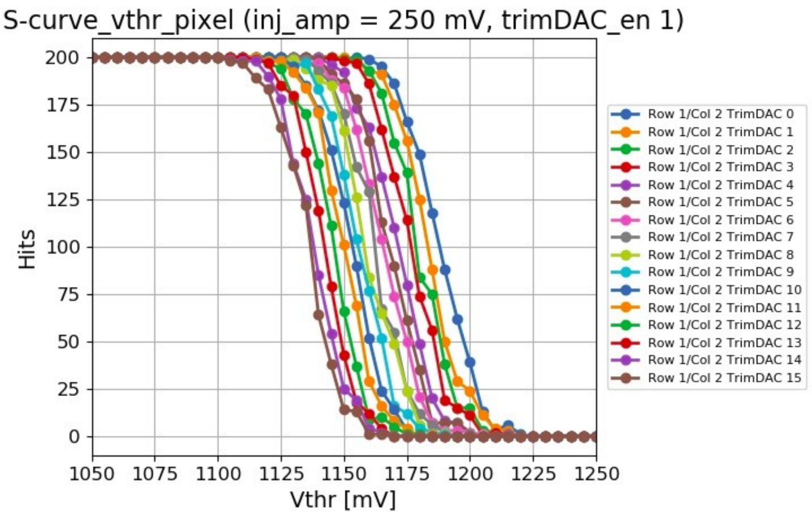
Mean ToT histogram for **CR pixel (left)** and **SR pixel (right)** for comparator threshold 950 mV. **10000 pulses injected** of amplitude 1800 mV

- **Pixel comparator output pulse acquired with DAQ.**
  - Bias registers configured with nominal values.
- **Hitmaps**
  - Number of pulses detected.
- **Mean ToT maps.**
  - Mean pulse width measurement per pixel.
- **ToT histogram for a pixel.**
  - Distribution of pulse width measurement.

- **RD50-MPW2 active matrix measurements** with **in-pixel calibration circuit**: **S-curves.**

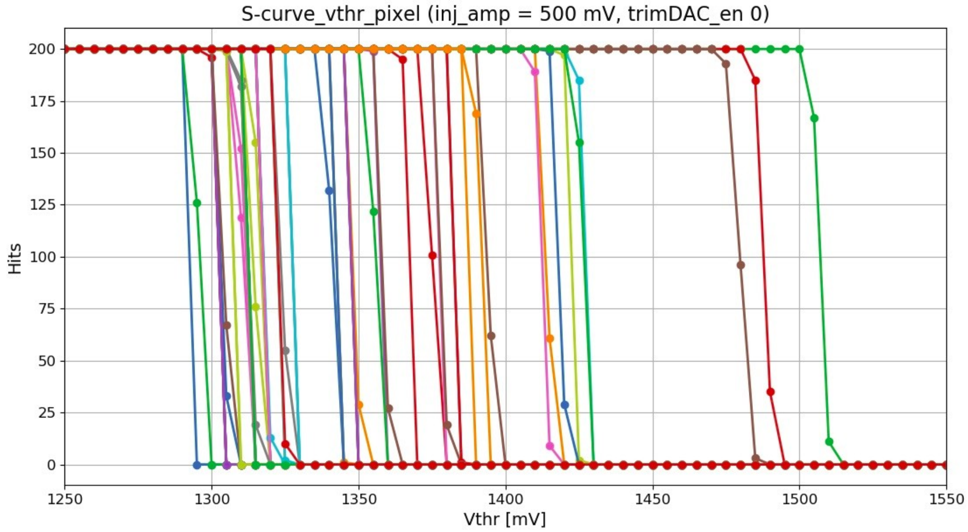


S-curves for **SR pixel** (R1/C6) with **varying injection amplitude** (0-300 mV). Threshold voltage 975 mV and **trim DAC enable (trim DAC value 0-15)**



S-curves for **CR pixel** (R1/C2) with **varying threshold voltage** (1050-1250 mV). Injection amplitude 250 mV and **trim DAC enable (trim DAC value 0-15)**

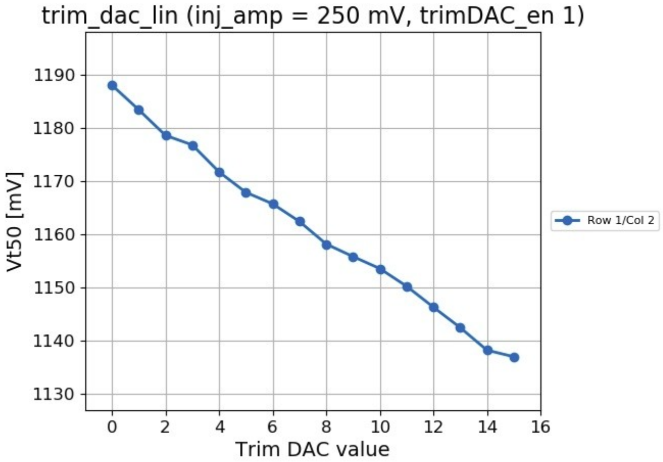
- **S-curves: number of hits as a function of...**
  - Injection amplitude variation.
  - Comparator threshold variation.
  - Also Trim DAC value variation.

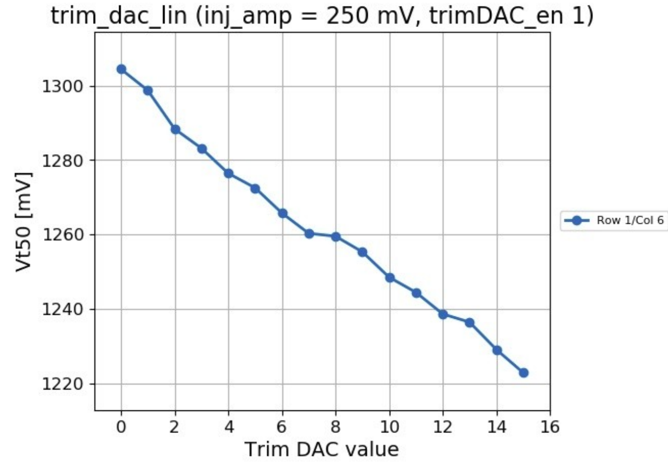


S-curves for **all pixels** with **varying threshold voltage** (1250-1550 mV). Injection amplitude 500 mV and **trim DAC disabled**

Characterization of RD50-MPW2 active matrix (Φ_{eq} = 0)

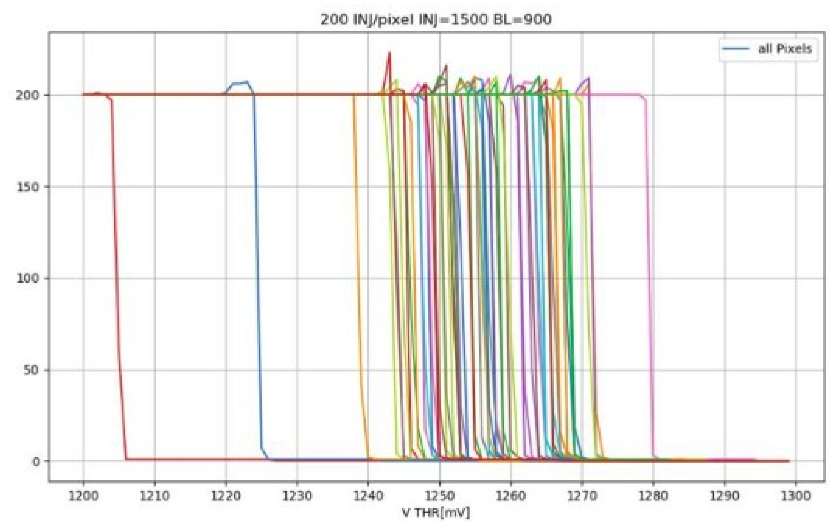
- **RD50-MPW2 active matrix measurements** with **in-pixel calibration circuit**: **S-curves.**





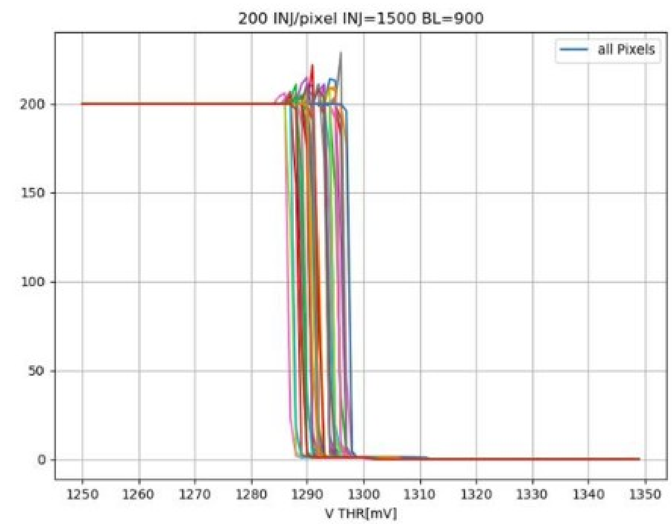
Vt50 (mV) versus trim DAC value for a **CR pixel (left)** and a **SR pixel (right)**. Injection amplitude 250 mV

- **S-curves.**
  - Trim DAC value variation linearity verification: Vt50 vs trim DAC value.
  - Trim DAC value optimization to reduce s-curve width.



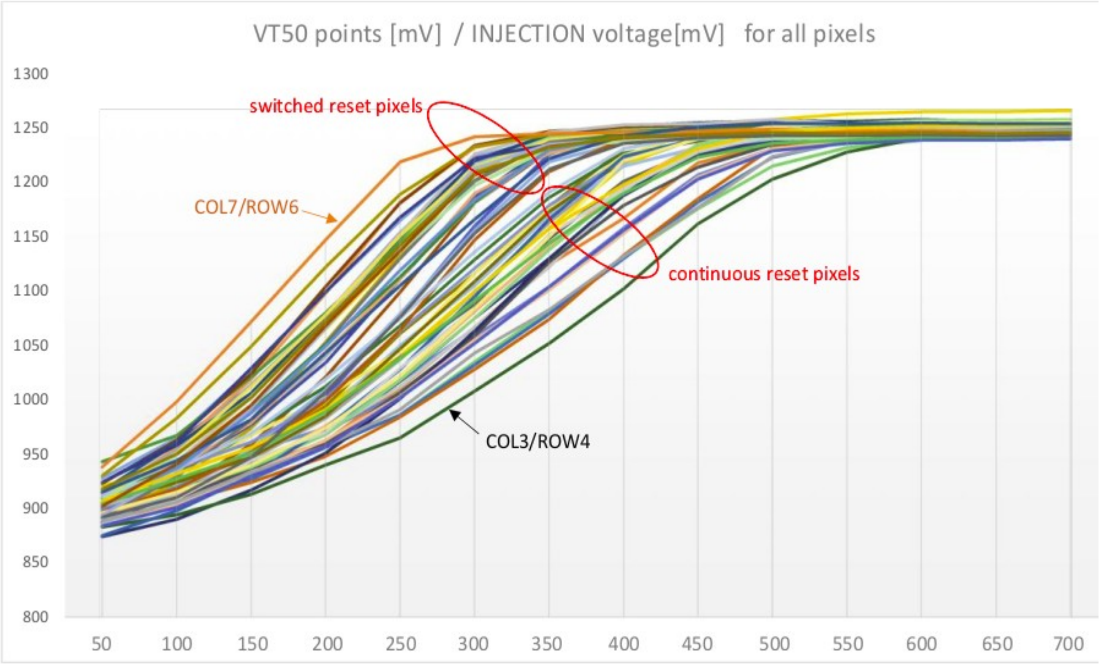
S-curves for **all pixels** with **threshold variation**. **Trim DAC value 15**. Injection amplitude 1500 mV

Trim DAC values optimization



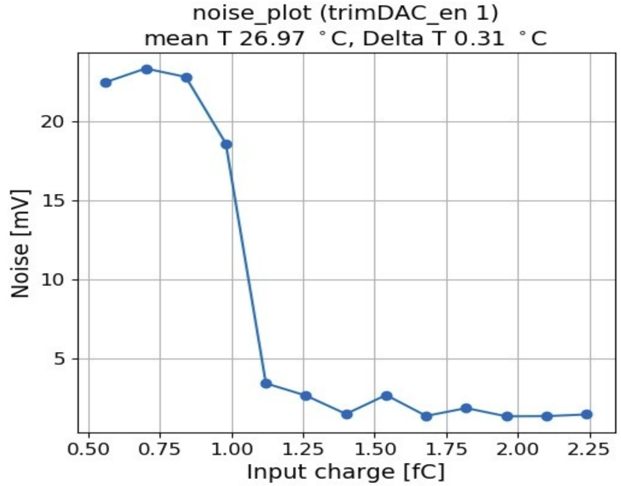
S-curves for **all pixels** with **threshold variation**. **Trim DAC values adjusted**. Injection amplitude 1500 mV

- **RD50-MPW2 active matrix measurements** with **in-pixel calibration circuit**: **gain** and **noise** measurements**.**

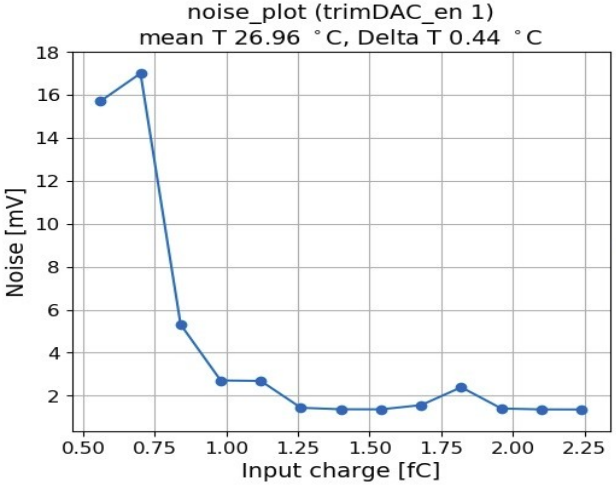


Vt50 (mV) versus injection amplitude (mV) for **all pixels**

- **Gain and noise measurements.**
  - Vt50 value from s-curves versus injection amplitude/charge (1 fC = 357 mV).
  - Vt84 -Vt16 value from s-curves versus injection amplitude/charge.



Noise (mV) versus input charge (fC) for **CR pixel**



Noise (mV) versus input charge (fC) for **SR pixel**

Characterization of RD50-MPW2 active matrix ($\Phi_{eq} = 0$)

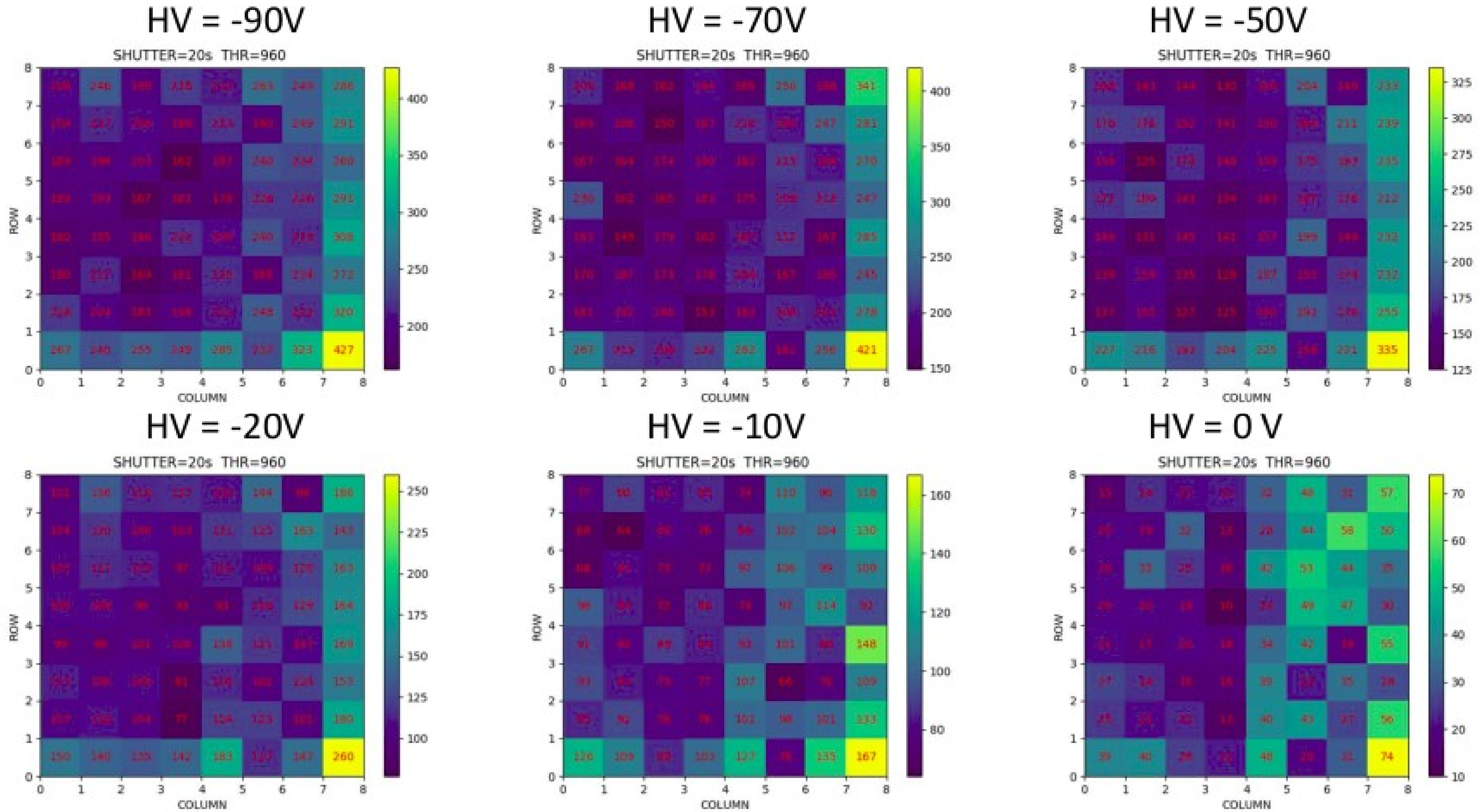
- **RD50-MPW2 active matrix measurements** with **in-pixel calibration circuit**: **gain** measurements **summary.**

	Vienna		Liverpool		Valencia	
	CR	**SR**	**CR**	**SR**	**CR**	**SR**
Bias registers	Nominal values		Nominal values		Nominal values	
BL (mV)	800		900		900	
Linear range (mV)	150-450	150-450	150-400	150-350	150-450	150-450
Linear range[1] (fC)	0.42-1.26	0.42-1.26	0.42-1.12	0.42-1.12	0.42-1.26	0.42-1.26
Gain (mV/mV)	0.9-1.1	1.2-1.4	1.4-1.68	1.96-2.1	1.26-1.4	1.54-1.68
Gain[1] (mV/fC)	321-392	428-500	500-600	700-750	450-500	550-600
[1]Considering C_{inj} 2.8 fF						

- **Values measured at different places with different setups tend to agree.**
- **Baseline value (comparator input DC value) influences the gain measured.**

Characterization of RD50-MPW2 active matrix (Φ_{eq} = 0)

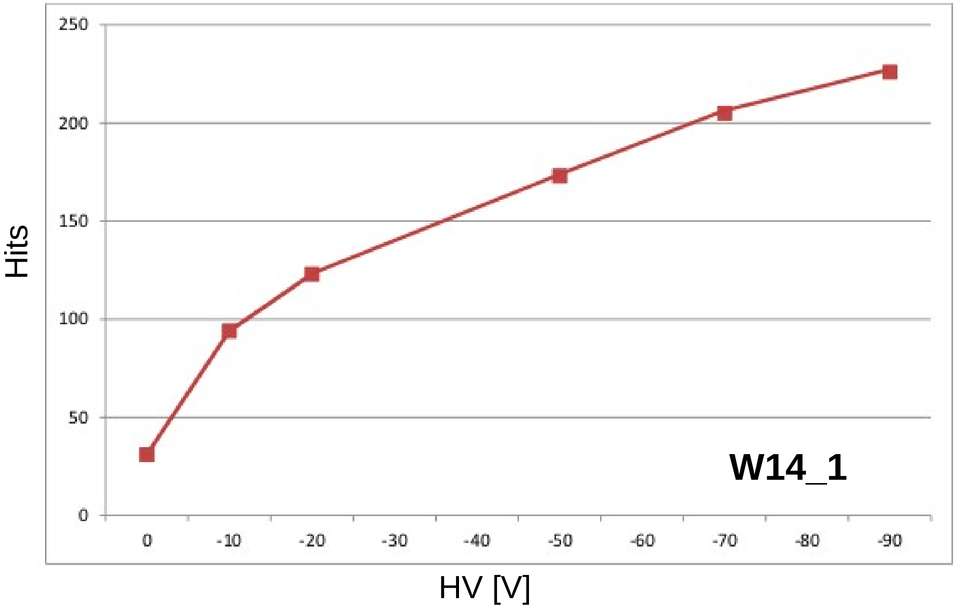
- **RD50-MPW2 active matrix measurements** with **radioactive source**: **hitmaps** for **different HV.**
  - ^{90}Sr source (10 mCi/370 MBq) used.
  - Two RD50-MPW2 samples measured (W14, > 2kΩ·cm).
  - Shutter time per pixel 20 s.
  - Noise trimming process (HV = -50 V): find trim DAC value per pixel to minimize noise.

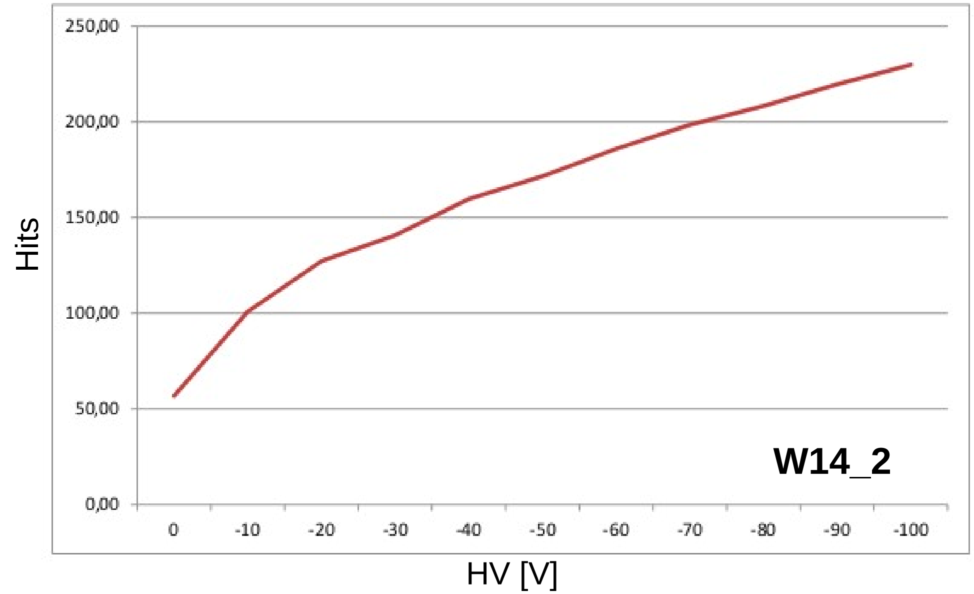


Characterization of RD50-MPW2 active matrix ($\Phi_{eq} = 0$)

- **RD50-MPW2 active matrix measurements** with **radioactive source**: **number of hits mean value** (all pixels) **versus HV**.

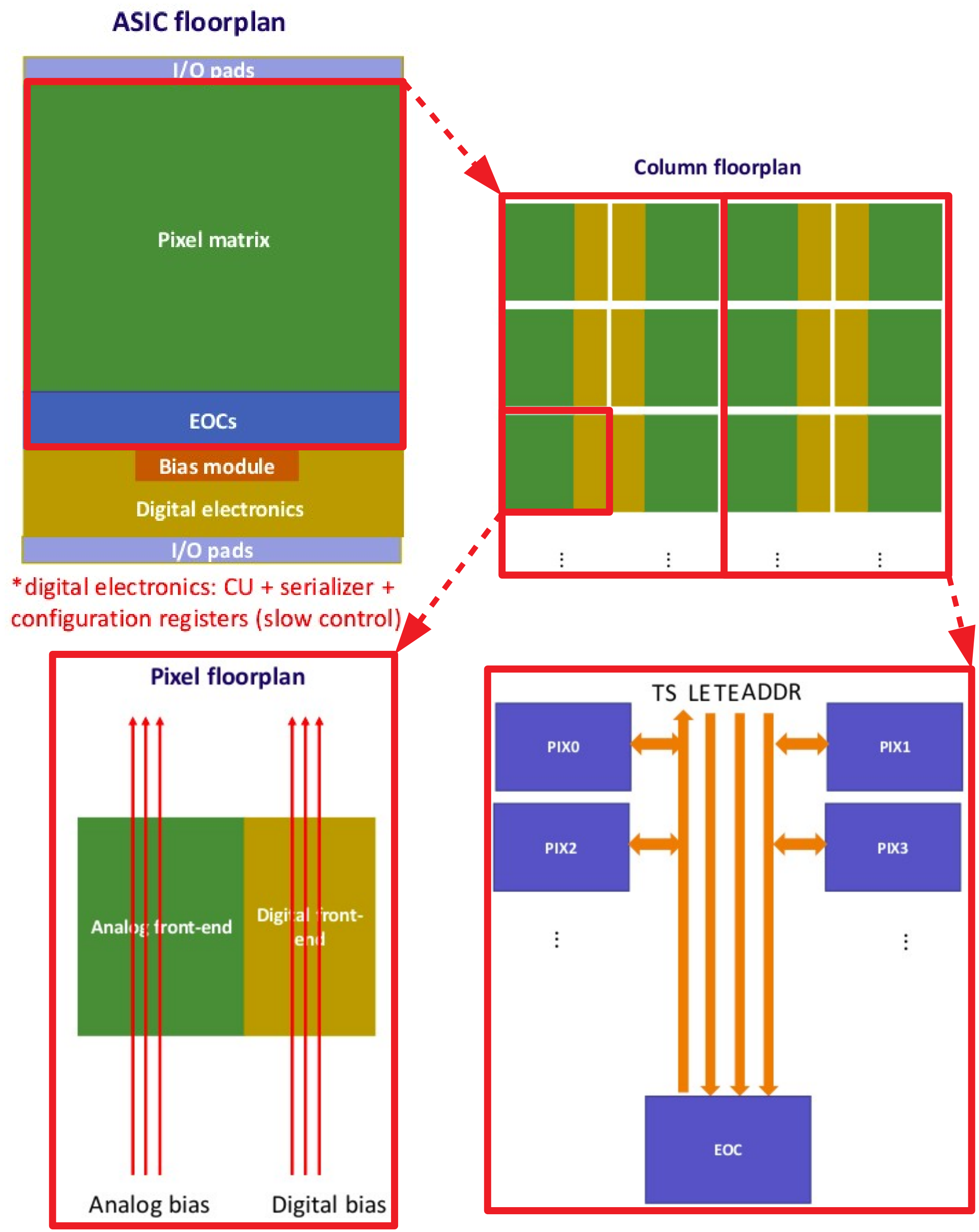
  - ^{90}Sr source (10 mCi/370 MBq) used.
  - Two RD50-MPW2 samples measured (W14, > 2kΩ·cm).
  - Shutter time per pixel 20 s.
  - Noise trimming process (HV = -50 V): find trim DAC value per pixel to minimize noise.





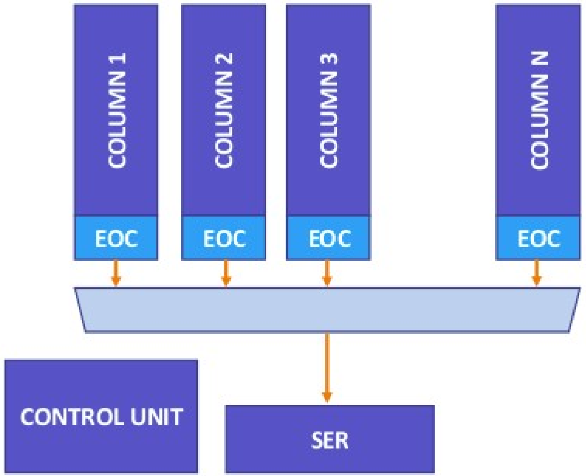
- **Number of hits mean value increases with HV.**

- **General characteristics.**
  - **MPW** in the **150 nm HV-CMOS process** from **LFoundry**: **large collection electrode**.
  - **Size** of **5 mm x 5 mm**. **Thickness** of **280 μm**.
  - Use **few high resistivity substrates**.
  - **Test structures** for **I-V, C-V** and **e-TCT**.
  - At least **one active FE-I3 style pixel matrix**.
  - Maybe **another independent active pixel matrix (sampling matrix)**.
- **Pixel matrix (FE-I3 style).**
  - **Same pixel** and **embedded readout** as in **RD50-MPW2**.
  - **Capability** of **masking noisy pixels**.
  - **Pixel floorpan** with **separated analog** and **digital bias**.
  - **Double columns** with **shared digital signals** to **reduce routing congestion** and **crosstalk.**

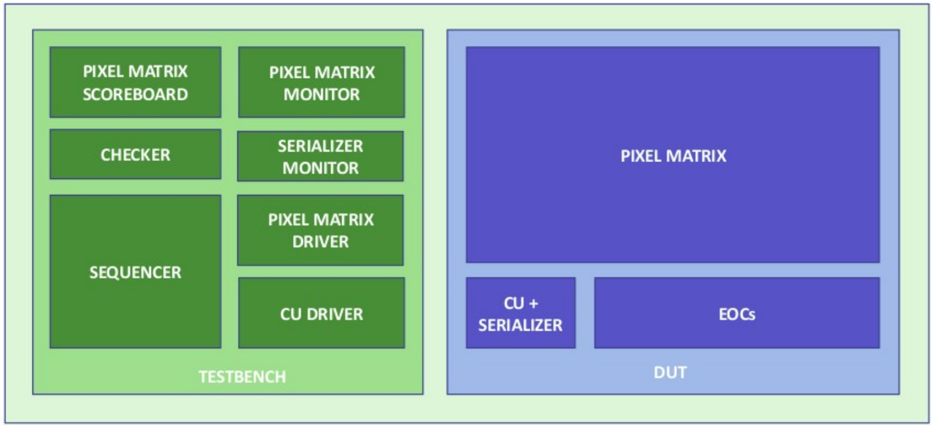


RD50-MPW3 design overview

- **Chip periphery.**
  - **Improved FE-I3 readout** to **optimize data TX**: **time slot only** given to **columns with data**.
  - **Two EOC architectures** to be **considered** (FSM + 24b register or FSM + FIFO) to **reduce pixel dead time**.
  - Only **one serial TX channel (LVDS)**.
  - **Data TX** in **frames**: **SOF+ADDR+LE+TE+EOF**.
  - **Possibility** of **encoding** to **keep sync** (8b/10b) + **idle pattern** + **non return to zero** to be **studied**.
  - **Slow control** for **pixel configuration** and **bias registers** based on **I2C** and **Wishbone**.
- **Chip development.**
  - **Digital-on-top** implementation to **guarantee timing**.
  - **RTL functional model** of **pixel**, **pixel matrix** and **periphery electronics (EOC 1/2)**: **simulation** of **different scenarios**.
  - **Pixel** treated as **an IP**: **generation** of a **timing library**.
  - **Post-layout simulation** of **double column and EOC**.
  - **Functional verification** of **digital part** in **FPGA**.



FE-I3 style digital readout block diagram



Functional verification block diagram

Summary and outlook

- **Summary.**
  - **RD50-MPW2 I_{leak} reduced** by **various orders of magnitude** with respect to **RD50-MPW1.**
  - **RD50-MPW2 V_{BD} increased** with respect to **RD50-MPW1**.
  - **RD50-MPW2 e-TCT** and **I-V measurements** of **irradiated devices show good device performance**.
  - **RD50-MPW2 active matrix configuration** and **readout electronics tested** for **non-irradiated devices** with **good results**.
  - **RD50-MPW3 design ongoing** with **RD50-MPW2 pixel design** and **improved FE-I3 digital readout style**.
- **Outlook.**
  - **RD50-MPW2 C-V measurements** with test structures.
  - **RD50-MPW2 active matrix characterization** of **irradiated devices**.
  - **RD50-MPW3 chip design** and **submission**.

Latest depleted CMOS sensors developments in the CERN RD50 collaboration

Ricardo Marco Hernández IFIC (CSIC-UV),
on behalf of the CERN RD50 collaboration.