Calorimetry Activities in Spain for CALICE and ILC

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CIEMAT, IFIC

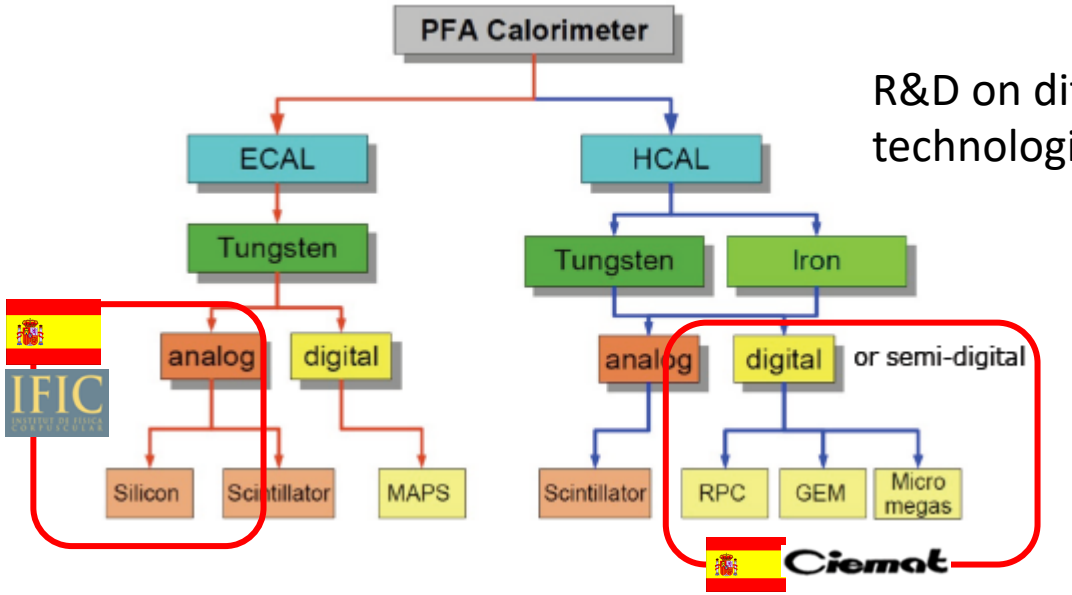
Meeting of the Spanish network for future colliders. 6-7 October 2020

CALICE Collaboration & Spanish groups

The CALICE Collaboration

Developing highly granular calorimetry optimised for particle flow event reconstruction for future energy-frontier electron-positron coliiders

336 physicists/engineers from 57 institutes and 17 countries coming from the 4 regions (Africa, America, Asia and Europe)



R&D on different technologies

Spanish Groups participation

CIEMAT joined in 2007

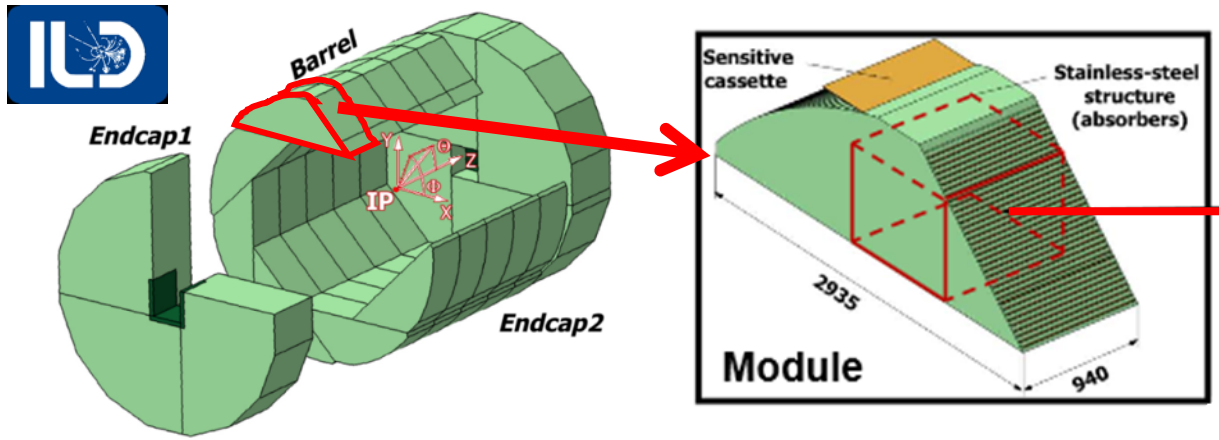
Mainly working in the ***SDHCAL***
(SemiDigital Hadron CALorimeter)

IFIC joined in 2020

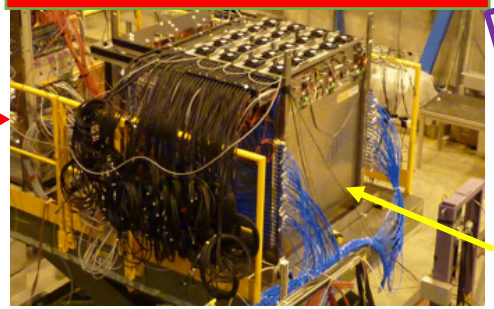
Mainly working in the ***SiW-ECAL***
(Silicon Electromagnetic CALorimeter)

SDHCAL Prototypes

The SDHCAL-GRPC is one of the two HCAL options based on PFA and proposed for **ILD of ILC**.
Modules are made of **GRPC** (**G**lass **R**esistive **P**late **C**hambers) equipped with **semi-digital, power-pulsed electronics** readout and placed in **self-supporting mechanical** structure to serve as absorber as well.



SDHCAL 1.3m^3 prototype



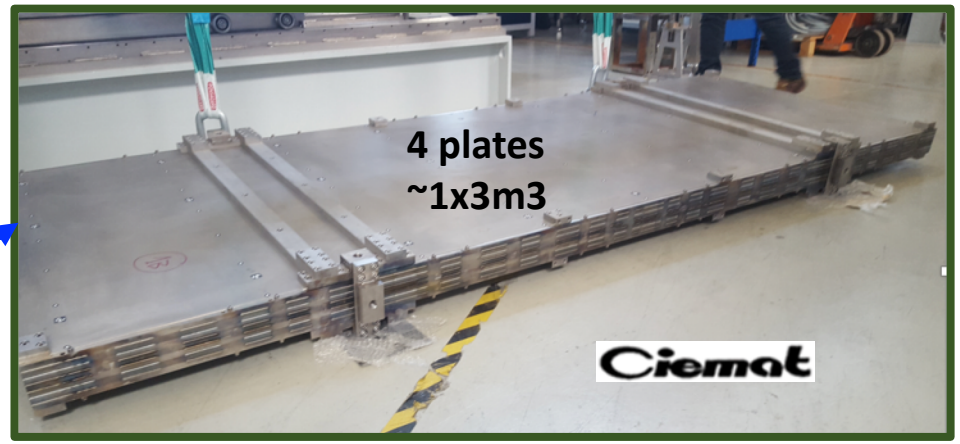
HIGH GRANULARITY CALORIMETER

~ half million of channels

New SDHCAL prototype

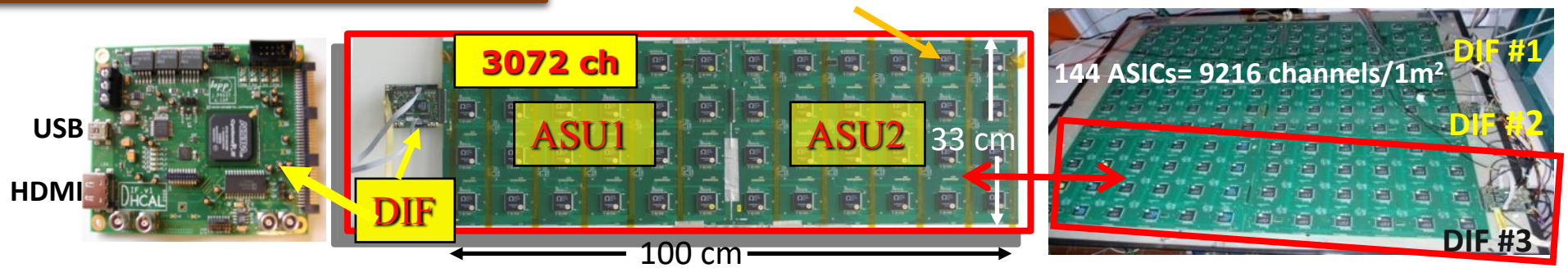
A mechanical structure of 4 plates of ~1x3m^2 (assembled with similar procedures to the final one) where inserting large ***RPCs equipped with a new improved electronics.***

Mechanical structure (calorimeter absorber) done by CIEMAT by using Electron Beam Welding for the assembly



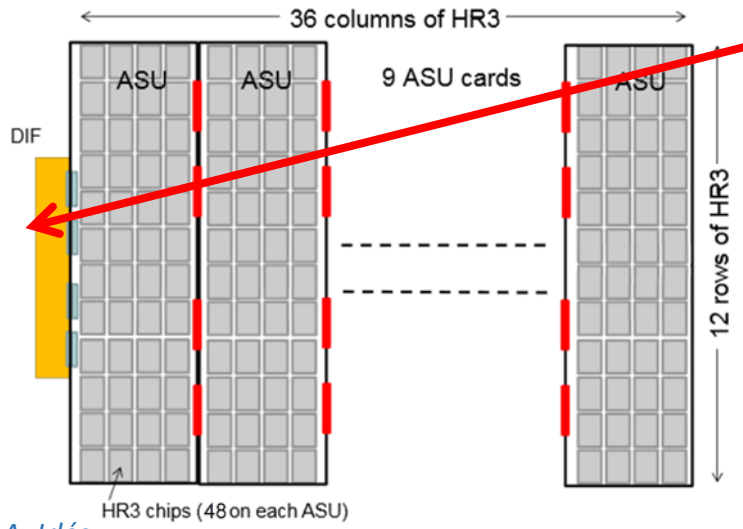
New SDHCAL electronics: ASIC,PCB,DIF

Electronics readout for the 1m³ prototype



1 DIF for 2 ASU (Active Sensor Unit.- PCB+ASICs) ➔ **3 DIFs for ONE 1m2 GRPC detector**

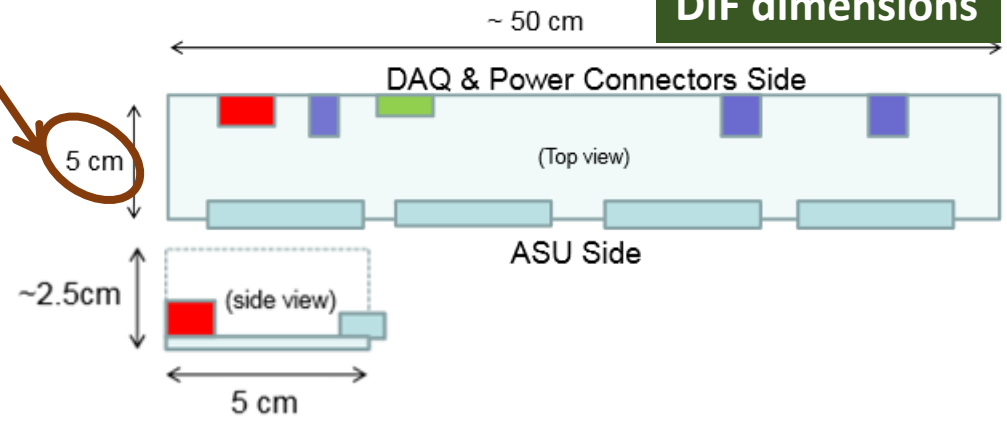
Electronics readout for the final detector



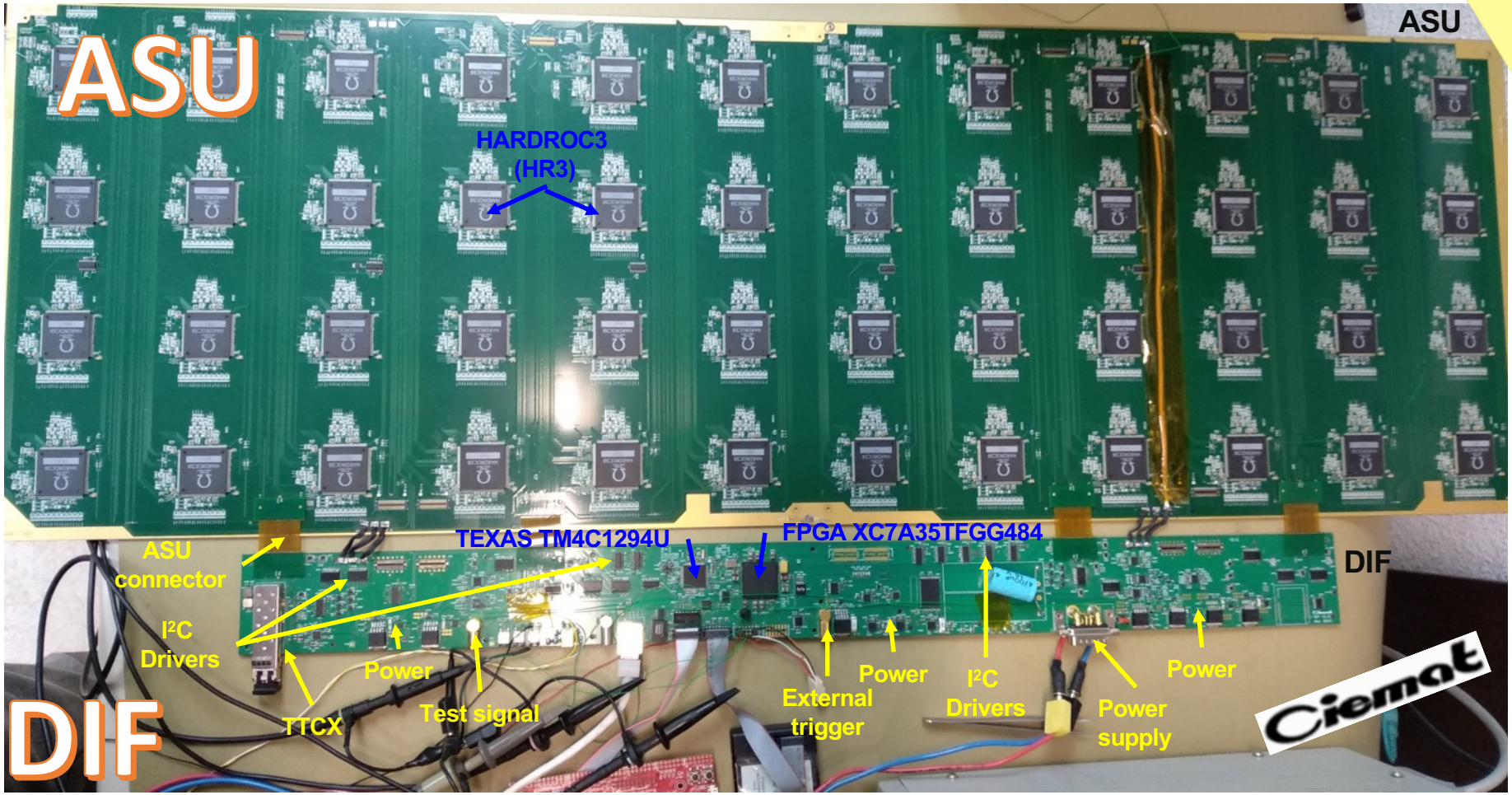
Only **1 DIF per GRPC (any dimension)** with small dimensions to fit in the **small** space available at the final detector

Ciemat

DIF dimensions



SDHCAL DIF+ASU under tests



4 DIFs
Fully assembled and operational

Most of tests done

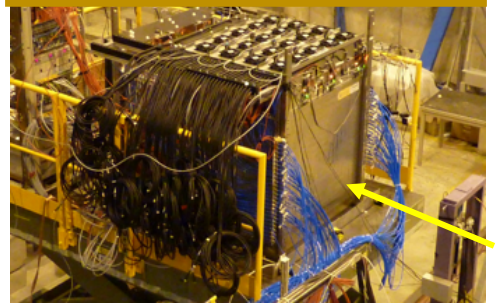
Main pending work:

Integration with DAQ

Under development at Lyon

Test beam data analysis ongoing

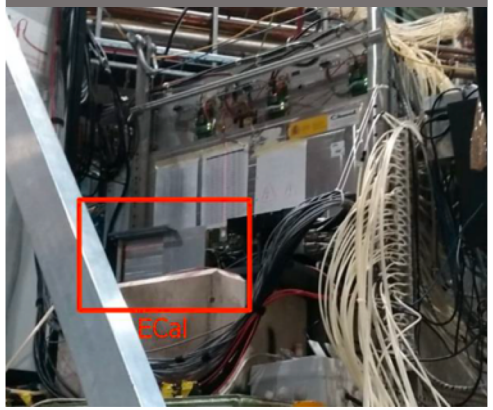
SDHCAL 1.3m^3 prototype



Lot of data taken in the past at SPS Test Beam facilities allowed to validate the technology. But there is still some pending data analysis, as the angular effects studies, started this year under CIEMAT responsibility

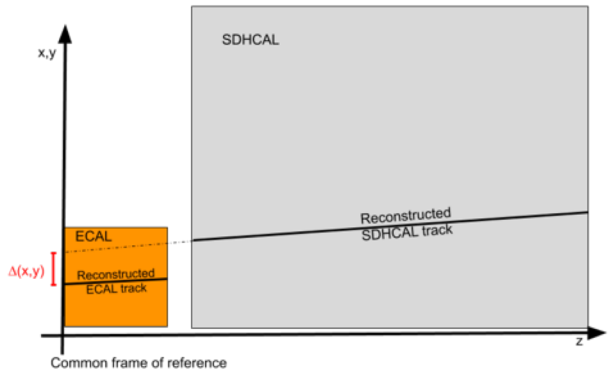
Analysis is ongoing
Not public results yet

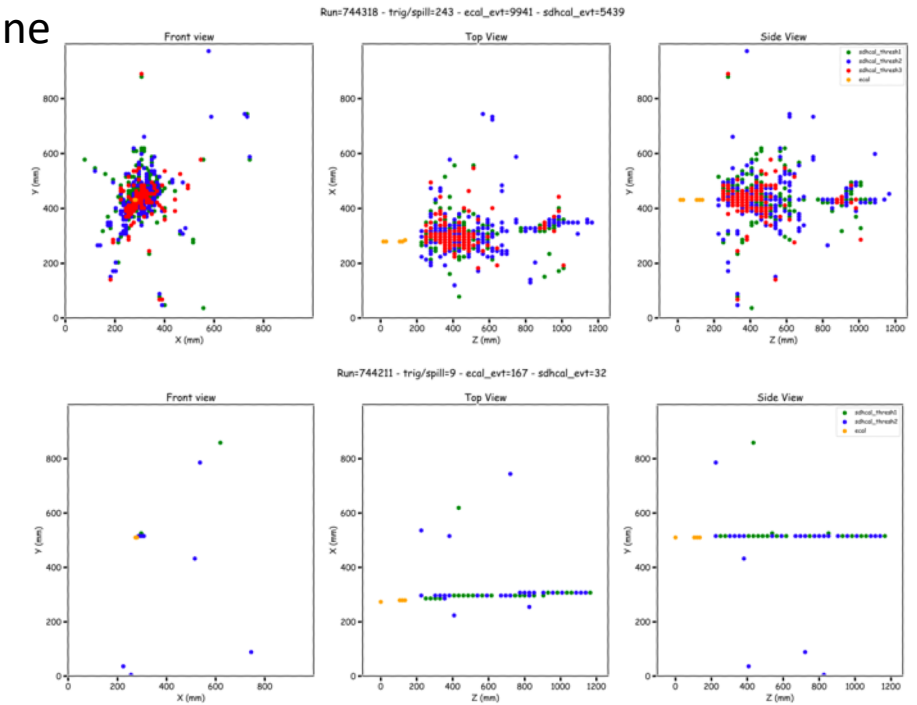
SiW-ECAL + SDHCAL Common tests



2 DAQ systems ➔ Event synchronization done offline

Alignment between both prototypes needed
Using tracks of muons





ILD software/physics studies & other CALICE plans at CIEMAT

- Working on a procedure (and software program) for ***validating SDHCAL Monte Carlo ILD releases/production in the framework of ILCSoft***

  Well advanced since beginning of the year, a standalone program already available and being tested already presented to the ILD.

- ***Montecarlo*** studies of ***using the time information*** given for the calorimeter (***5D readout***) in the event identification and reconstruction

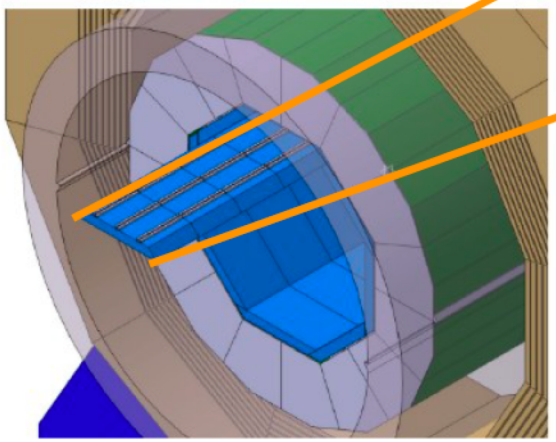
  Some studies started by our Lyon's colleagues, interested on join this efforts

- Some **Higgs studies** in our ***long term plan. (just starting to look the ILD MC code in depth)***

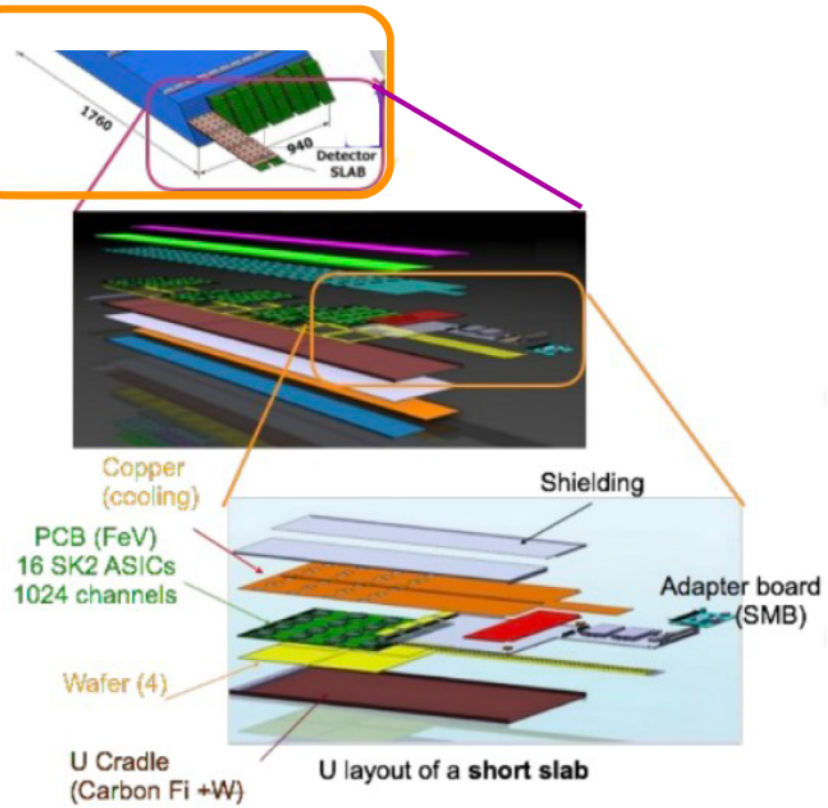
  Plan to start to study first the **W decays on jets** using the **SDHCAL option reconstruction** (most of ILD physics studies uses the Analog DHCAL – based on scintillator tiles)

- Plans to participate in the **new SiW-ECAL prototype commissioning and test beam**. But problems because of the covid-19. A PhD student started to work in the commissioning at Paris in March was forced to come back to Madrid after couple of weeks, we still plan to participate on the DESY test beam, if possible (end of November), but it will depend on thee covid-19 situation in Madrid, Paris and Germany

SiW-ECAL for the ILD



The SiW ECAL in the ILD Detector



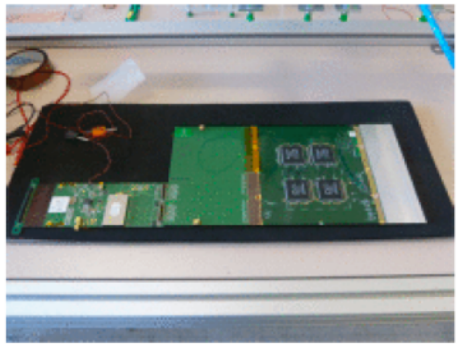
- $O(10^4)$ slabs
- $O(10^5)$ ASUs (PCB)
- $O(10^{6-7})$ ASICS
- $O(10^8)$ cells
  - 2000 m^2 of Si
- 130 T of tungsten

- Very compact design: Thickness of **20 cm for 20-30 active layers + 24X0 tungsten**
- Cell size of 5x5 mm → **all cells are self triggered + zero suppression** → **SKIROC ASIC (Omega)**
- Very limited space for inactive material (PCB, electronic components) → **No active cooling but Power Pulsing**

SiW – Technological Prototype

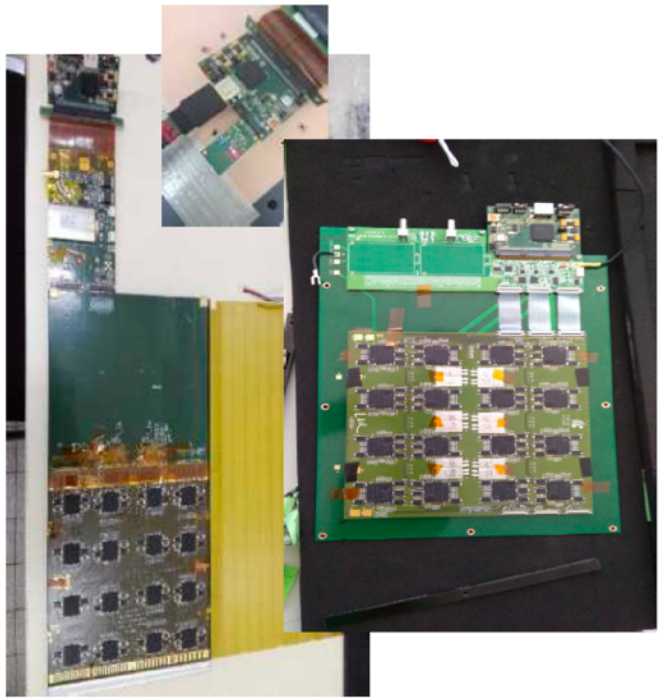
- Front end and VFE compactification with self-trigger ASIC (SKIROC2/2a) operated in power pulsing, higher granularity (5.5x5.5mm), compact modules

2010-2015



- Version 0 of techn. Prototype
- 256 channels
- 1st power pulsing tests

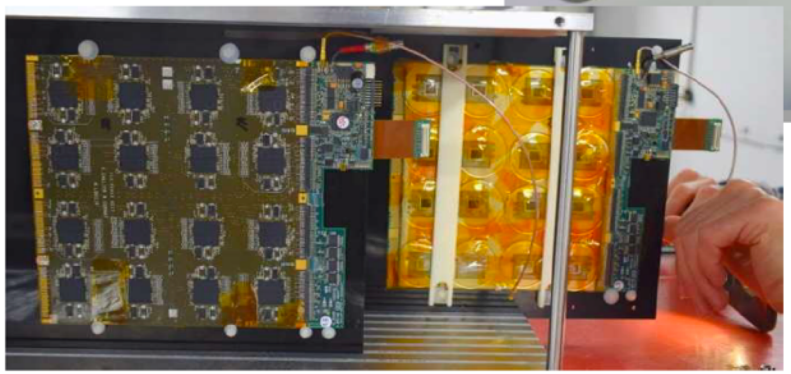
2015-2018



2015-2019

- Ultra thin PCB (COB) with wirebonded ASICs

2018-2019

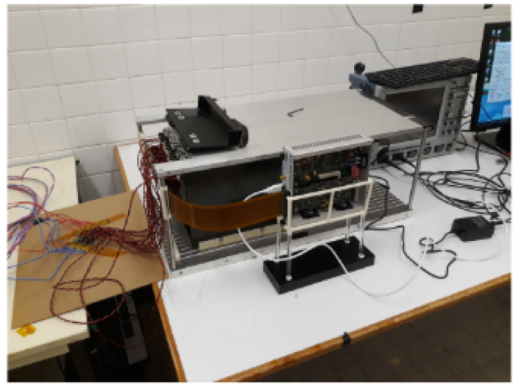


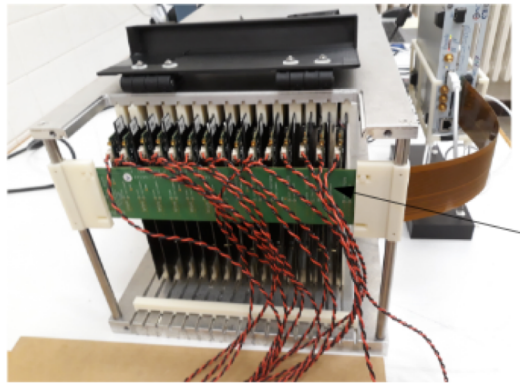
- **1024 chns per module in a 18x18xm surface**
- **Ultra compact DAQ and PCBs**

SiW-ECAL facing an intense test beam campaign

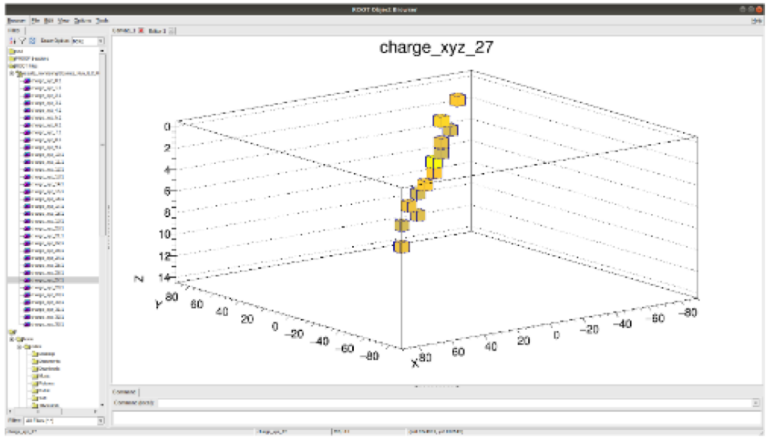
Beginning of June ...

Running with 15 layers with 15360 channels (of which 13824 equipped with wafers !!!!)





First cosmic (Adrian Irles)



- Already now a major breakthrough for the project
  - (Towards) the culmination of 10 years of work on Technological prototype
- Real size digital readout gives realistic impression of density at extremities of Ecal layers
- Revision and scrutinisation of setup
  - This talk

IFIC in CALICE

Adrian Irles' proposal of CALICE membership accepted by CALICE (unanimously supported)

Work in the SiW-ECAL prototype (A.I. + 50% of an student)

IFIC/Spain is in a privilege position to get a leading role in the detector integration and beam test preparation/operation/analysis

A.I. is (the main?) expert for commissioning/validation/operation/analysis of the prototype

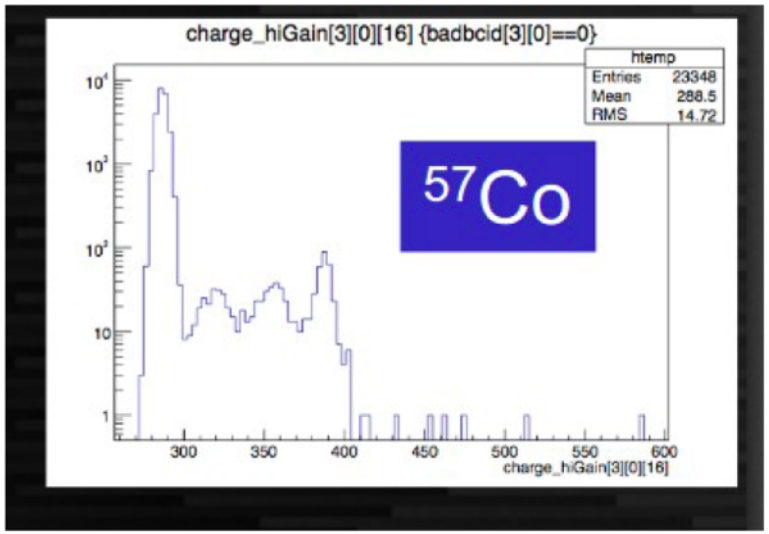
Next TB happening (??) at the end of November 2020.

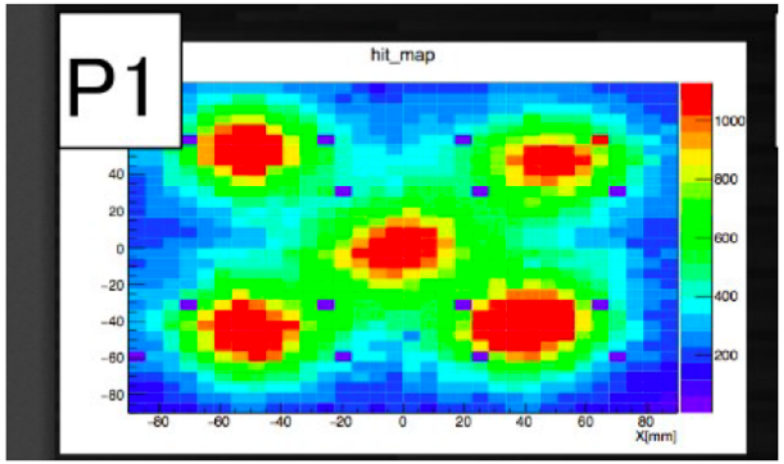
IFIC in CALICE (short term activities - I)

- IFIC will play an important role in the validation/test of the coming Hardware developments
  - Integration with EUDAQ (a step towards integration with AIDA TLU + telescopes)

    Also an activity of interest for the IFIC CMOS pixel group → will make possible the combination of setups

  - Validation/debugging/optimization of new DAQ
  - Validation of new PCBs (to come during 2021-22)
- Therefore IFIC will have fully equipped testbench + few modules
  - "Mini SiW-ECAL" calorimeter at home (w/o tungsten)
  - Useful for small experiments at home





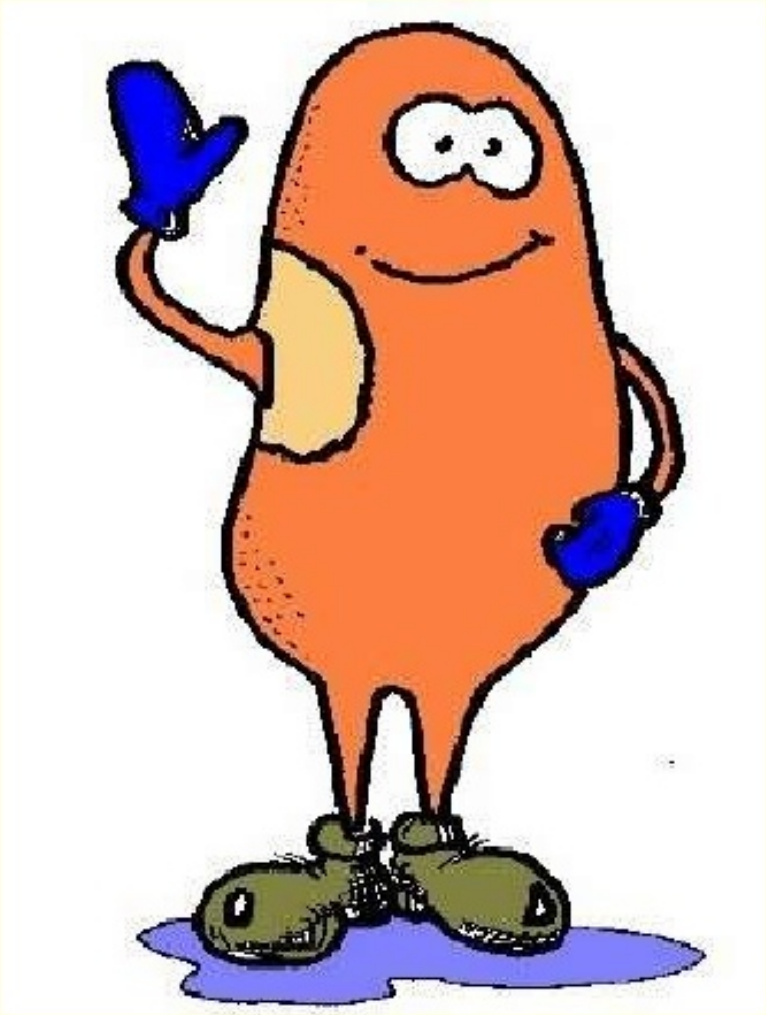
IFIC in CALICE (short term activities - II)

- IFIC will contribute to the purchase of wafers to complete the SiW-ECAL stack
  - Discussions ongoing with Hammamatsu
  - Develop dedicated 6” PID diode sensor characterization capabilities at IFIC? Spain? (under consideration)
- Contribution to complete the stack
- SiW-ECAL is currently exploring the 8” wafer solution (instead of the 6”)
  - Price reduction “profiting” from CMS production (and also geometry)

    But for today, they took the full production: no 8” availability for others until end 2021

  - Feasibility of mass scale production still to be proven
  - Characterization, comparison of performance not studied yet…
  - Could the IFIC/Spain play a role in this?

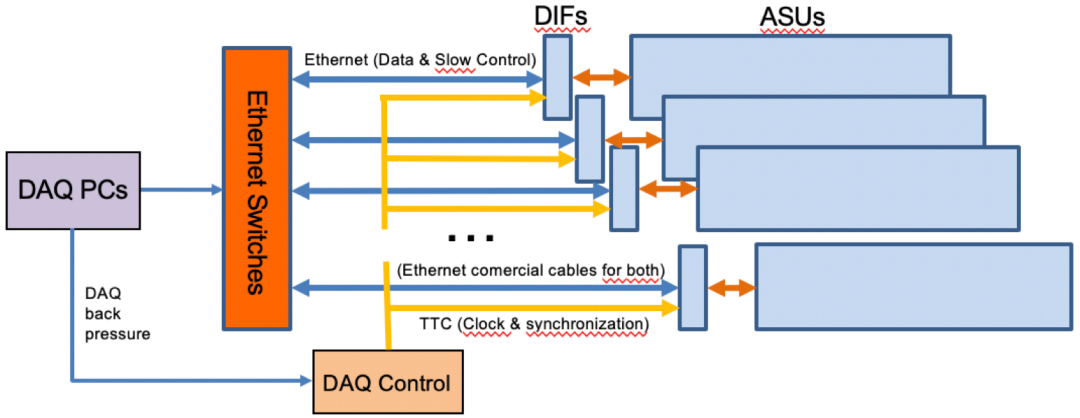
Thank You For Your Attention !



BACK-UP

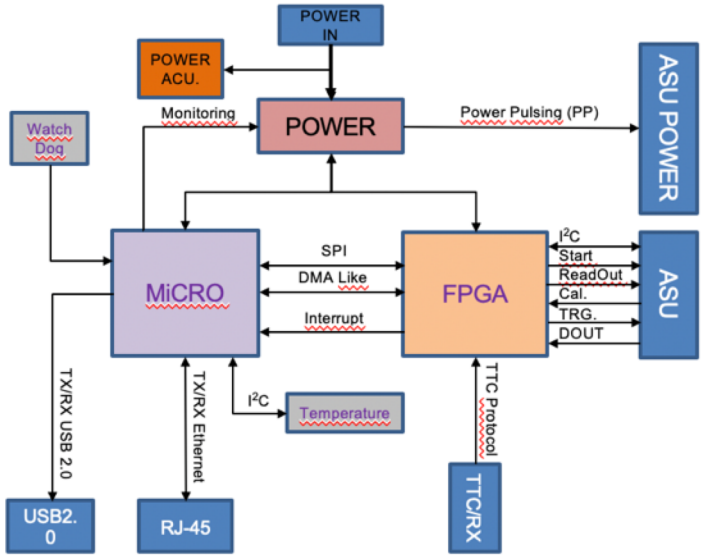
SDHCAL DAQ architecture

A *central PC* collects data from all the *ASUs* (containing de *ASIC chips*) through an *Ethernet switch* acting in such a way as data concentrator and generates the required commands for *ASU* and *DIF* configuration generating at the same time synchronization signal required for a correct data acquisition process.

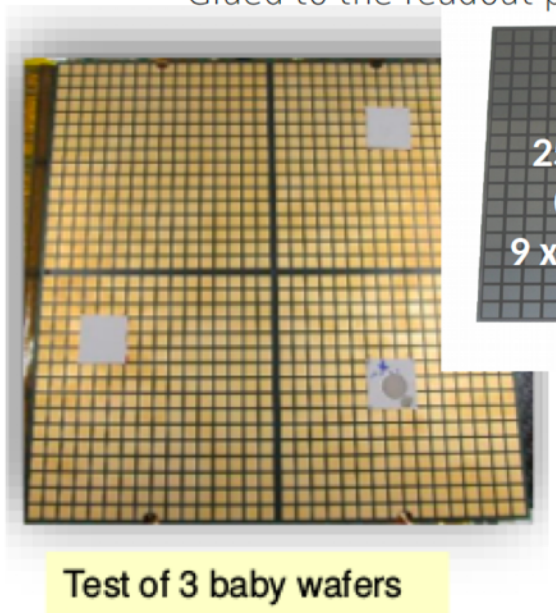


DIF architecture

- Only one DIF per plane (instead of **three**)
- DIF handle up to 432 HR3 chips (vs **48 HR2** in previous DIF)
- **Clock and synchronization** by TTC (already used in LHC)
- **93W Peak power supply** with super-capacitors
  (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**

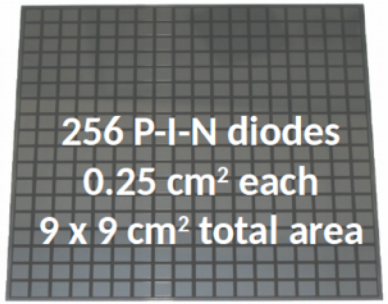


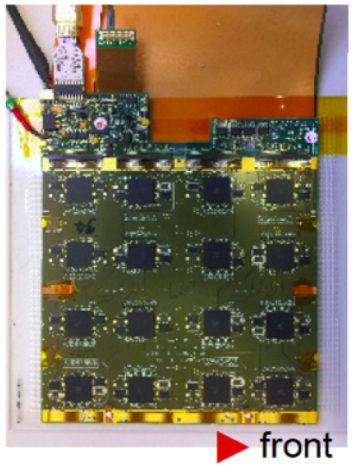
Glued to the readout pads



Test of 3 baby wafers

back

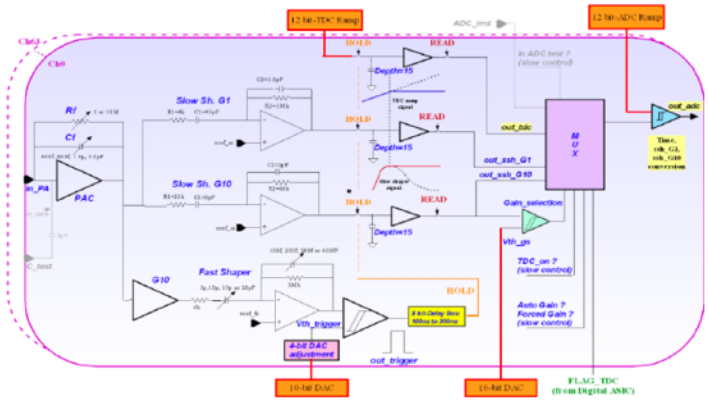




front

"Simple" P-I-N diode Silicon Sensors

Designed for ILC : Low cost, 3000 m2
Minimized number of manufacturing steps
Target is 2.5 EUR/cm2
Now : 10 EUR/cm2 (Japan)
Use of floating guard-rings



SKIROC2a is a 64-channel front-end chip

ADual gain charge ADC (1/10 factor)
BAutotrigger chain → high gain fast shaper
C15 memory buffers.
D
EDynamic range : 0.5 MIP (~4fC) to 2000 MIP

A. Irles, 6th October 2020

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