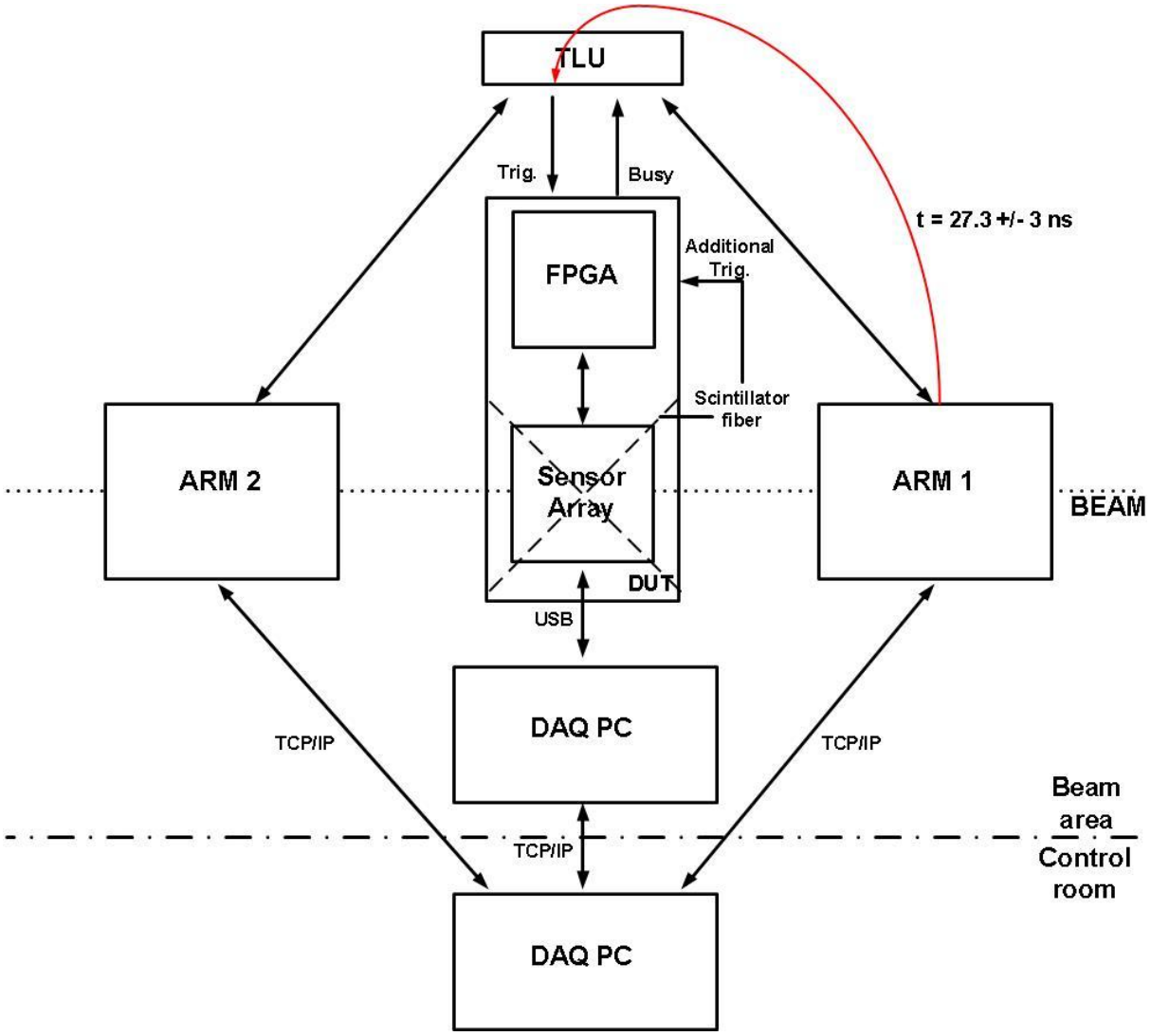
Testbeam preparation

O. Alonso, E. Vilella, A. Diéguez

VLSI Design Group
Department of Electronics
Universitat de Barcelona

Testbeam setup



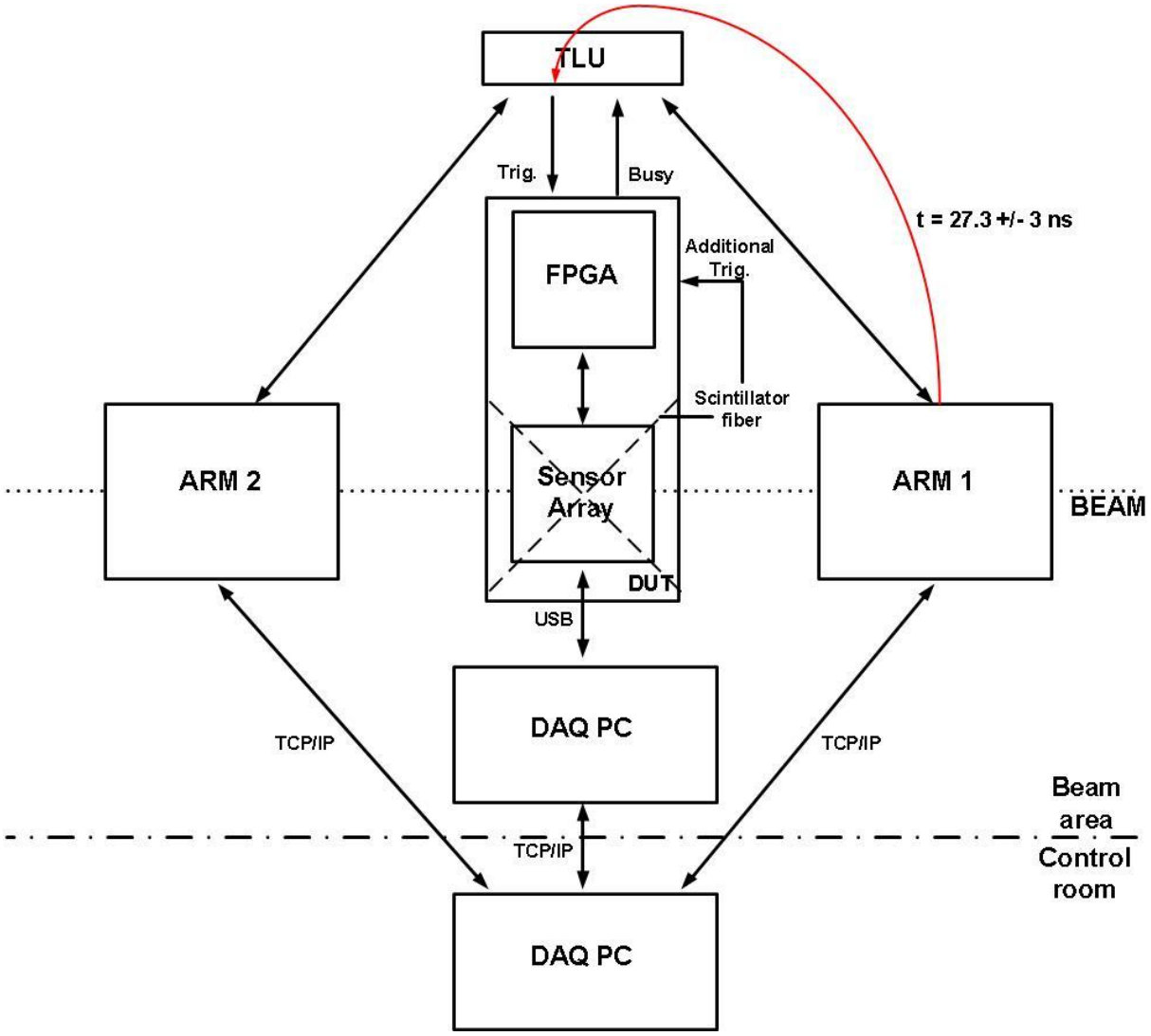
DUT

- Array 1mm x 1mm
- Additional trigger
- One or two stacked DUTs

Additional

- Protection box
- SW for the PCs

Testbeam setup



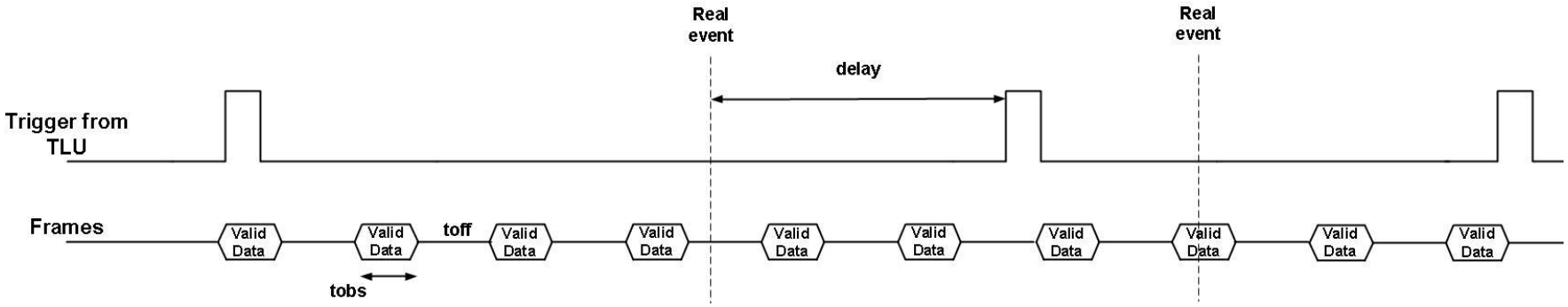
Triggers

- TLU
- Fiber + TLU

Configurable

- Stored frames
- tobs, toff
- Delay between clocks

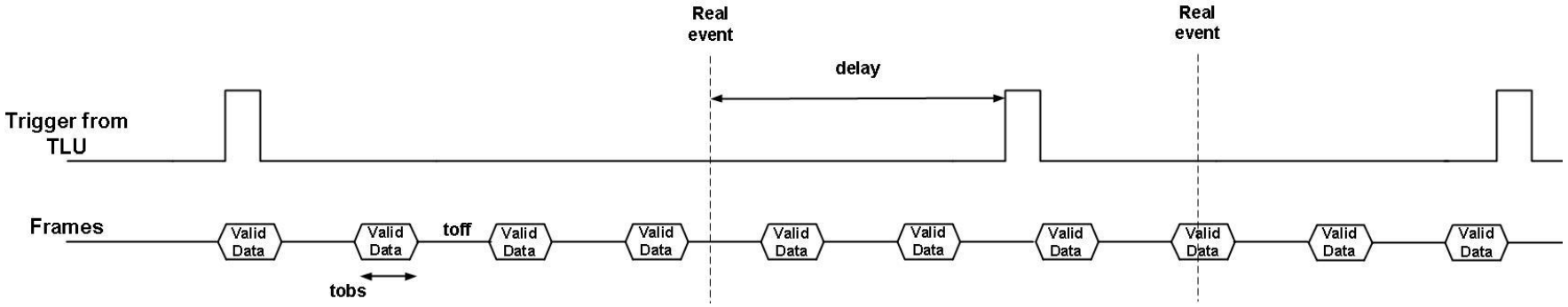
Testbeam setup



- Min. delay = 27.3 +/- 3 ns
- Min. toff to avoid after pulsing = 300 ns.
- It is needed to store n frames to deal with the delay.
- tobs, toff must be calculated.

Testbeam setup

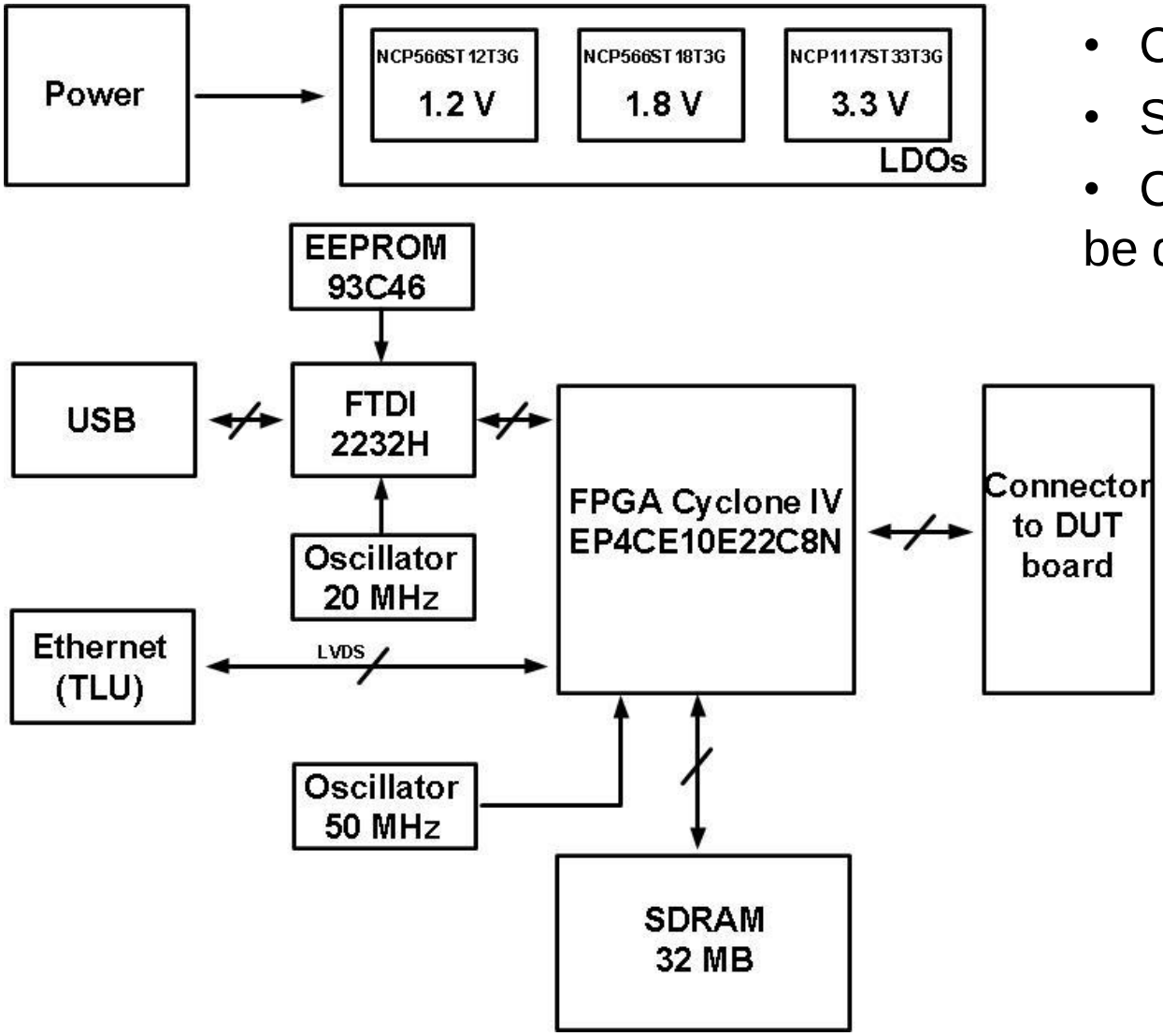
- FPGA continuously storing (and discarding) n frames in a FIFO.
- When trigger is asserted:
  - TLU sends timestamp
  - Data from the FIFO is written to a SRAM
- Read request:
  - With this strategy it is possible to still measure and store data.
  - Busy line is asserted and TLU stops sending triggers while reading SRAM.



Testbeam setup

- Nano DE-0 FPGA from Terasic
- No LVDS
- Not flexible (USB streamout using NIOS)
- Adapter PCB must be used

Testbeam setup



- Custom FPGA board
- Similar to DE-0 board
- Connector to DUT must be defined

Testbeam setup

To do

- Design and fabrication of the FPGA board
- Test of the FPGA board with the APDs Array (prove functionality)
- Test of the FPGA reading constantly data from the Array via USB port
- Test using 2 stacked boards (with one array each one) and the scintillators
    - Characterization of times (nº of frames to store)
    - Delays between clocks
- Further tests to be done (what & where) must be defined