Work on DEPFETS performed by UB during 2011

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Outline

- Resume
- IBM 90 nm (DHP 0.2)
- TSMC 65 nm (DHPT)
- Future work (temperature measuring system)
- Conclusions

Resume

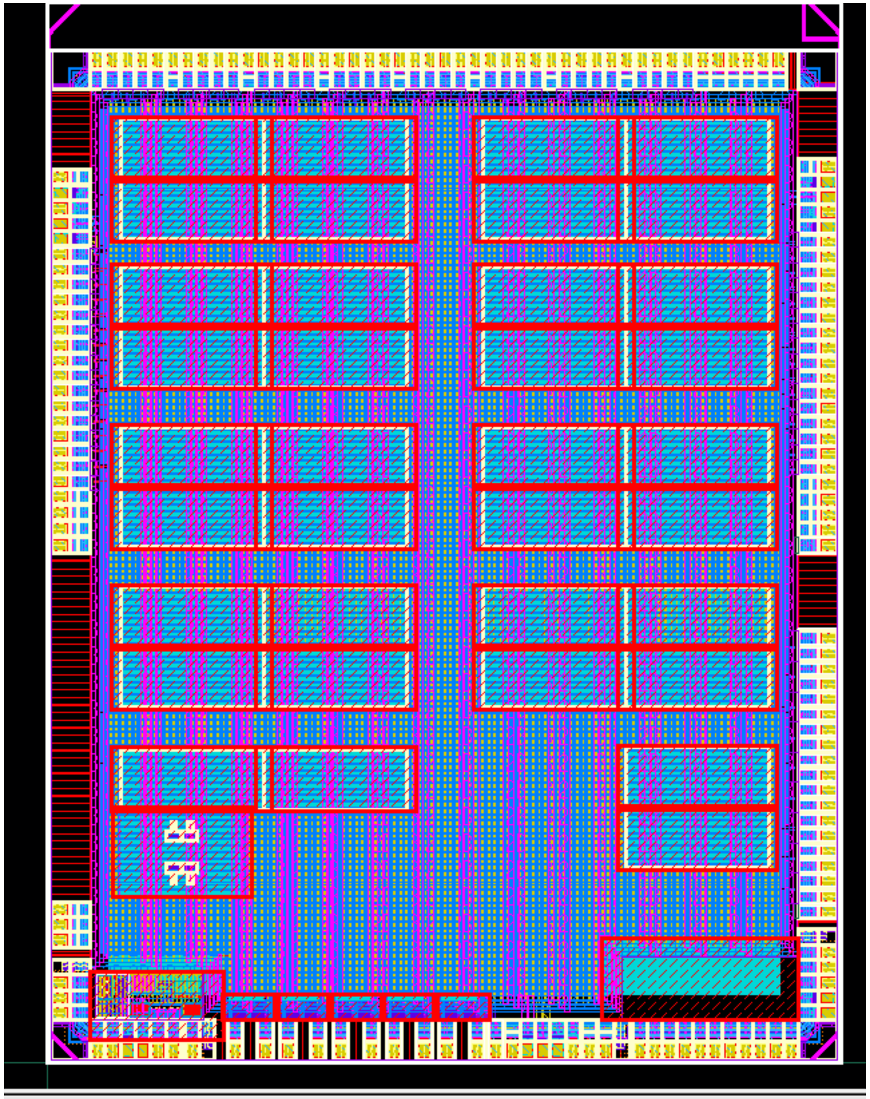
- UB collaboration in the DHP 0.1 chip consisted on:
  - JTAG control
  - Bandgap
  - 8-b DAC with output voltage
  - 10-b ADC
- All blocks work correctly but the ADC and the bandgap need some improvements.
- For the DHP 0.2 chip, Hans Kruger asked for the next modules:
  - 8-b DAC with output current for biasing some analog blocks
  - 10-b ADC
  - Independent temperature current source
  - Temperature measuring circuit (April 2011)
  - Complete bias module for DHP 0.2 analog modules (April 2011)
- The 8-b DAC with output voltage and the bandgap were not needed.
- UB members working on DHP 0.2: Raimon Casanova, Oscar Alonso.
- DHP 0.2 finished and sent to fabricate late May 2011. Expected by late November 2011.

Resume

- April 2011 MOSIS announces that IBM 90 nm process will be not longer available. Further developments of DHP chip will have to be done in a new CMOS process.
- 65 nm CMOS process from TSMC chosen as the new technology for fabricating DHP chips:
  - Digital modules are easily translated to the new technology.
  - Analog modules have to be redesigned from scratch.
  - Learning curve.
  - New design kit. It has to be checked.
- Mini-asic (DHPT) scheduled to beginning October 2011 to design some basic analog modules.
- UB contribution to DHPT chip:
  - 2 temperature independent current sources
  - 8-bits DAC with output current
- Future work:
  - DHP 0.2 test
  - DHPT test
  - Redesign temperature measuring circuit

DHP 0.2

DHP 0.2 chip



- Technology: IBM 90 nm
- Size: 3.145 mm x 4 mm
- Memory blocks (2048 rows equivalent):
  - Raw data
  - Offset data for 2 bit DAC
- Data processing core
- Output FIFO
- Serializer:
  - PLL
  - 20:1 mux
  - CML driver (pre-emphasis)
- Analog blocks:
  - 11 bias DACs (8 bit)
  - ADC(10 bit)
  - temp. measurement

DHP 0.2 chip (UB contribution)

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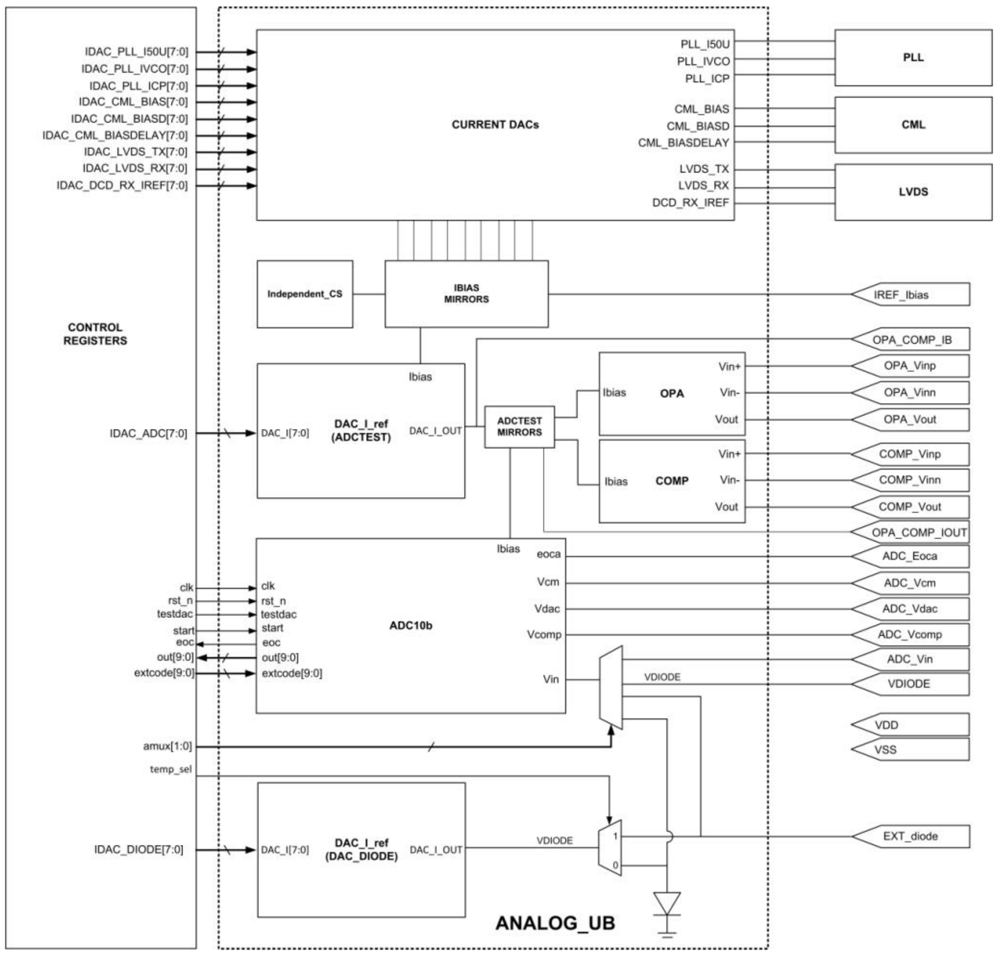
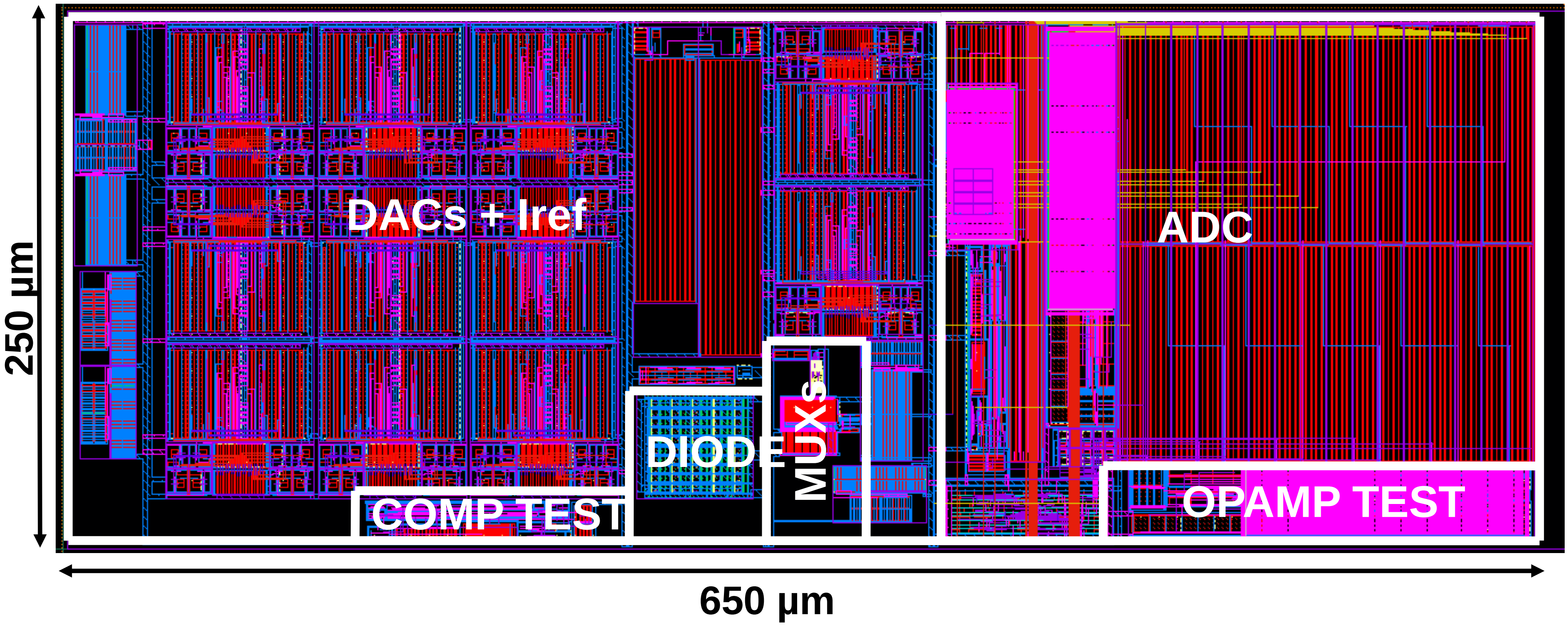
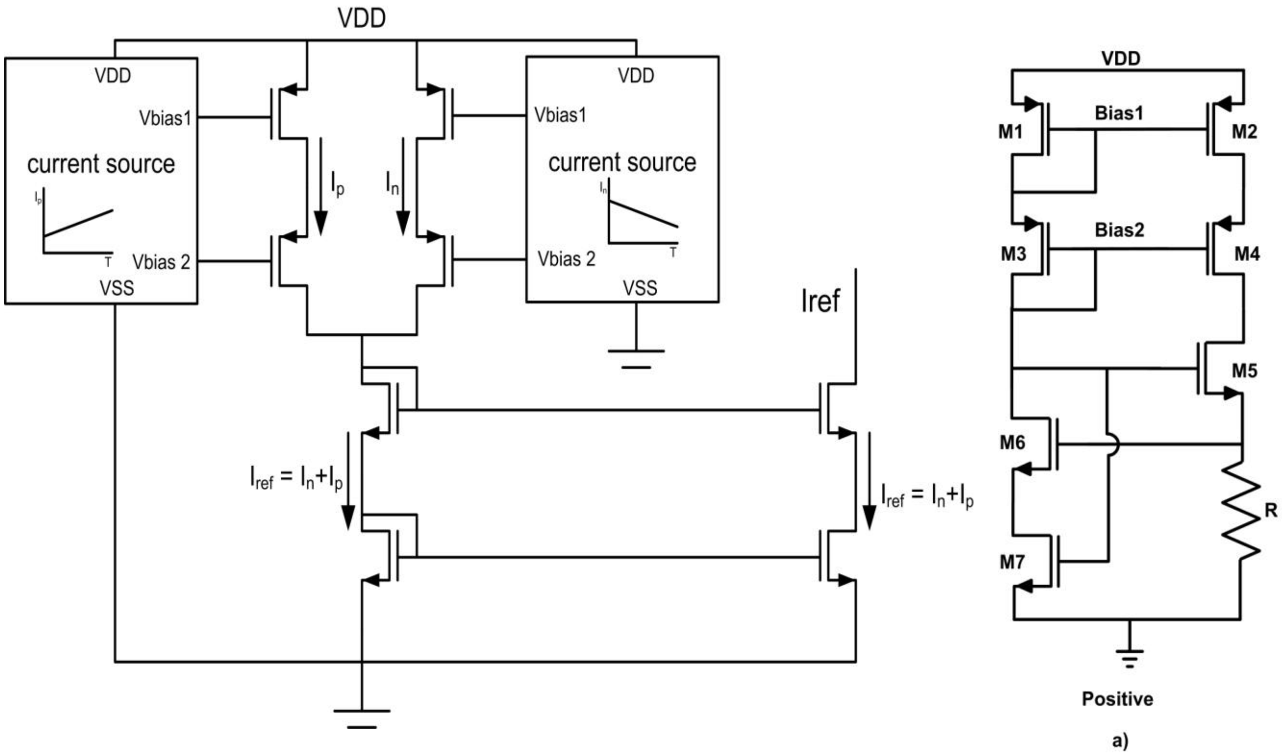


- 9 DACs with output current (LSB =1 µA) to bias CML, PLL and LVDS blocks.
- Independent temperature current reference (1 µA).
- Temperature measuring system:
  - Internal/external diode.
  - Output current DAC to drive diodes.
  - 10-bits ADC to measure diode voltage.
  - Accuracy limited by LSB of the ADC to 2 ºC.
  - Controlled by JTAG.
- Modules for testing: opamp, comparator, current reference, and DAC.

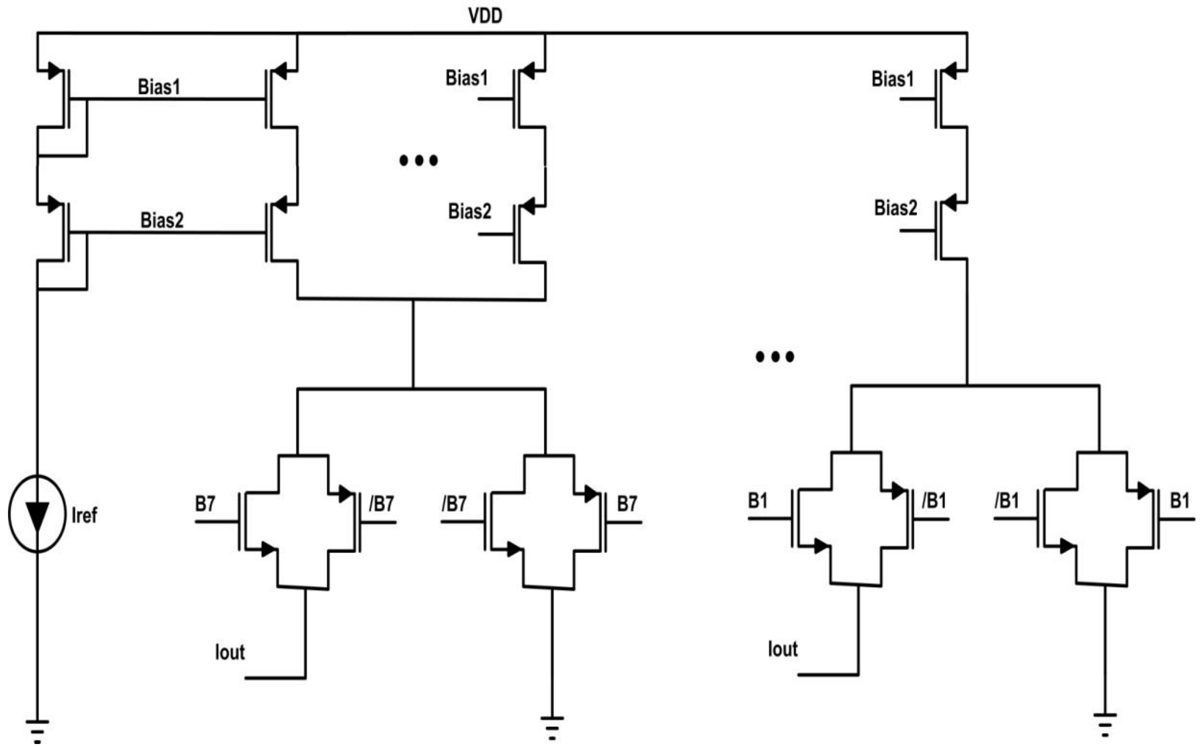
DHP 0.2 chip (UB contribution)



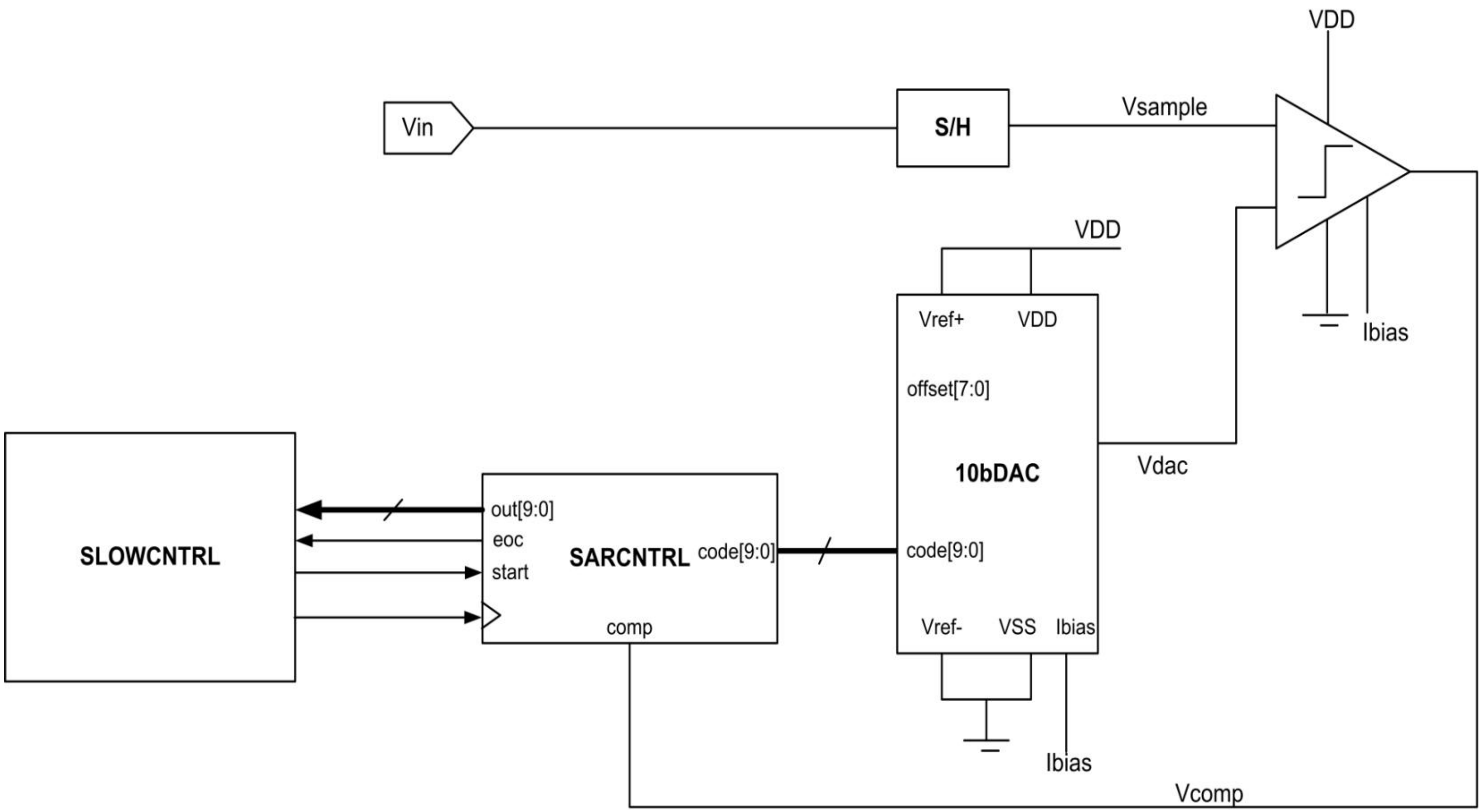
DHP 0.2 chip (UB contribution)



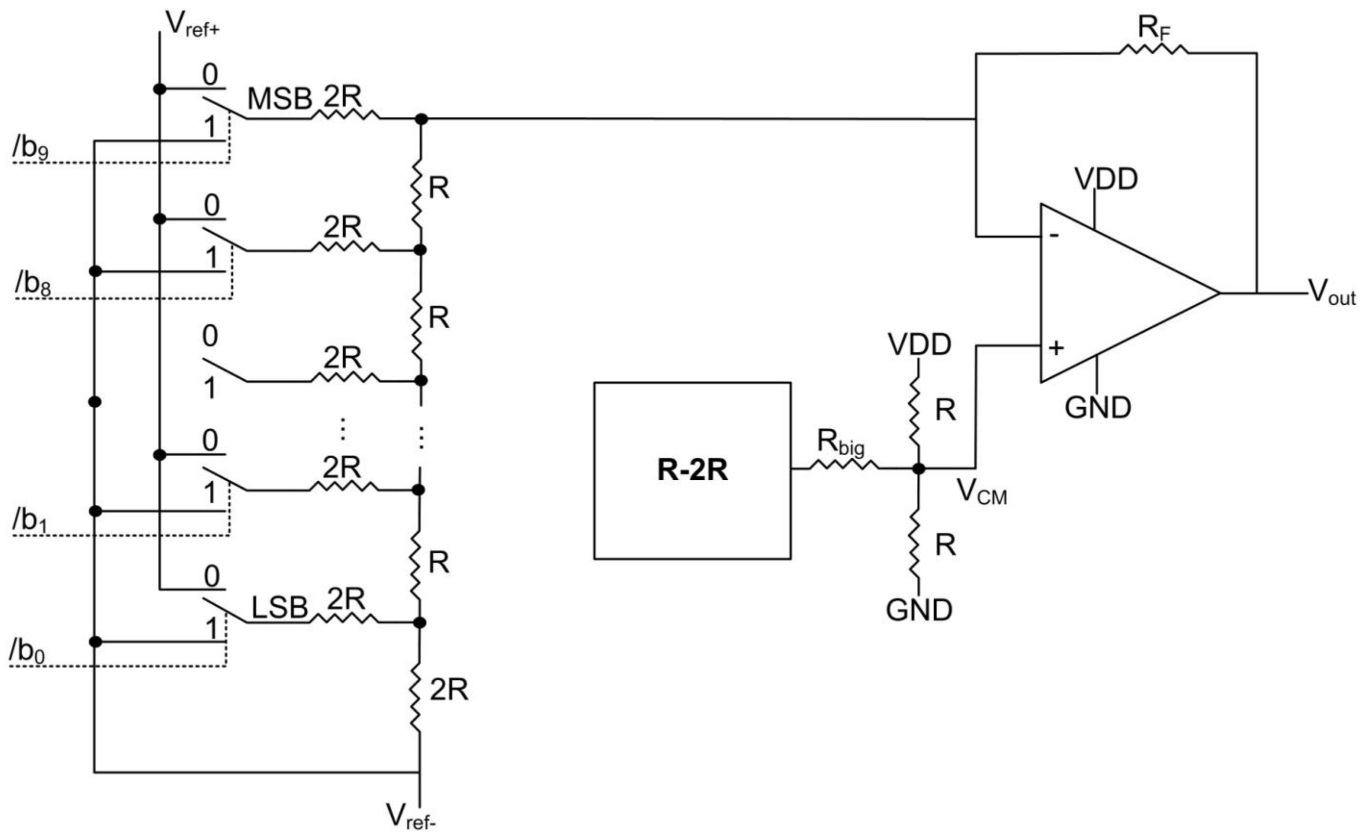
DHP 0.2 chip (UB contribution)



DHP 0.2 chip (UB contribution)



DHP 0.2 chip (UB contribution)



DHP 0.2 (Temperature measuring system)

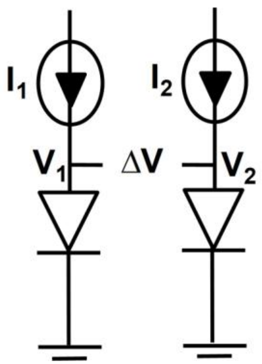
Diode I-V characteristic

$$I_1 = I_S\left(e^{\frac{qV_1}{nKT}} - 1\right) \Rightarrow I_1 \approx I_S e^{\frac{qV_1}{nKT}} \Rightarrow V_1 = \frac{KT}{nq}\ln\left(\frac{I_1}{I_S}\right)$$

for V_{BE}>>KT/q
(forward biasing)

n = non-ideal factor (1<n<2)
- for large forward voltages n~1
- for low forward voltages n~2

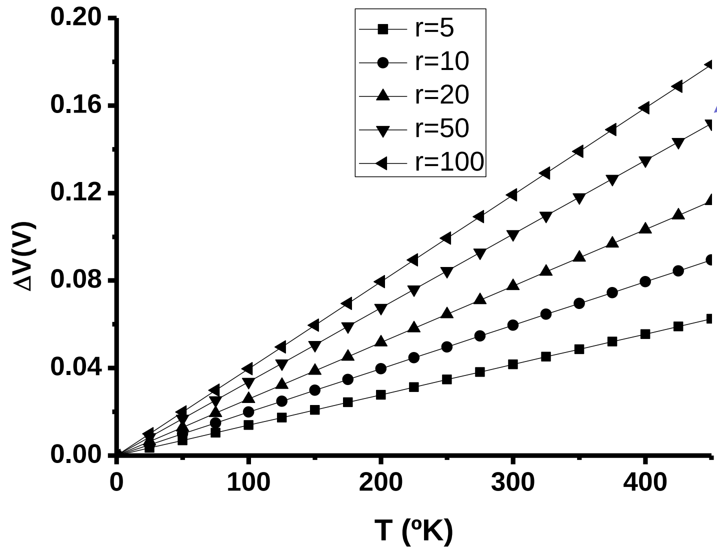
Temperature measurement



- Two equal diodes but biased with different currents (I_1 and I_2).
- I_1=r I_2 where *r* is the current ratio.
- The voltage difference at the anodes (ΔV) is proportional to absolute temperature (VPTAT).

$$\Delta V = V_1 - V_2 = \frac{nKT}{q}\ln\left(\frac{I_1}{I_2}\right) = \frac{nKT}{q}\ln(r) \Rightarrow T = \frac{q}{nK}\frac{V_1 - V_2}{\ln(r)}$$

DHP 0.2 (Temperature measuring system)



$$slope = \frac{nK}{q}\ln(r)$$

r	slope (mV/ºK)
5	0.139
10	0.198
20	0.258
50	0.337
100	0.397

A variation of 1ºK produces a small voltage variation of 0.397mV for a given large current ratio *r* of 100.

A high resolution ADC is required to obtain accuracies of 1ºK/bit.

Future work (Temperature measuring system)

Diode I-V characteristic

$$I_1 = I_S\left(e^{\frac{qV_1}{nKT}} - 1\right)$$

n = non-ideal factor (1<n<2)

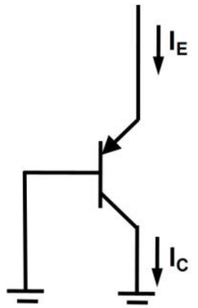
•for large forward voltages n~1

•for low forward voltages n~2

•Since n depends on Is, which in turn depends on processing parameters, the PTAT voltage becomes sensitive to processing spread. This prevents the use of practical silicon diodes for accurate temperature sensing.

•Bipolar transistors behave much more ideal, with a non-ideal factor very close to 1.

Diode configuration

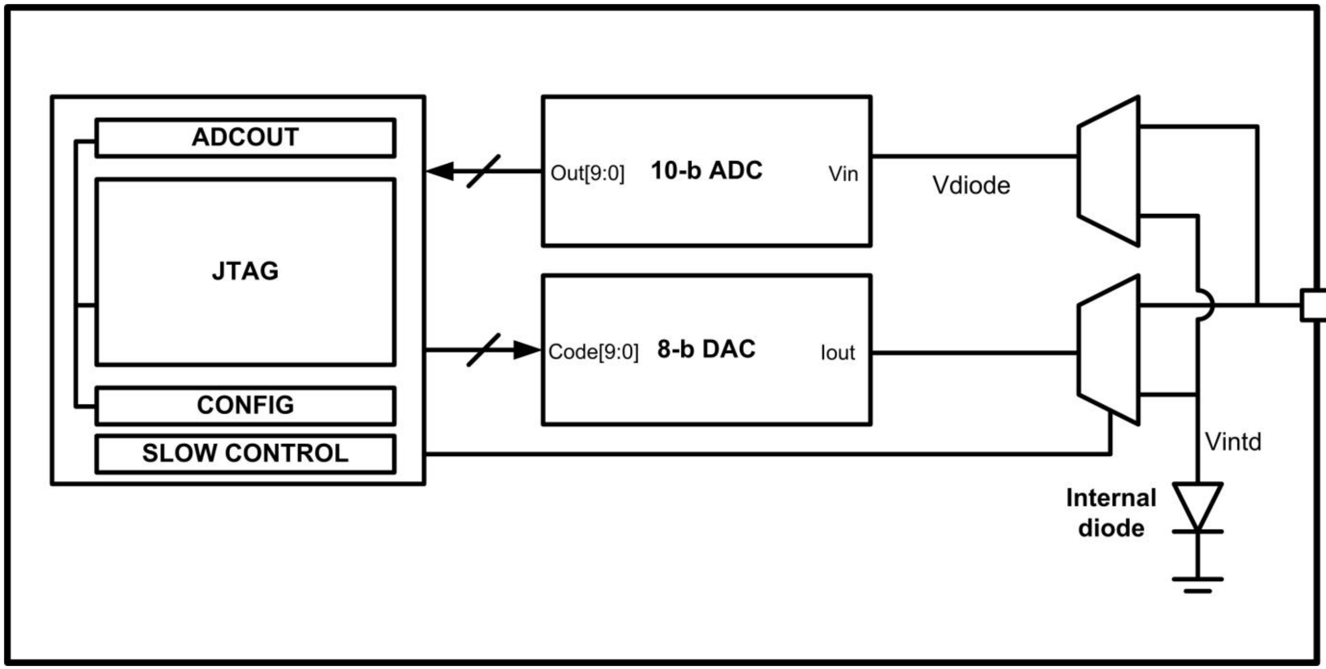


$$I_C = I_S\left(e^{\frac{qV_1}{nKT}} - 1\right) \quad \Rightarrow \quad I_C \approx I_S e^{\frac{qV_1}{nKT}}$$

for V_{BE}>>KT/q

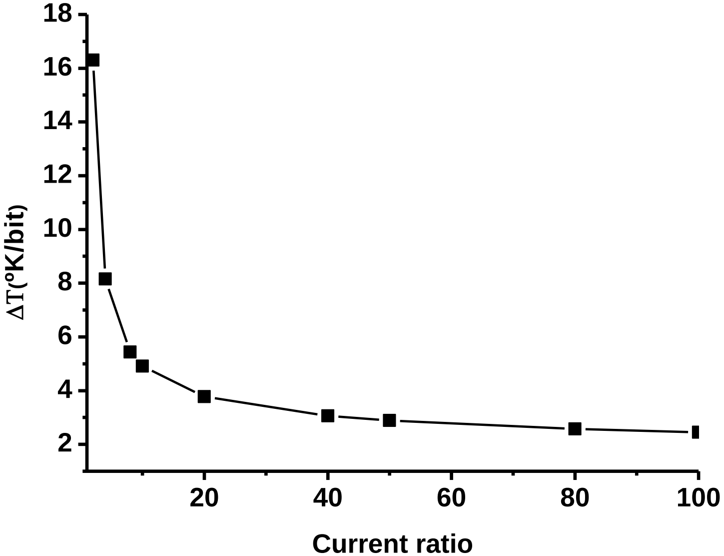
$$I_E = \frac{\beta_F + 1}{\beta_F} I_S e^{\frac{qV_1}{nKT}} = I_{SE} e^{\frac{qV_1}{nKT}}$$

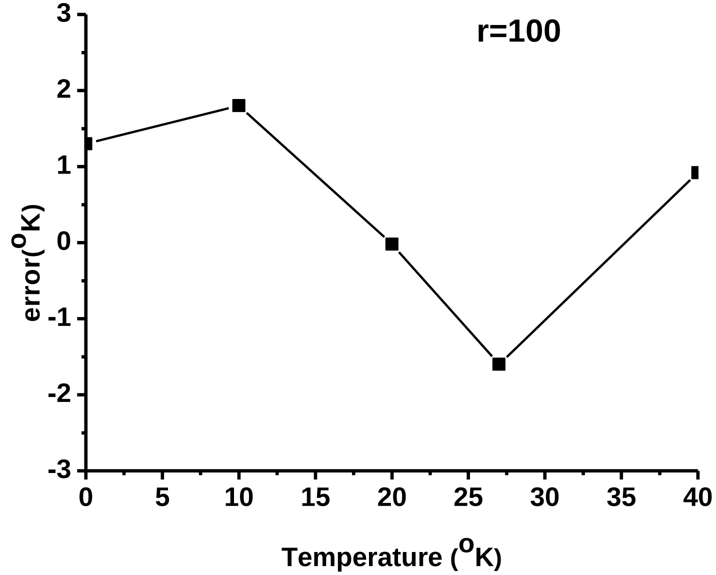
DHP 0.2 chip temperature measuring system



- Internal and external sensing diodes.
- Internal diode implemented with a PNP bipolar transistor.
- Current ratio programmable (1 to 255).
- Currents applied can be adjusted between 1 µA to 255 µA.
- Digitalized voltage at the diodes is transmitted through JTAG for off-chip processing.

DHP 0.2 chip temperature measuring system



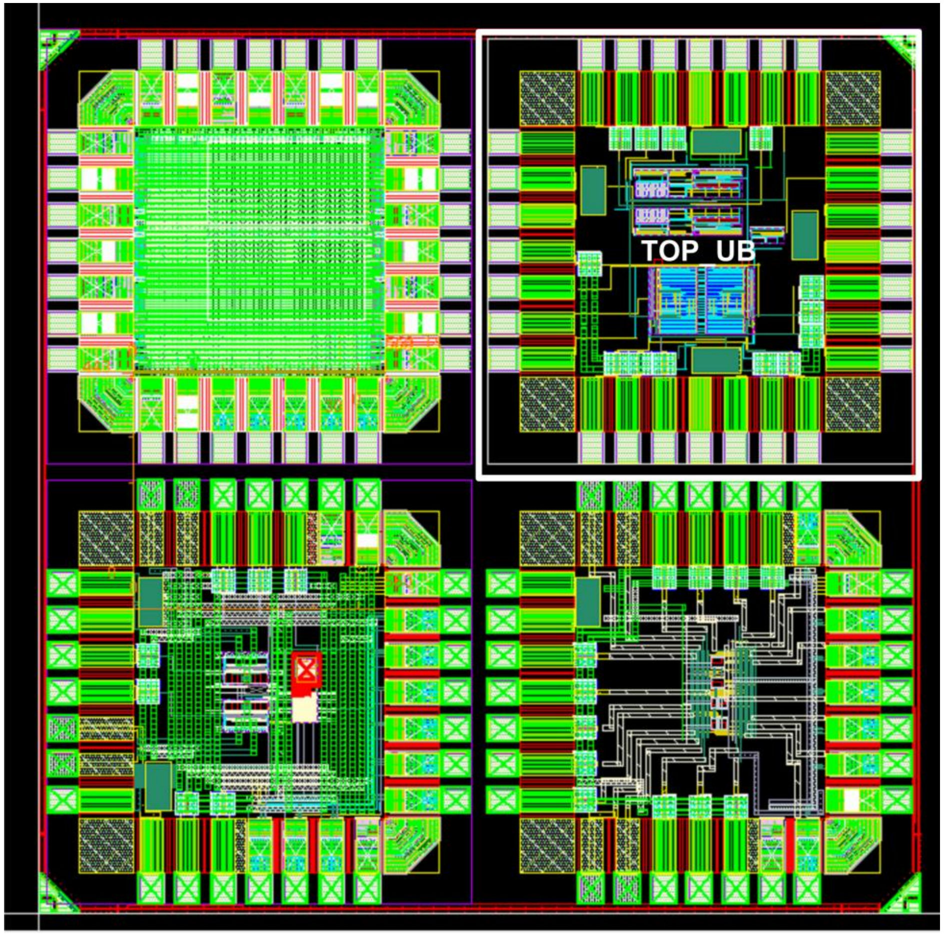


•To achieve accuracy of 2ºK/bit, high current ratios have to be used => high currents. Three major drawbacks:

- •self heating effects
- •high power consumption
- •Non-ideal factor is not constant.

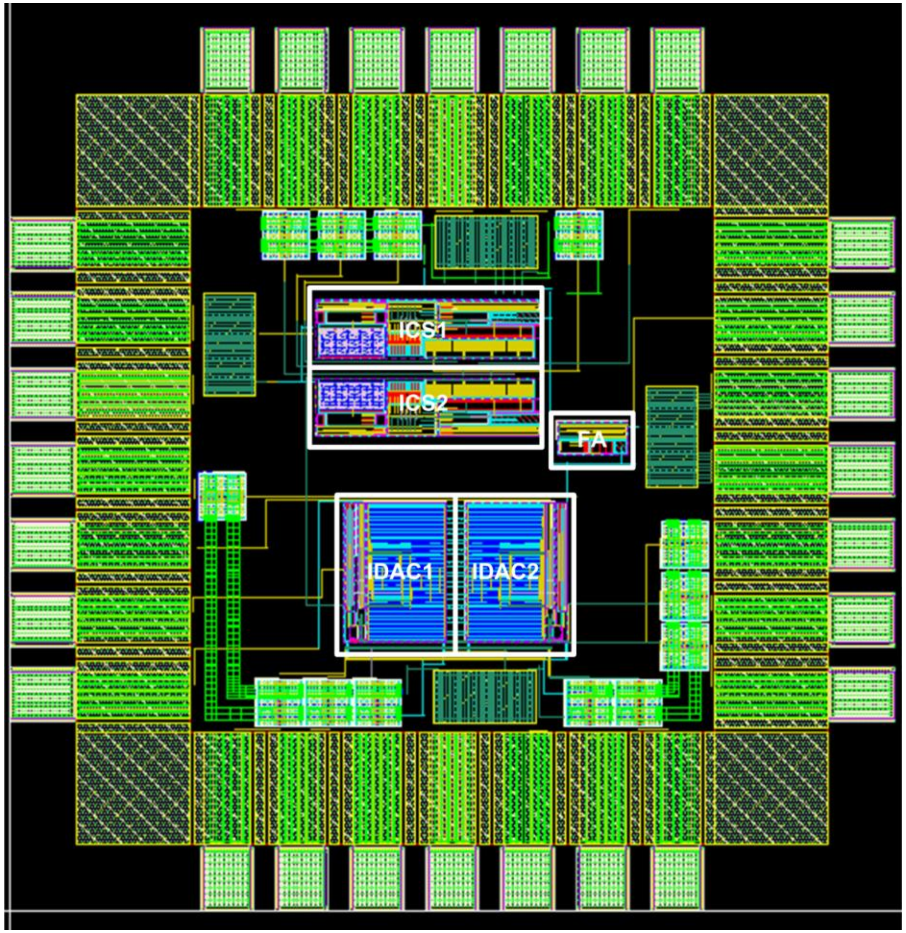
DHPT

DHPT chip



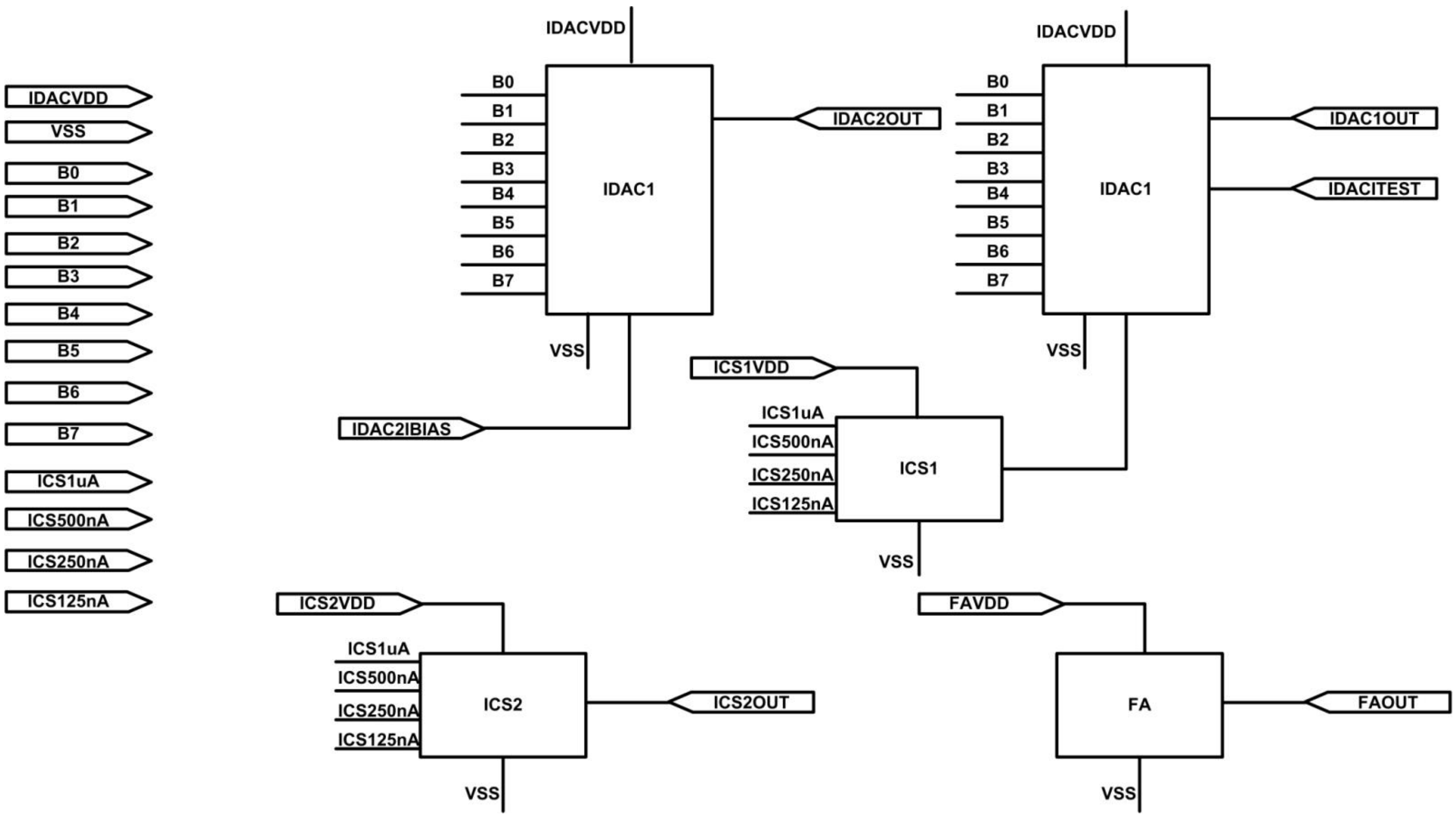
- DHPT is a mini-asic fabricated with a 65 nm CMOS process from TSMC.
- Total area: 2 mm x 2 mm
- It includes 4 mini chips:
  - JTAG
  - PLL
  - CSA
  - TOP_UB
- Send to fabricate during October 2011.

TOP_UB



- Technology: 65 nm TSMC
- Total area: 940 µm x 940 µm
- TOP_UB chip includes 5 modules:
  - Two 8-bits output current DACs.
  - Three independent temperature current sources.

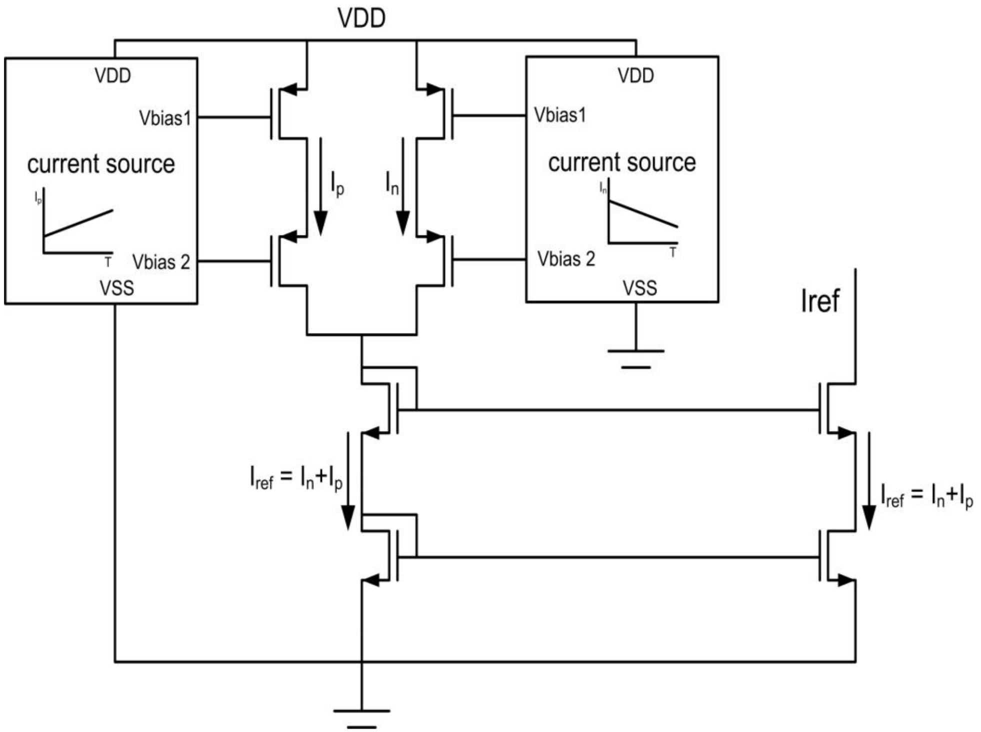
TOP_UB



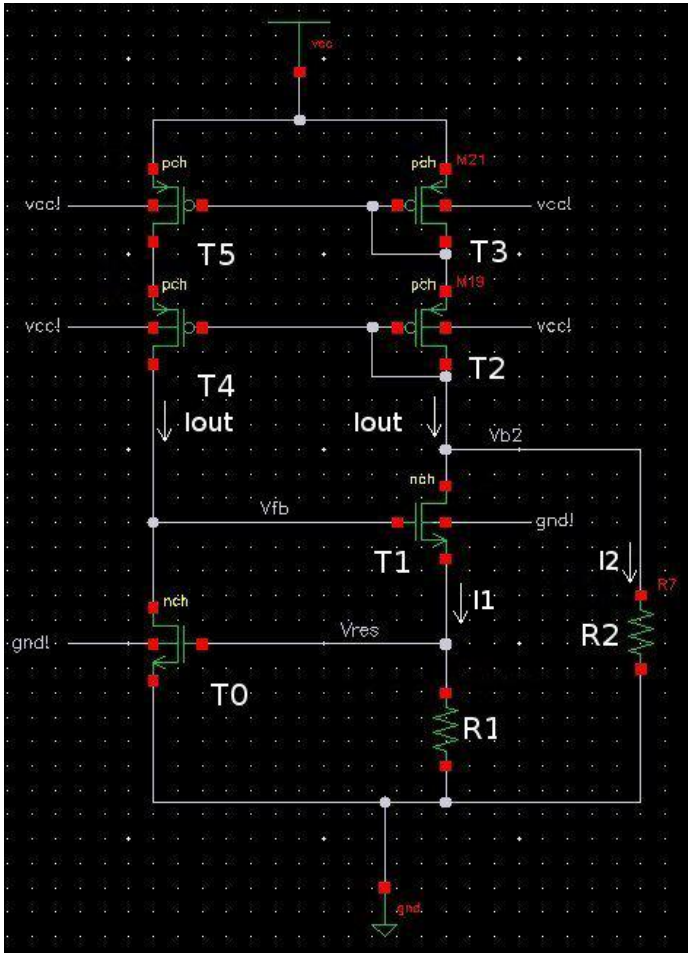
IDACVDD
VSS
B0
B1
B2
B3
B4
B5
B6
B7
ICS1uA
ICS500nA
ICS250nA
ICS125nA
IDACVDD
IDAC1
IDAC2OUT
IDAC2IBIAS
IDACVDD
IDAC1
IDAC1OUT
IDACITEST
ICS1VDD
ICS1
ICS2VDD
ICS2
ICS2OUT
FAVDD
FA
FAOUT
VSS

TOP_UB (current sources)

ICS current source

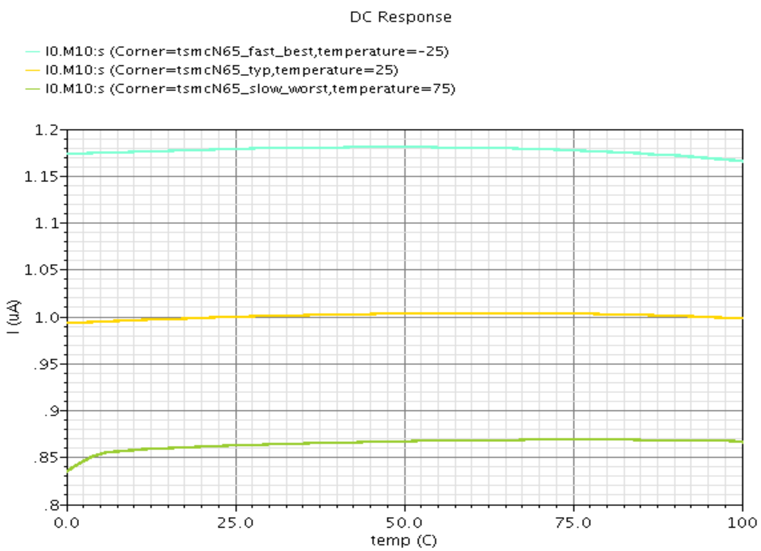


FA current source

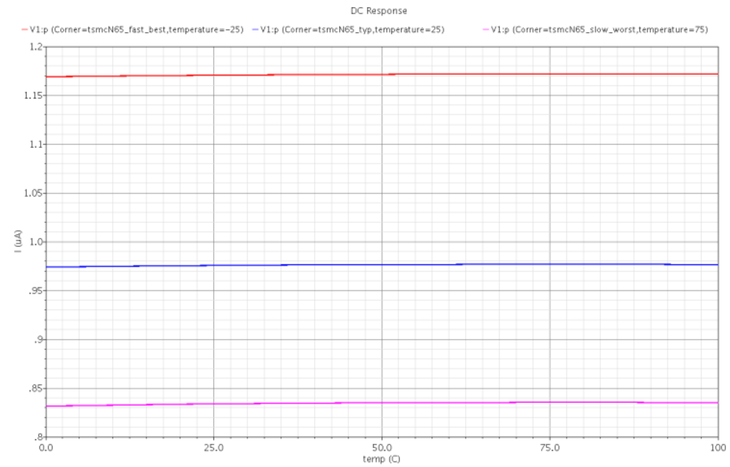


TOP_UB (current sources)

ICS current source

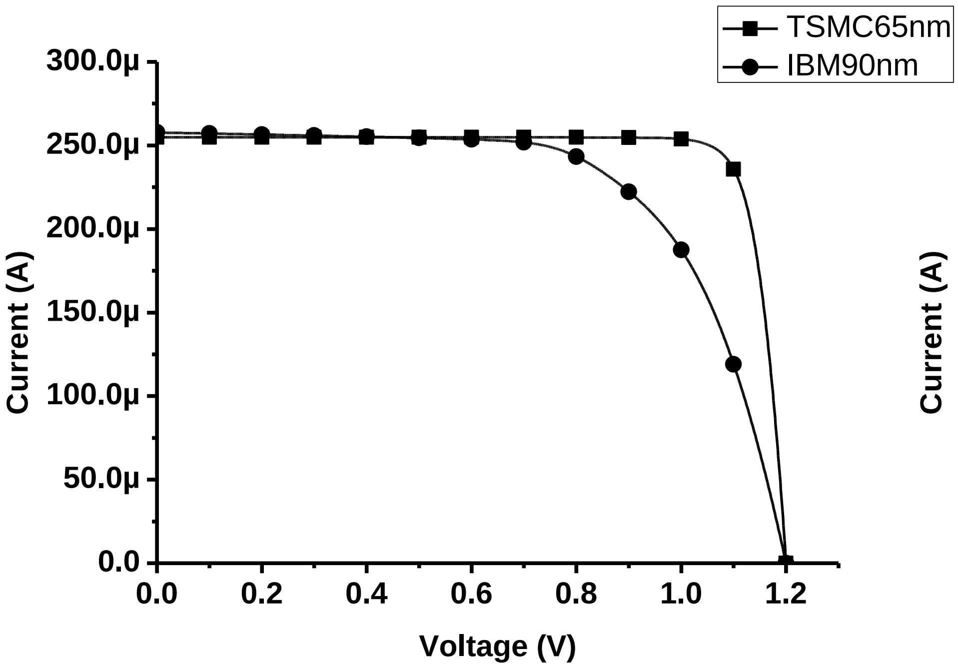


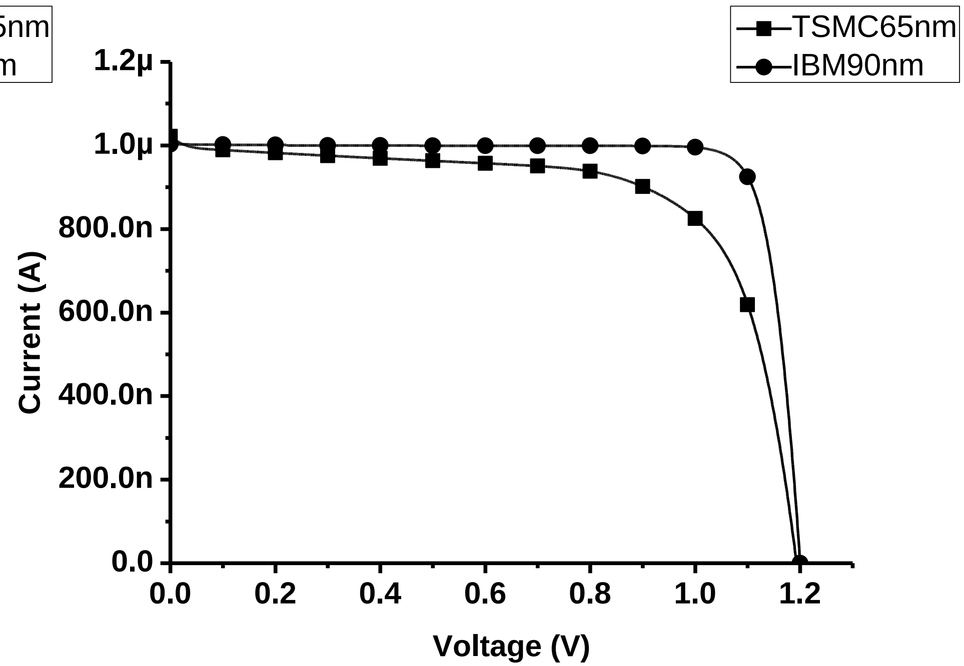
FA current source



- Two independent current sources implemented:
  - Source1: architecture fabricated and verified in older chip.
  - Source2: new architecture. No curvature in temperature, lower area and power consumption.

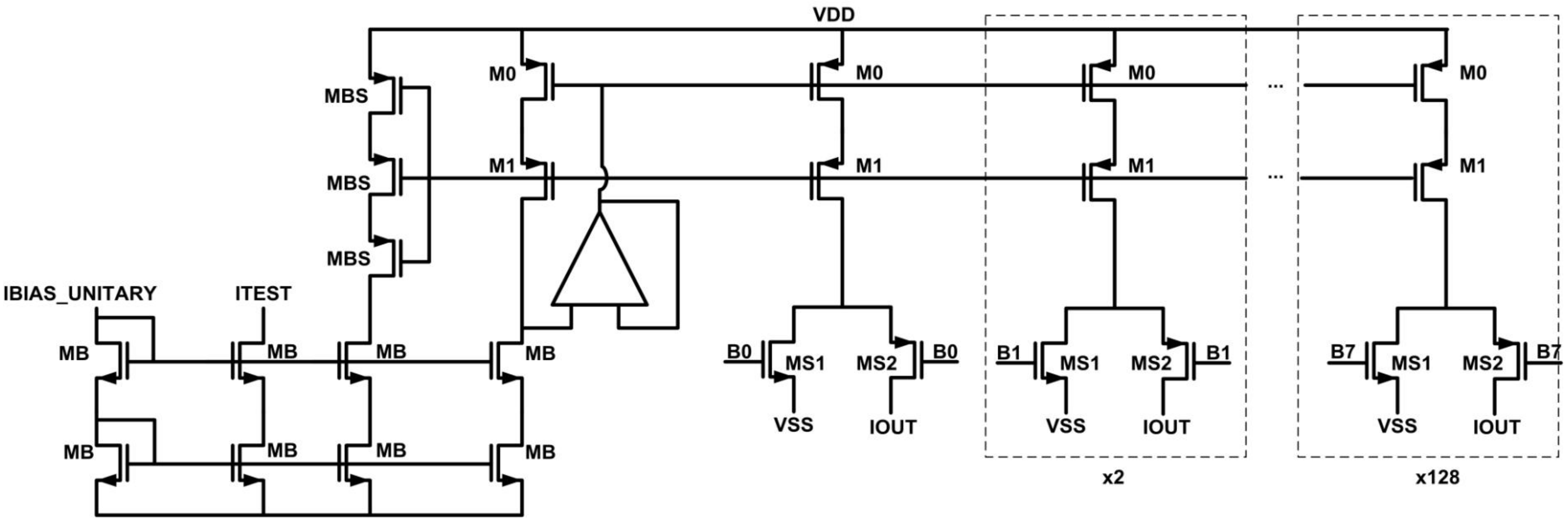
TOP_UB (improved DAC)





- Improved output voltage range (0 to 950 mV).
- Output current almost constant (less than 0.25% from nominal current) within the output voltage range.
- Gate leakage current compensation.

TOP_UB (improved DAC)



Future work (Temperature measuring system)

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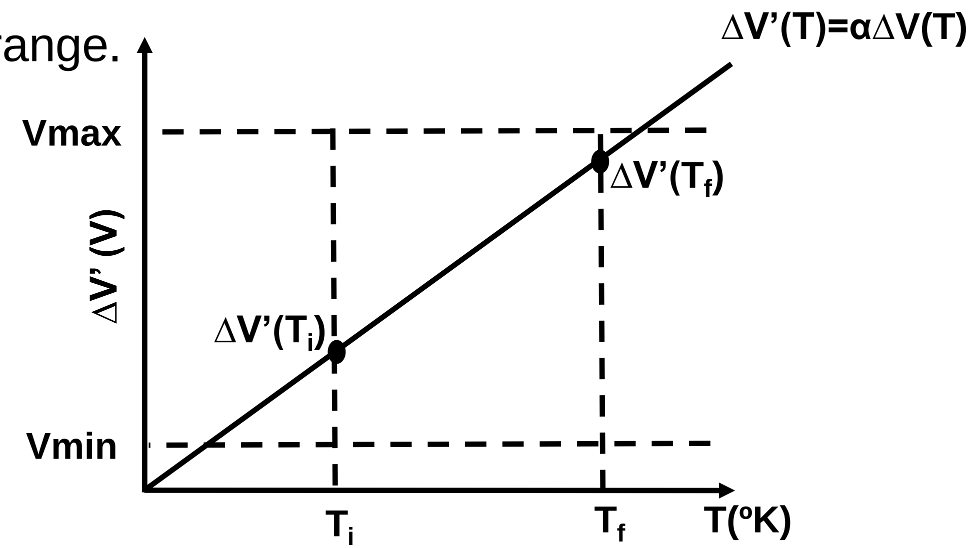
- Beta is usually constant in a range of I_C of several decades. In TSMC 65 nm this range goes from 0.1 nA to 10 µA.
- Accuracy can not be increased by augmenting the current ratio *r* if Beta has to be kept constant. Another approach has to be taken.
- A possible solution is to multiply the slope by a factor α.

$$\Delta V^{'}(T) = \alpha \Delta V(T) = \alpha \frac{nKT}{q} \ln(r)$$

- α is limited by the ADC input voltage range.

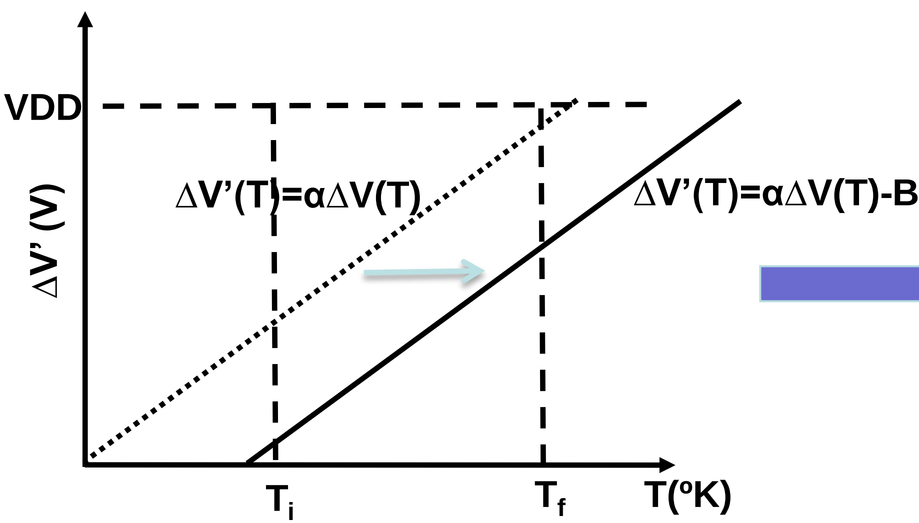


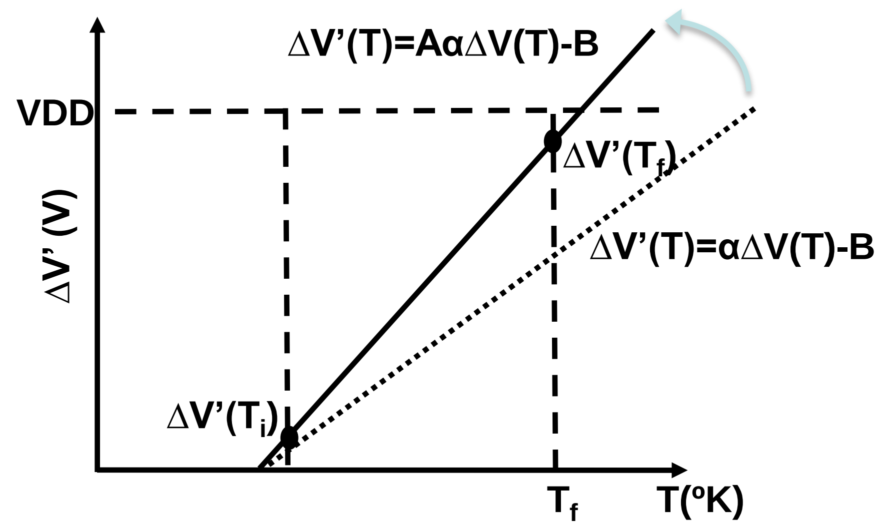
Future work (Temperature measuring system)

For an input range of 1.2V and r=10:

Temperature range	$\Delta V'(T_i)$ (V)	Percentage of input range used
Ti=-55ºC Tf=125ºC	0.139	51.5% of VDD
Ti=-20ºC Tf=70ºC	0.198	29.9% of VDD

Low percentage. How can the percentage of input range used be increased?



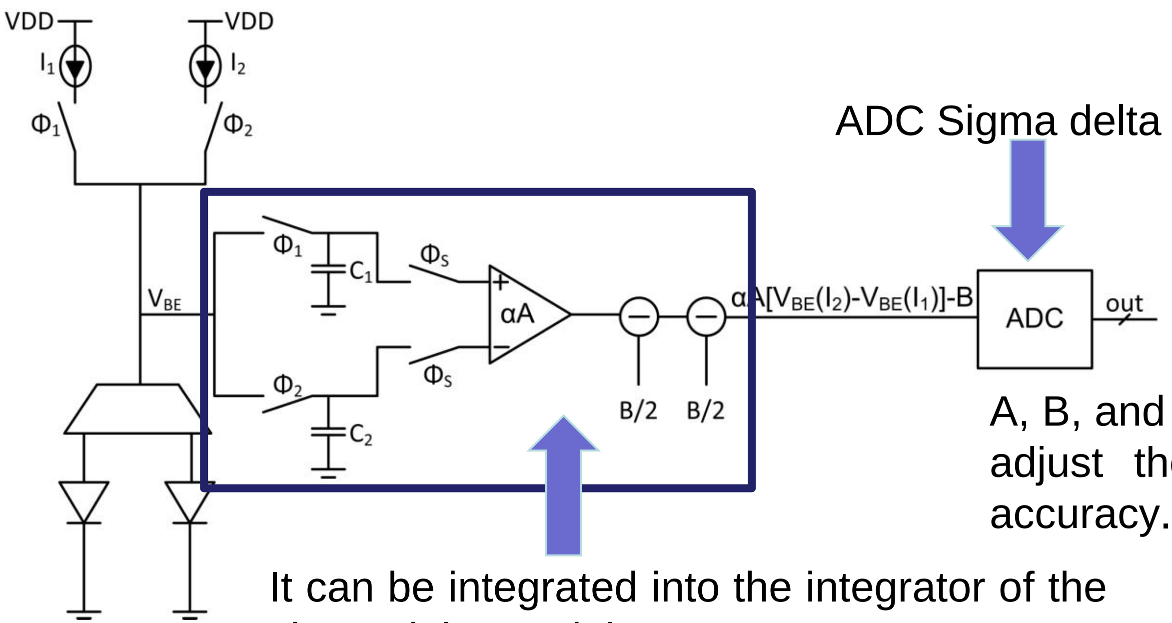


Future work (Temperature measuring system)

$$\Delta V'(T) = \alpha A \frac{K}{q} \ln(r) T - B$$

transformation allows to increase the input range percentage up to a 90% for a given temperature range.

Proposed circuit:



ADC Sigma delta modulator

A, B, and α programmable in order to adjust the temperature range and accuracy.

It can be integrated into the integrator of the sigma delta modulator ADC

Conclusions

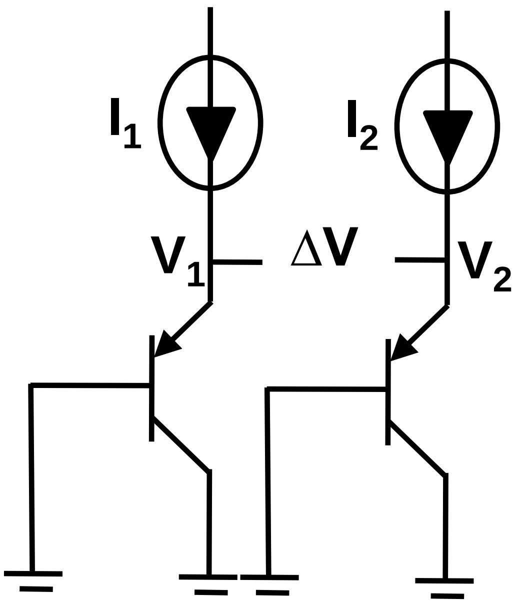
Conclusions

- Development of an independent temperature current source, an 8 bit DAC output current, a 10-b ADC converter and a temperature measuring system in IBM 90 nm.
- Developed circuits successfully integrated into DHP 0.2 chip.
- DHP 0.2 sent to fabricate late May 2011 and expected reception late November 2011.
- Cancellation of IBM 90 nm technology through MOSIS.
- A new technology has been chosen for future development (TSMC 65 nm).
- Moving to 65 nm implies redesign of every analog module.
- Redesign of the independent current source and 8-bits DAC output current in TSMC 65 nm finished in October 2011. Modules sent to fabricate.
- Temperature measuring system proposed by Bonn offers low accuracy (2 ºK as much). Redesign of the temperature measuring system to improve the accuracy to 0.5 ºK. Programmable accuracy and temperature range.

Additional slides

Future work (Temperature measuring system)

Temperature measurement



$$\Delta V = V_1 - V_2 = \frac{nKT}{q} \ln\left(\frac{I_{E1}}{I_{E2}} \frac{I_{SE2}}{I_{SE1}}\right)$$

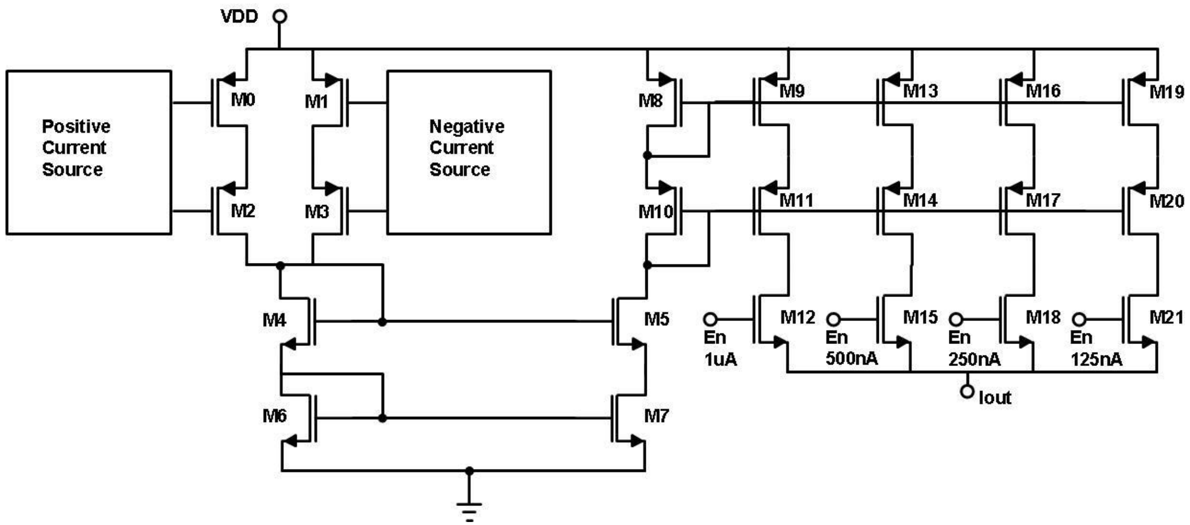
If β_F is constant then $I_{SE1} = I_{SE2}$

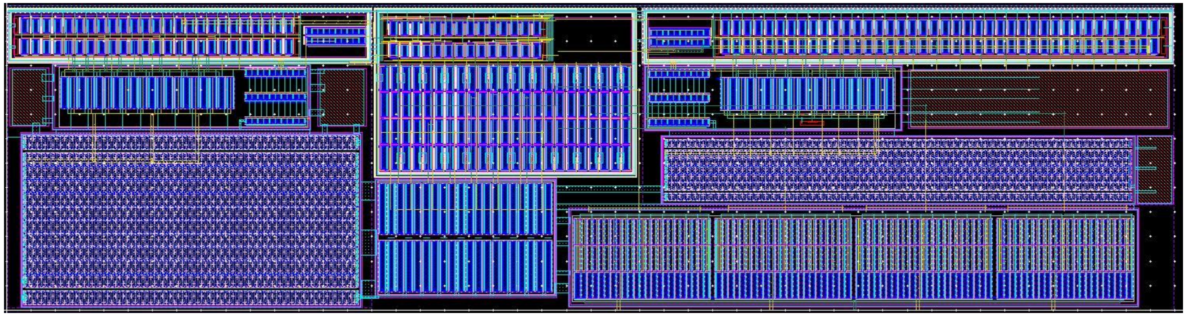
$$\Delta V = V_1 - V_2 = \frac{nKT}{q} \ln\left(\frac{I_{E1}}{I_{E2}}\right)$$

$$n = \frac{qV_1 - V_2}{KT}\left(\ln\left(\frac{I_{E1}}{I_{E2}}\right) + \ln\left(\frac{I_{SE2}}{I_{SE1}}\right)\right)$$

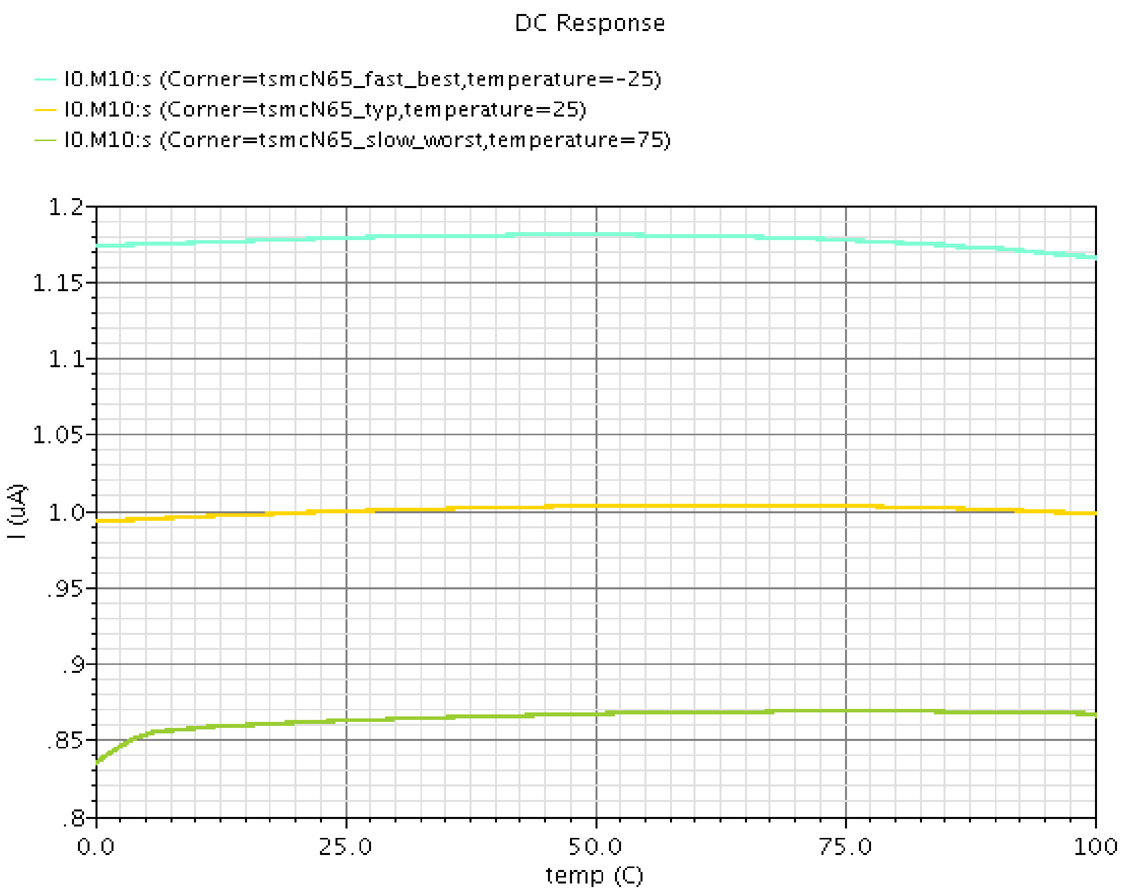
β_F must be constant !

Current source

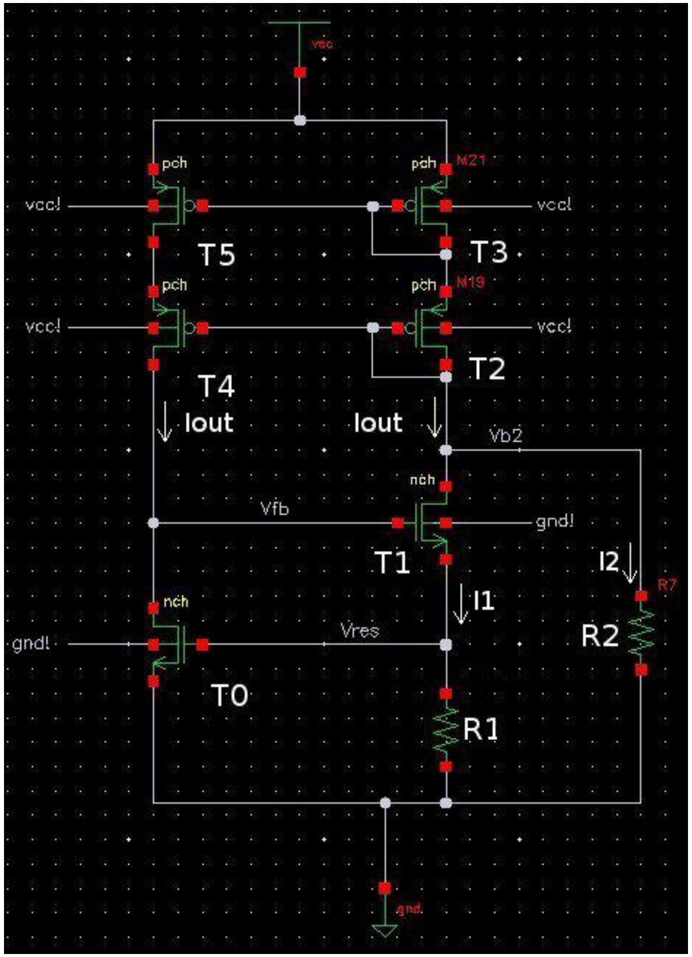


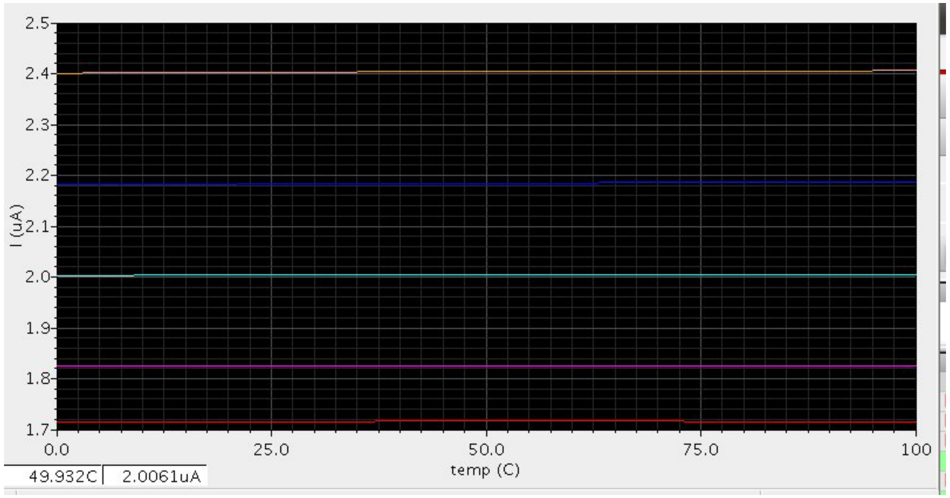


Current source

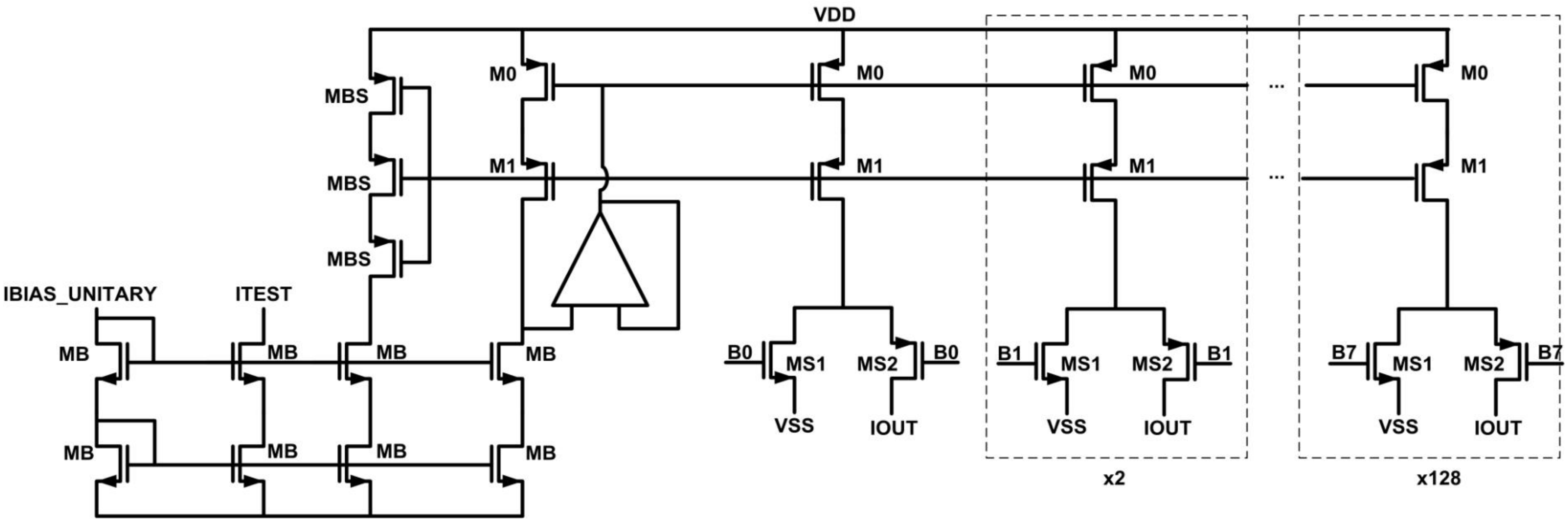


Current source





Current source



Current source

Corner	I@0V	I@900mV	I@950mV	I@1V
Slow	1.0039 µA	999.649 nA	999.331 nA	998.01 nA
Typical	1.0044 µA	999.757 nA	999.23 nA	996.374 nA
Fast	1.0065 µA	999.67 nA	998.557 nA	993.592 nA

Corner	I@0V	I@900mV	I@950mV	I@1V
Slow	255.31 µA	255.2 µA	255.12 µA	254.73 µA
Typical	255.32 µA	255.2 µA	255.06 µA	254.26 µA
Fast	255.29 µA	255.14 µA	254.86 µA	253.43 µA

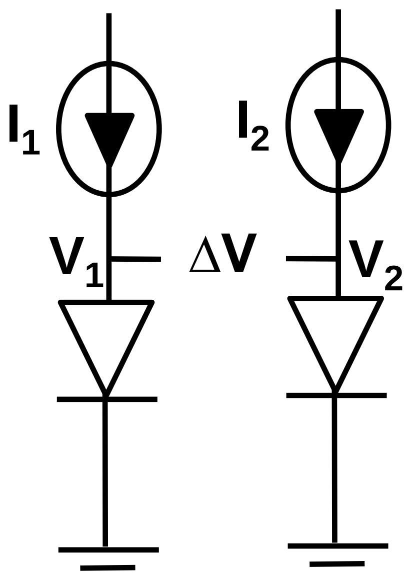
	Value (at 27ºC)
Static power consumption	312 µW
Area	150 µm x 110 µm
Ouput current range (ideal)	0-255
Maximum ouput voltage (for output currents of 0- 255 µA)	970 mV

Temperature measurement

Diode I-V characteristic

$$I_1 = I_S\left(e^{\frac{qV_1}{nKT}} - 1\right) \quad \xrightarrow{\text{for } V_{BE} >> KT/q} \quad I_1 \approx I_S e^{\frac{qV_1}{nKT}} \quad \longrightarrow \quad V_1 = \frac{KT}{nq}\ln\left(\frac{I_1}{I_S}\right)$$

Temperature measurement



$$\Delta V = V_1 - V_2 = \frac{nKT}{q}\ln\left(\frac{I_1}{I_2}\right)$$

VPTAT

(Voltage Proportional To Absolute Temperature

$$T = \frac{q}{nK}\frac{V_1 - V_2}{\ln\left(\frac{I_1}{I_2}\right)}$$

DHP 0.2 chip (UB contribution)