

Contributions to the ATLAS Readout Electronics for the HL-LHC

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The High-Luminosity LHC (HL-LHC) is a major upgrade of the LHC planned for 2026. The HL-LHC will increase the instantaneous luminosity by a factor of 5 compared to the current LHC with a pileup close to 200 collisions per bunch interaction. The ATLAS Phase-II upgrades will accommodate the subdetectors and data acquisition system to the new radiation levels and increased data bandwidths imposed by the HL-LHC.

This contribution presents the design and first results of the Compact Processing Modules for the ATLAS Tile Calorimeter (TileCal). The TileCal Phase-II Upgrade will imply the complete replacement of the readout electronics system. In this new readout architecture, the on-detector electronics will stream detector data to 128 Compact Processing Modules (CPM) operated in 32 ATCA carrier blades located in the counting rooms. The CPM is an Advanced Mezzanine Card (AMC) form factor board, which is responsible for the detector data acquisition, LHC clock distribution, cell energy reconstruction and interface with the ATLAS Trigger and DAQ systems. Each CPM is equipped with 8 Samtec FireFly modules connected to a Xilinx Kintex UltraScale FPGA for the high-speed interface with the on-detector and TDAQ systems; and one Artix 7 FPGA for slow control functionalities.

In addition, this contribution also presents the status and design of the End-Cap BusTapes for the Inner Tracker silicon strip detector (ITk strips) at the HL-LHC.

The EC BusTape is a two-layer flexible PCB using Kapton, which will be co-cured onto the mechanical structure of the EC (Petals). This flexible board provides a high-speed communication path for ITk strip modules for the sensor readout and TTC (Timing, Trigger, and clock) reception through the End-of-Substructure card. In addition, this board also distributes low voltage, high voltage and control signals to the PowerBoards. The flexible PCBs are designed to have high reliability, low voltage drops, and reduced mass.

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