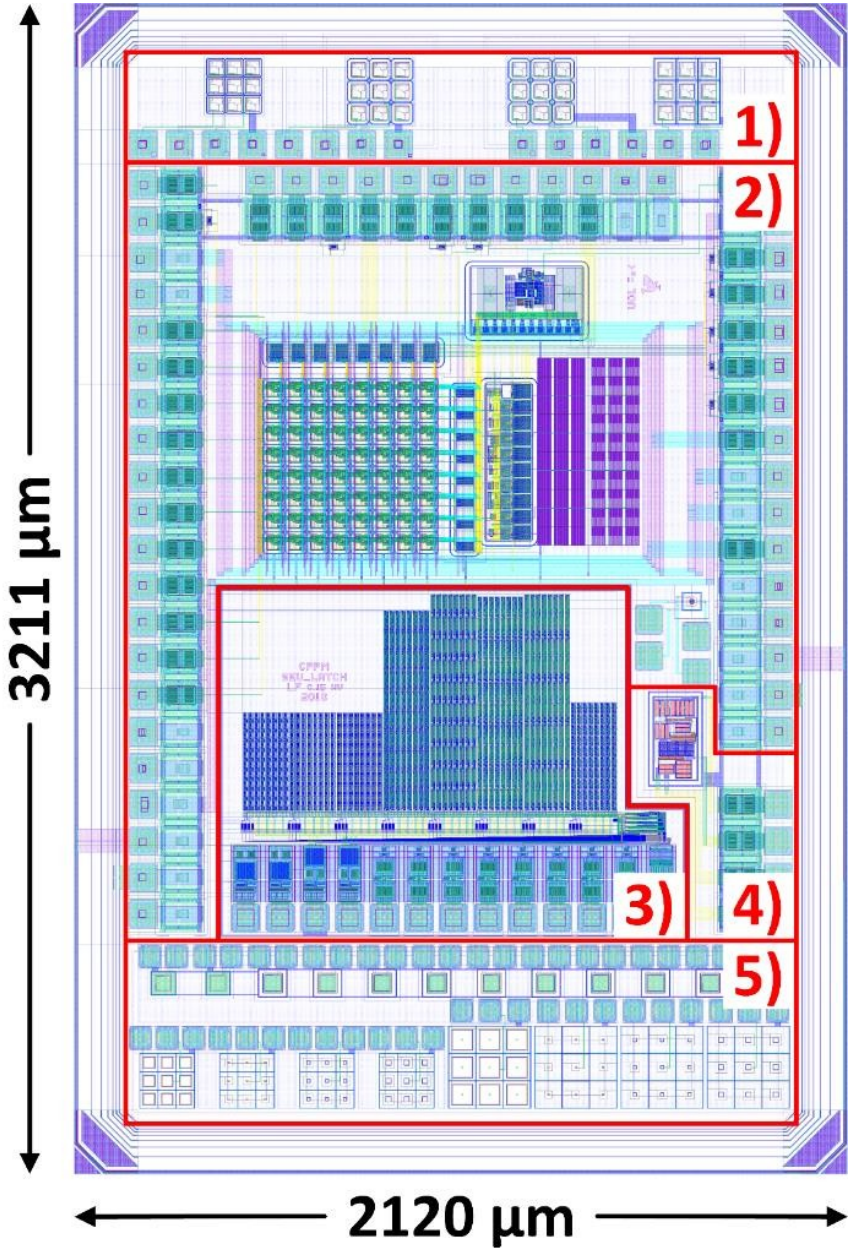
RD50-MPW2 device main characteristics

Dr. Ricardo Marco Hernández

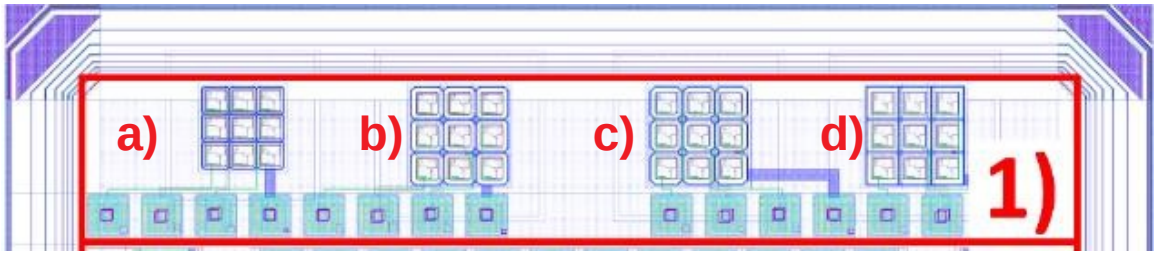
RD50-MPW2 floor plan

- Tests structures with depleted CMOS pixels (1).
- Matrix of depleted CMOS pixels with analog readout (2).
  - 8 x 8 pixels.
  - 60 µm x 60 µm pixel area.
  - Analog readout embedded in the sensing area.
- SEU tolerant memory array (3).
- Bandgap reference voltage (4).
- Test structures with SPADs and depleted CMOS pixels (5).



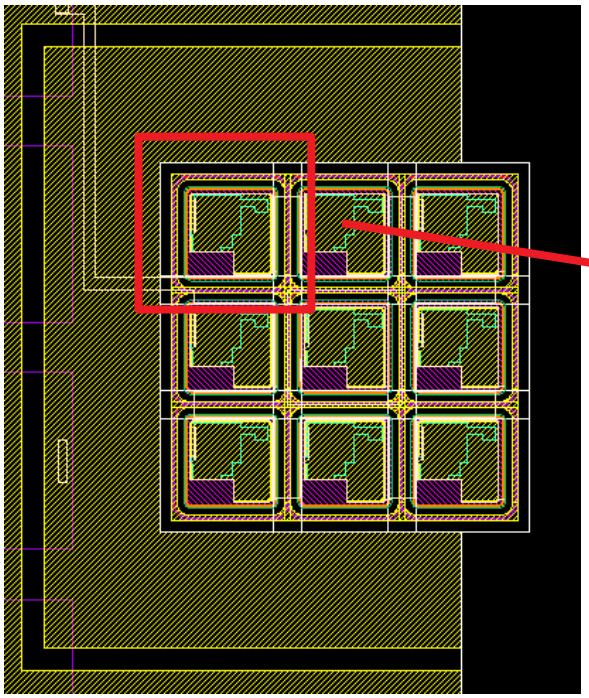
Matrices of 3x3 depleted CMOS pixels

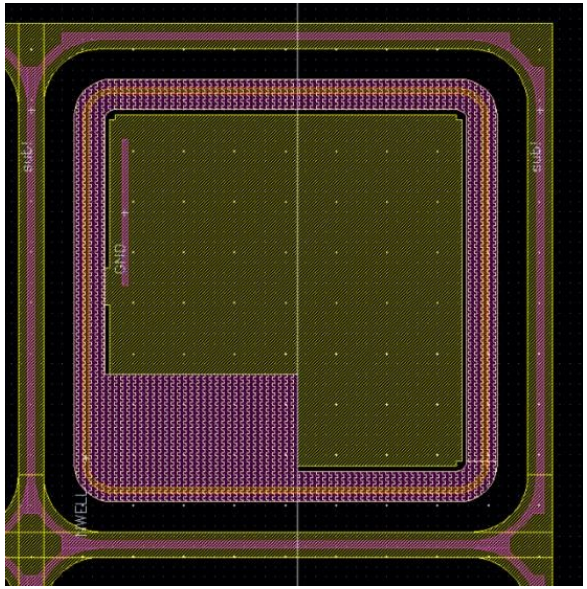
- 8 external pixels are shorted together.
- I/O pads for central and external pixels.
- No electronics in the pixels.



- Matrix (a):
  - Pixel size 50 µm x 50 µm.
  - P-substrate/deep n-well spacing 3 µm.
  - Corners rounded.
- Matrix (b):
  - Pixel size 60 µm x 60 µm.
  - P-substrate/deep n-well spacing 8 µm.
  - Corners rounded.
- Matrix (c):
  - Pixel size 60 µm x 60 µm.
  - P-substrate/deep n-well spacing 8 µm.
  - Corners chamfered.
- Matrix (d):
  - Pixel size 60 µm x 60 µm.
  - P-substrate/deep n-well spacing 8 µm.
  - Corners squared.

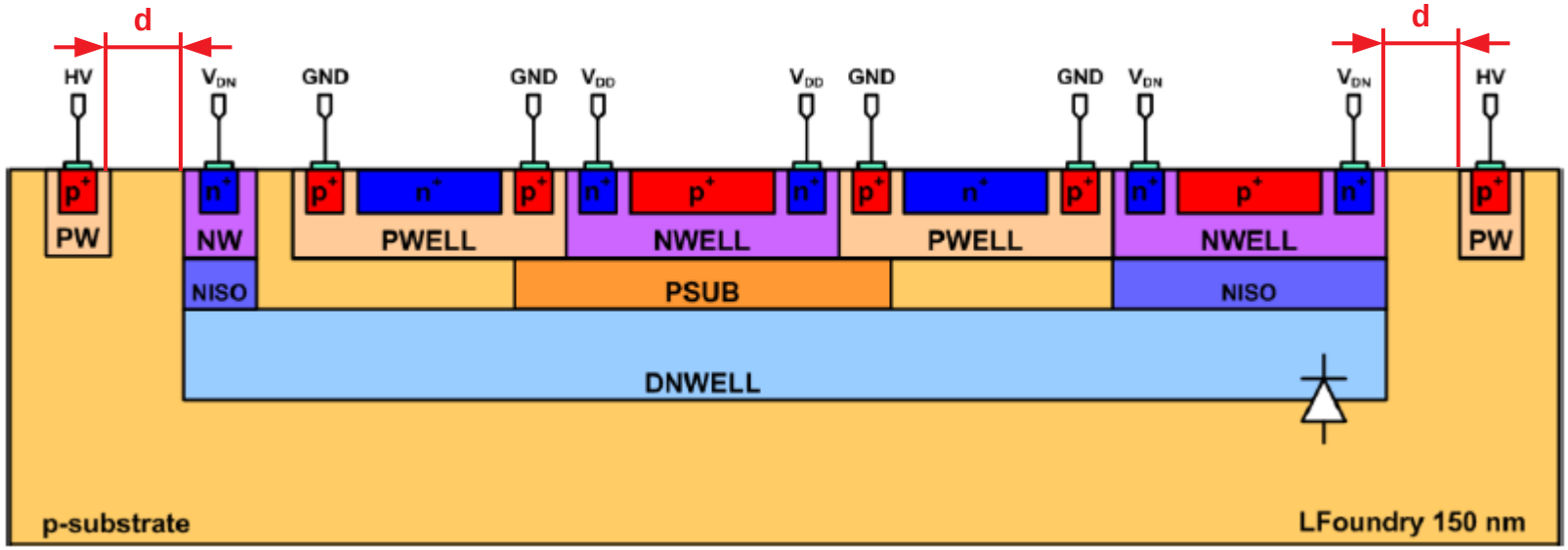
RD50-MPW2 test structures





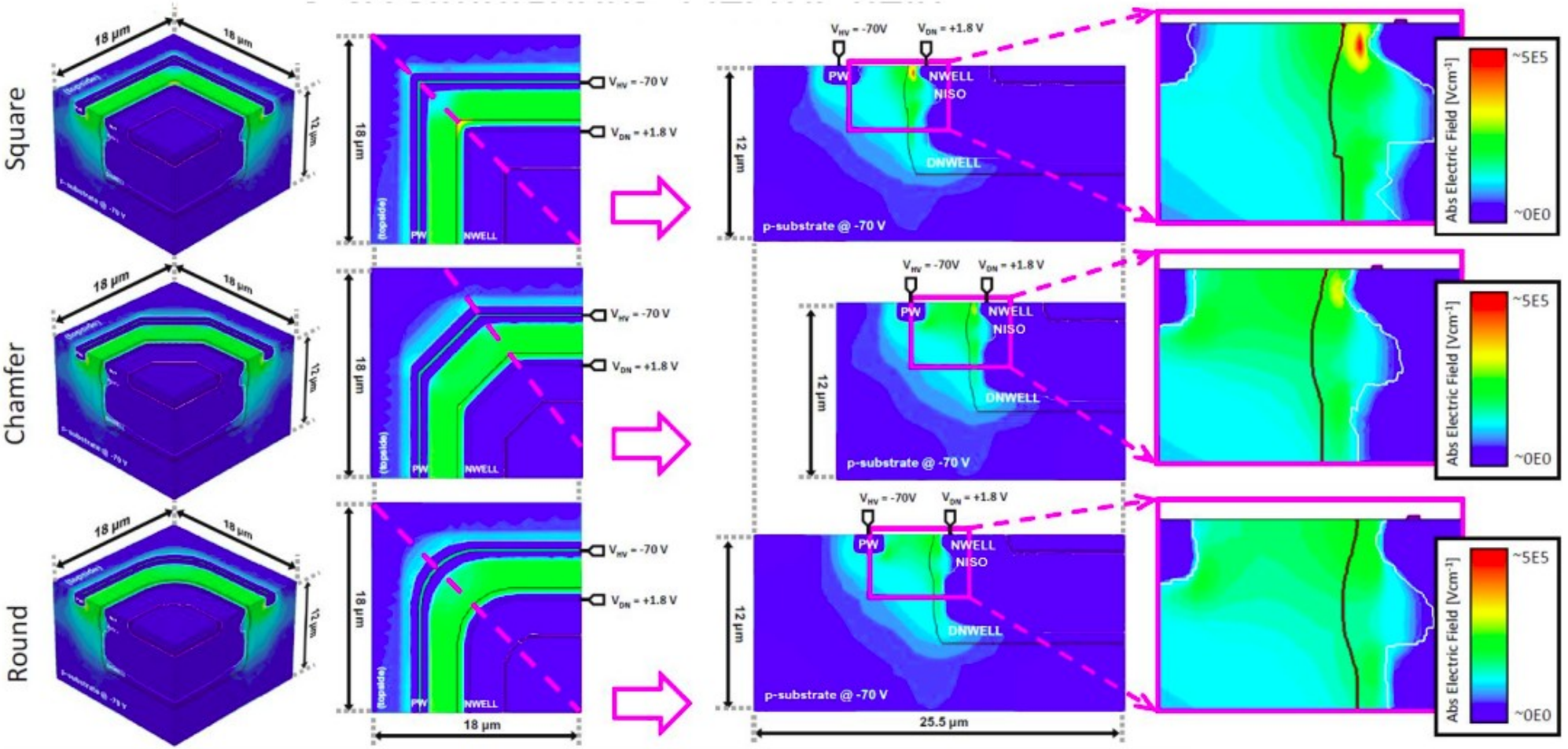
NWELL

PWELL

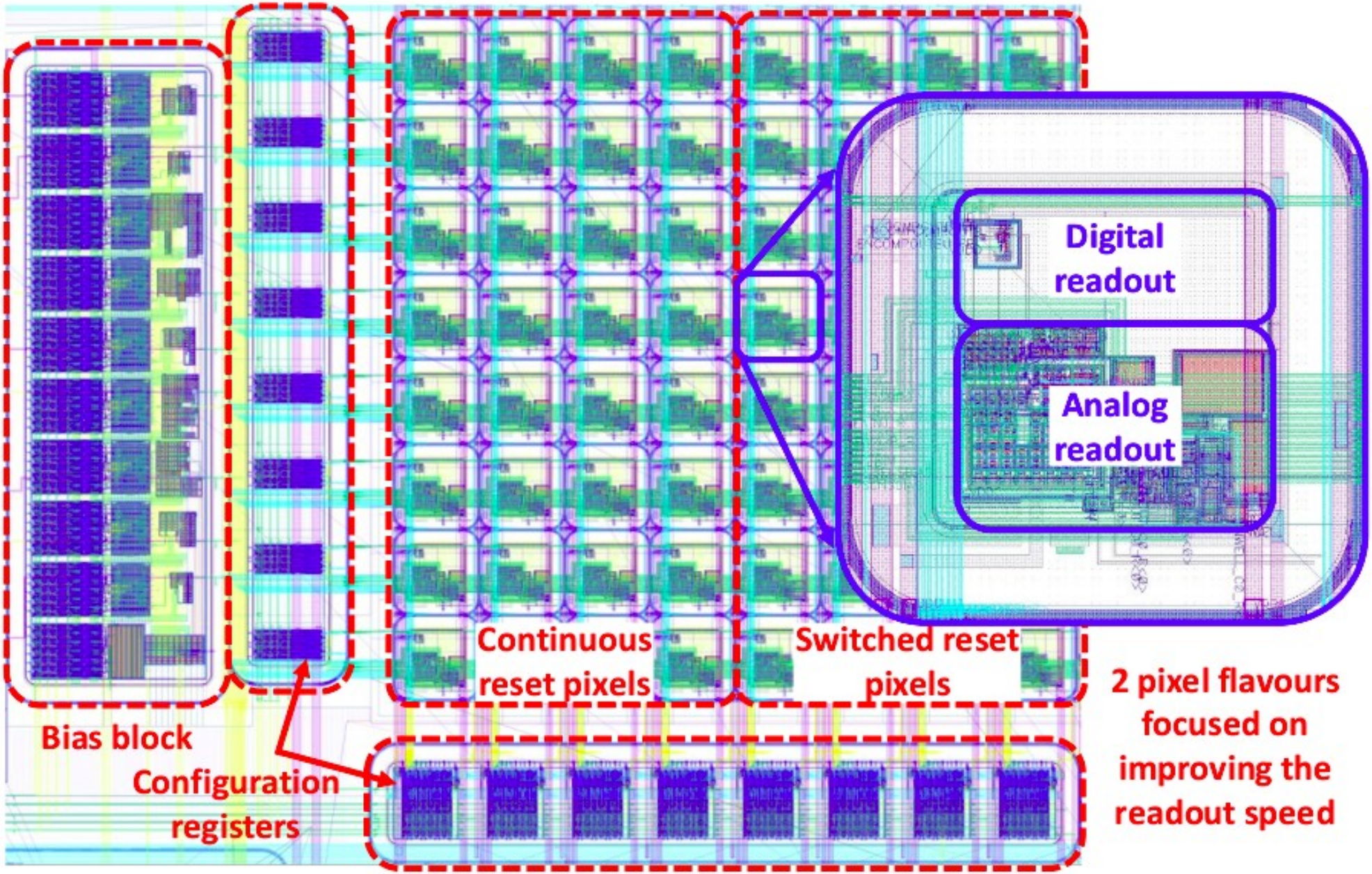


Electric field as a function of corner geometry in pixel

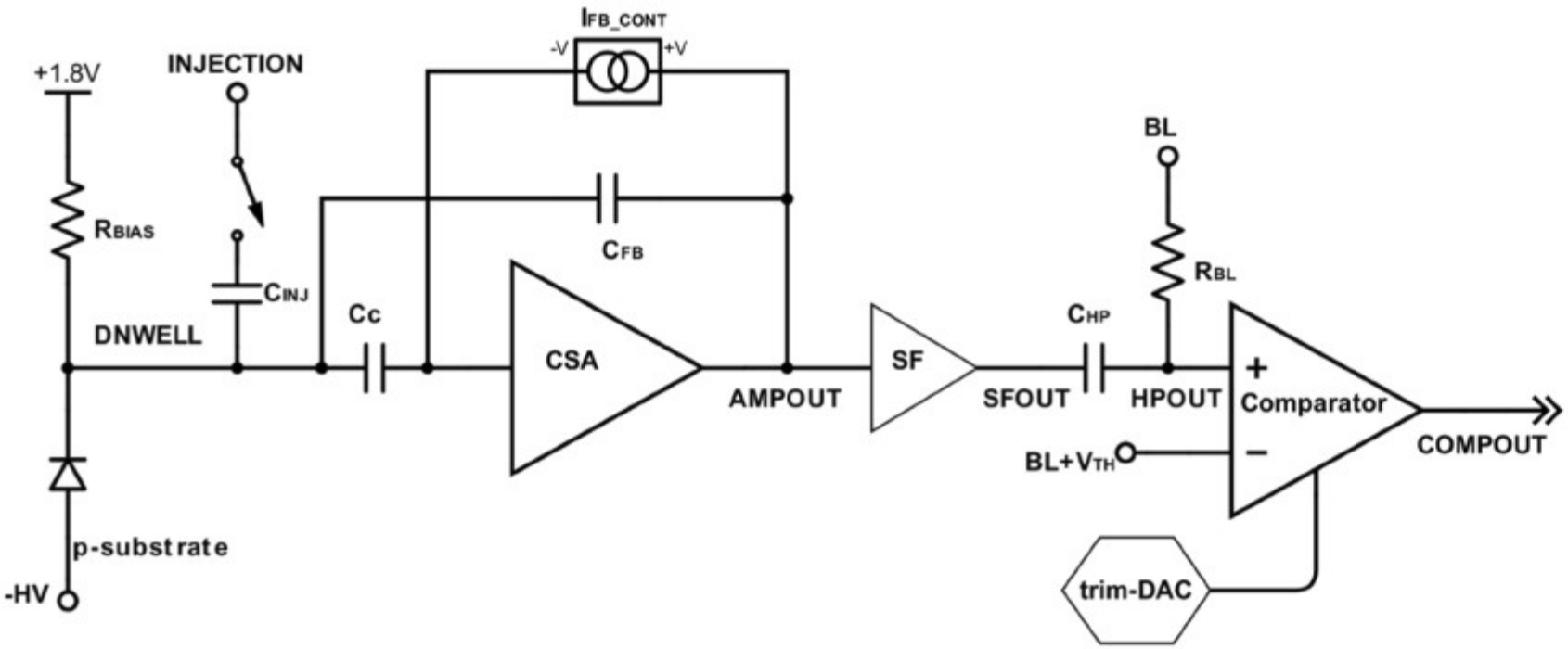
- TCAD 3D simulations confirm better electric field distribution when using rounded corner geometries.



Matrix of depleted CMOS pixels

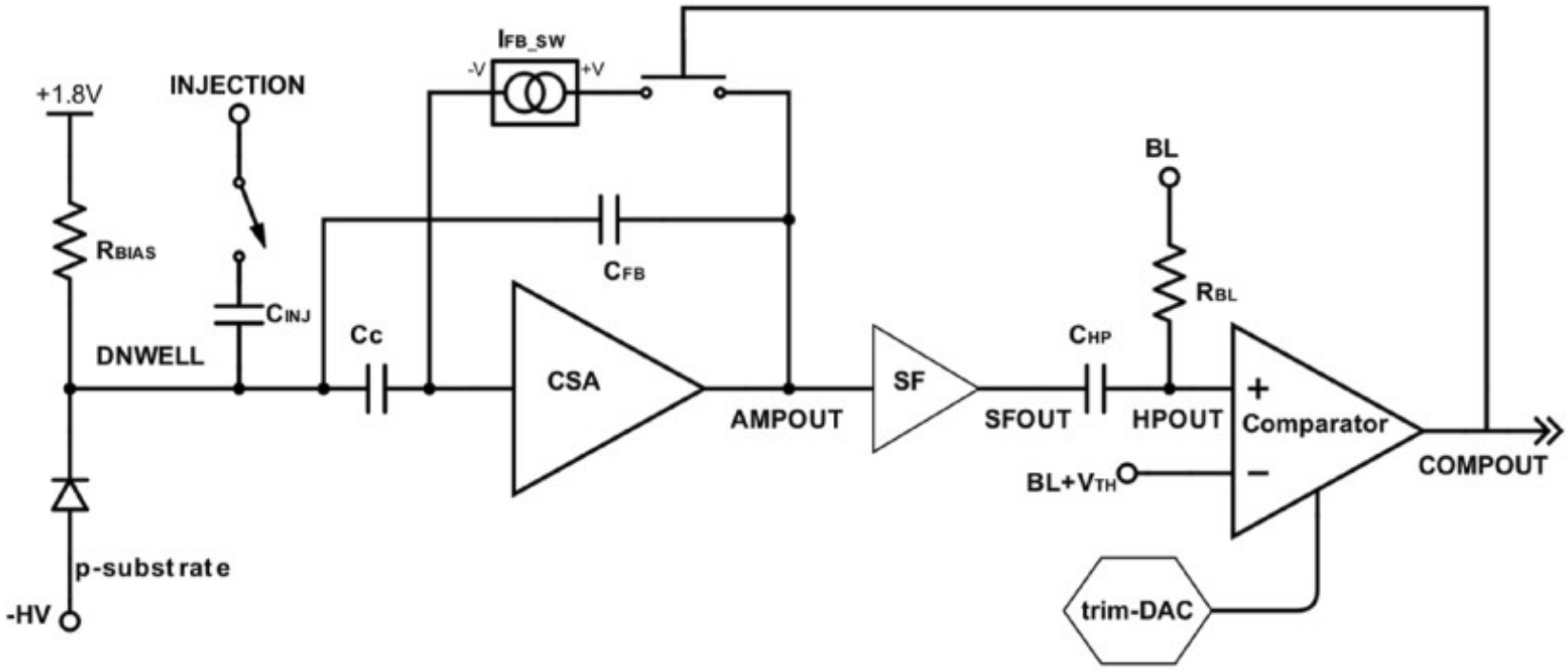


Continuous reset pixel



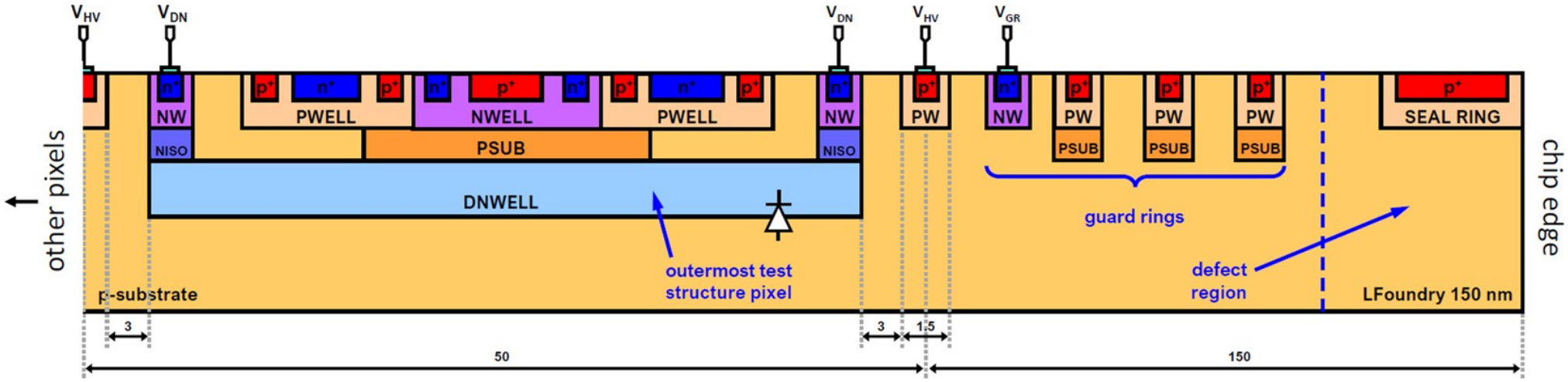
- Amplified pixel signal:
  - Rising edge controlled by speed of CSA.
  - Falling edge controlled by CSA feedback capacitance and current: constant current so linear discharge

Switched reset pixel



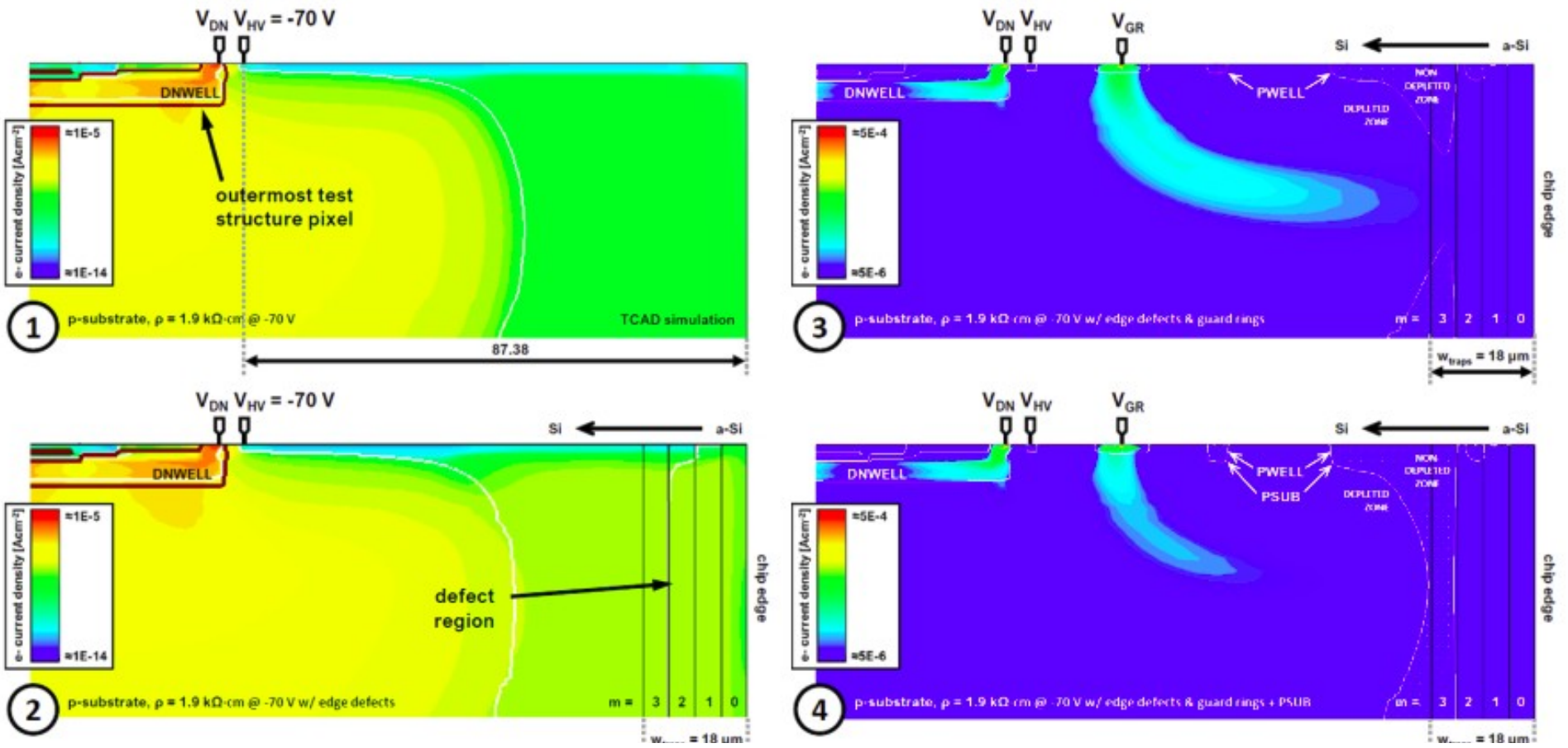
- Amplified pixel signal:
  - Rising edge controlled by speed of CSA.
  - Falling edge controlled by CSA feedback capacitance and current: COMPOUT controls the switch that resets the pixel (non-linear discharge).

RD50-MPW2 edge guard and seal rings



- Defects in silicon lattice due to dicing can become significant.
- Leakage current increases when pixel depletion region is near the defect region.
- N-type guard ring added as safeguard to “collect” leakage current.
- P-type guard rings added to reduce “lateral” depletion. PSUB to further reduce lateral depletion.

Edge effects



- TCAD simulation of edge effects: current density shown.
  1. Without effects (ideal case).
  2. With defects and no guard rings.
  3. With defects, and NWELL and PWELL guard rings.
  4. With defects, and NWELL and PWELL with PSUB guard rings.

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