GOBIERNO DE ESPAÑA
MINISTERIO DE CIENCIA E INNOVACIÓN

Ciemat
Centro de Investigaciones Energéticas, Medioambientales y Tecnológicas

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CALICE

AIDA 2020

ILD

Calorimetry Activities at CIEMAT

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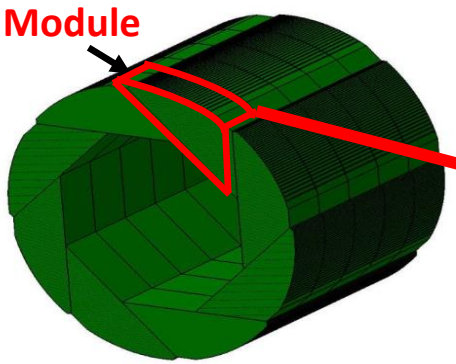
CIEMAT

Jornadas de la red española de futuros colisionadores. IFT Madrid. 10-11 February 2020

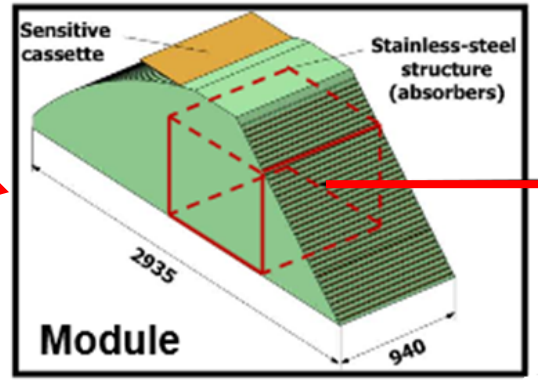
Semi-Digital Hadronic Calorimeter (SDHCAL) CALICE and ILD

The SDHCAL-GRPC is one of the two HCAL options based on PFA and proposed for **ILD of ILC**.
Modules are made of **GRPC** (**G**lass **R**esistive **P**late **C**hambers) equipped with **semi-digital, power-pulsed electronics** readout and placed in **self-supporting mechanical** structure to serve as absorber as well.

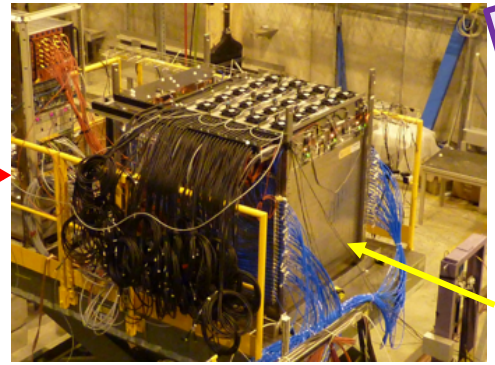
SDHCAL ILD barrel



SDHCAL ILD module



SDHCAL 1.3m^3 prototype



HIGH GRANULARITY CALORIMETER

~ half million of channels

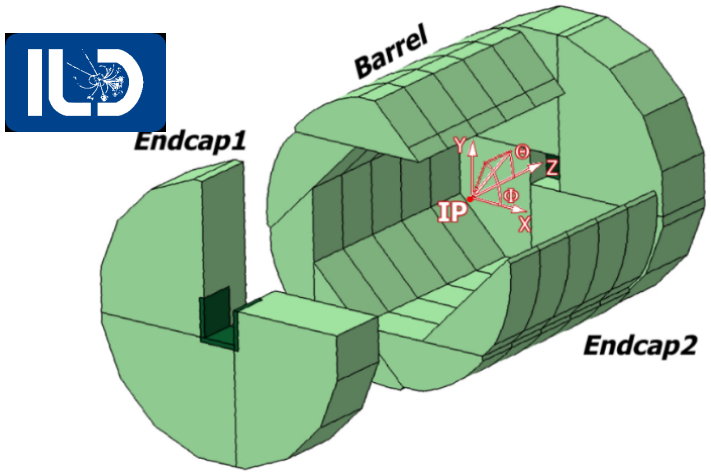
Absorber: Stainless Steel
Active Medium: GRPC
SemiDigital readout. **1cm^2 pads**

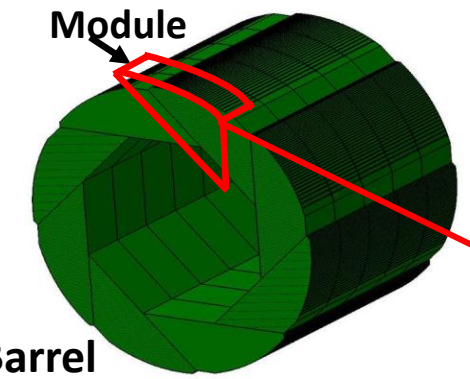
Electronics embeded in the detector

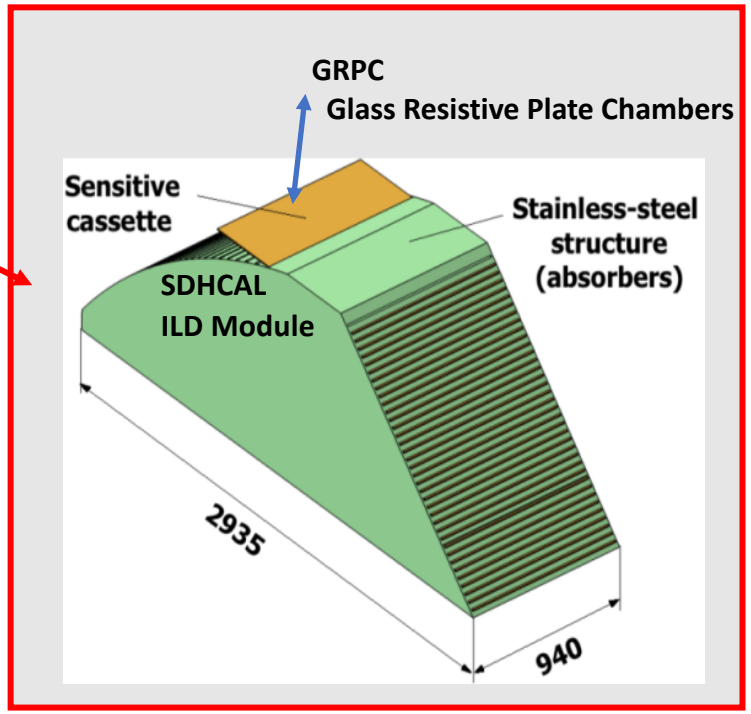
ILD SDHCAL
Plates & GRPCs: up to **~3x1 m^2**
Absorber assembly **Welding**?

~1.3m3 SDHCAL prototype
Plates & GRPCs : **~1x1 m^2**
Absorber assembly: **Bolted**

The new SDHCAL prototype







The ~1m3 prototype built in the past was based of layers of plates absorbers of ~1m2

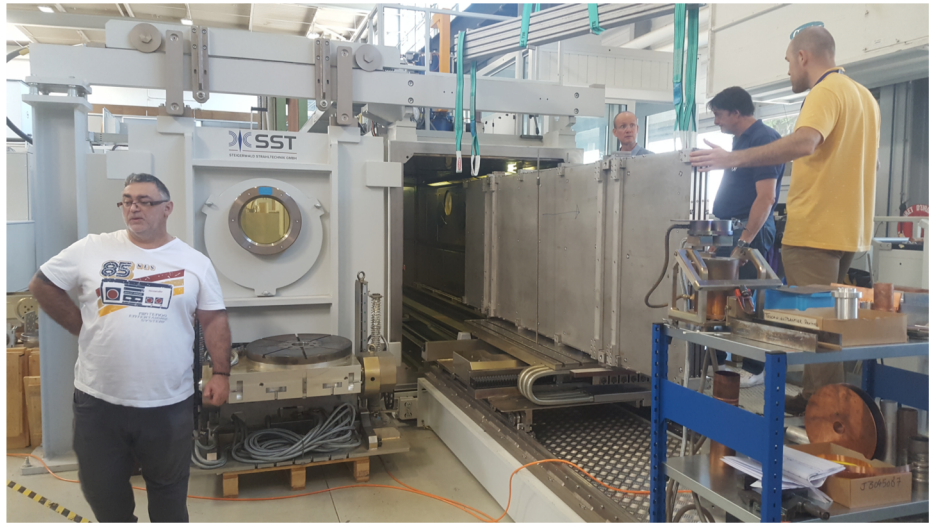
To enlarge them to the maximum size (~3x1m2) expected at ILD, implies new challenges for the detector, embedded electronics and mechanics

The goal

To build a ***new prototype*** ***with a mechanical structure of 4 plates of ~1x3m²*** (assembled with similar procedures to the final one) where inserting large ***RPCs equipped with a new improved electronics.***

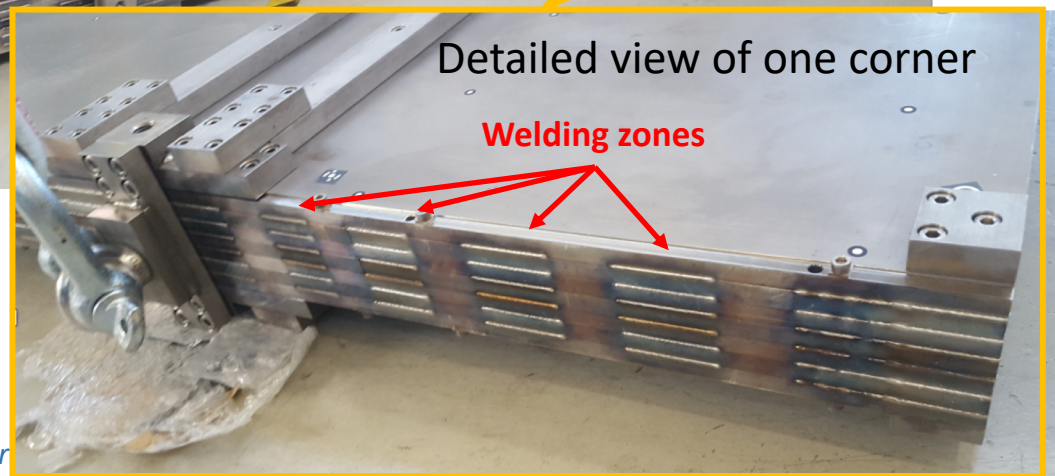
Mechanical developments: Calorimeter absorber

Evaluation of the use of Electron Beam Welding for the assembly of the absorber mechanical structure



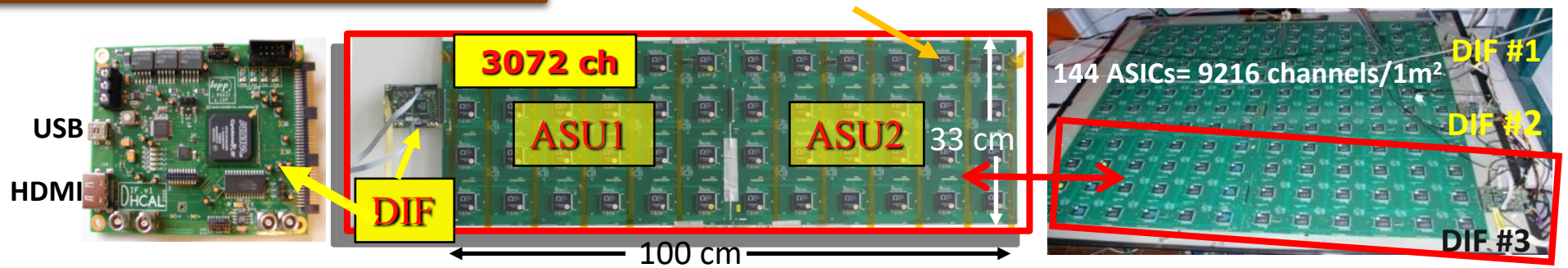
Introduction of the pre-assembled absorber structure inside the EBW machine at CERN

See E. Calvo's Talk



New electronics: ASIC,PCB,DIF

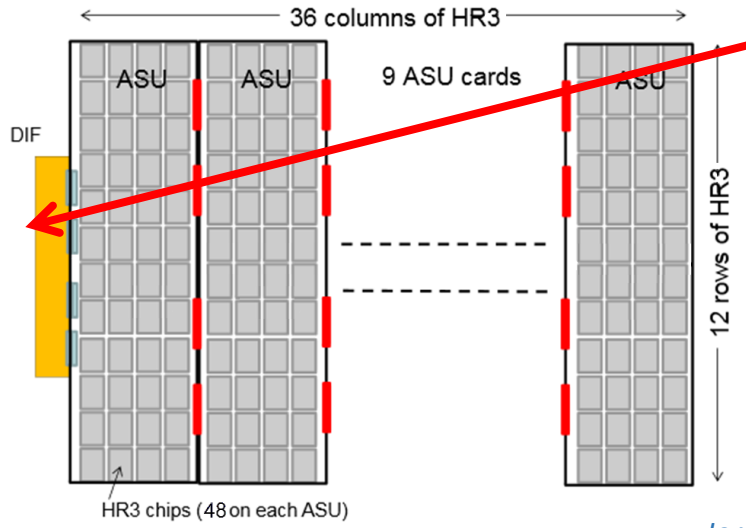
Electronics readout for the 1m³ prototype



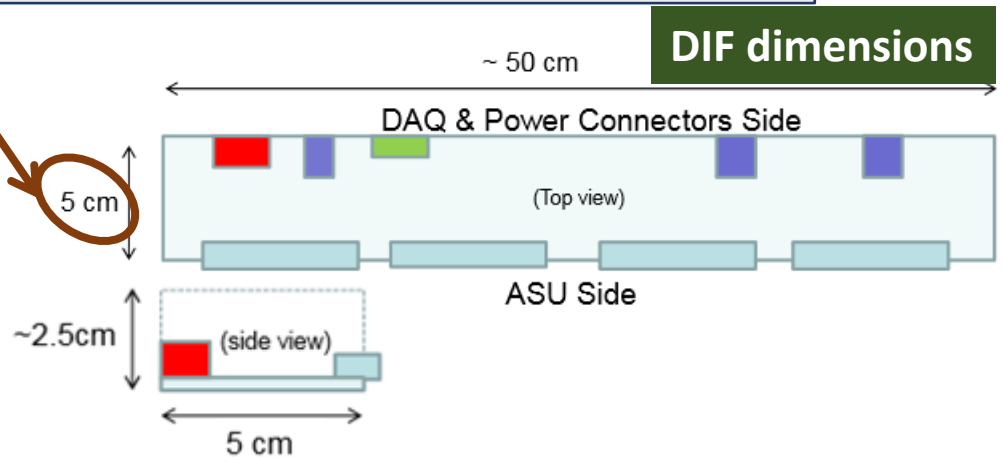
1 DIF for 2 ASU (Active Sensor Unit.- PCB+ASICs) ➔ **3 DIFs for ONE 1m2 GRPC detector**

Electronics readout for the final detector

Only **1 DIF per GRPC (any dimension)** with small dimensions to fit in the **small** space available at the final detector

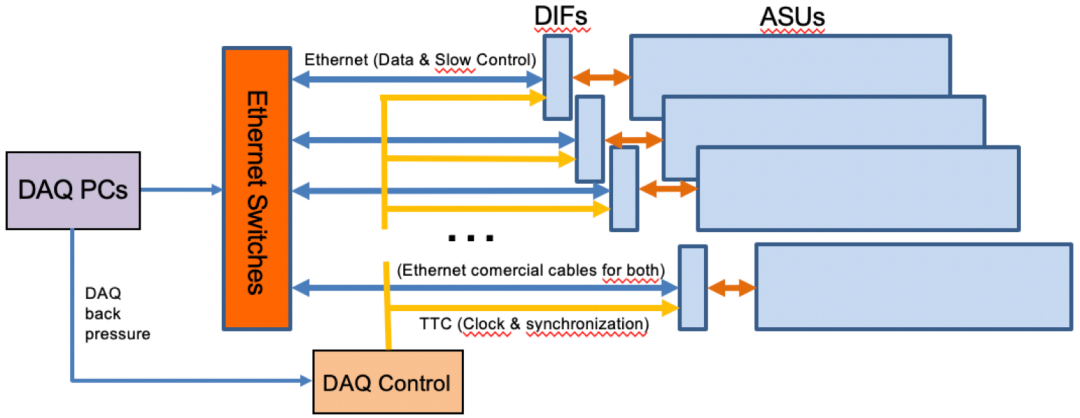


DIF dimensions



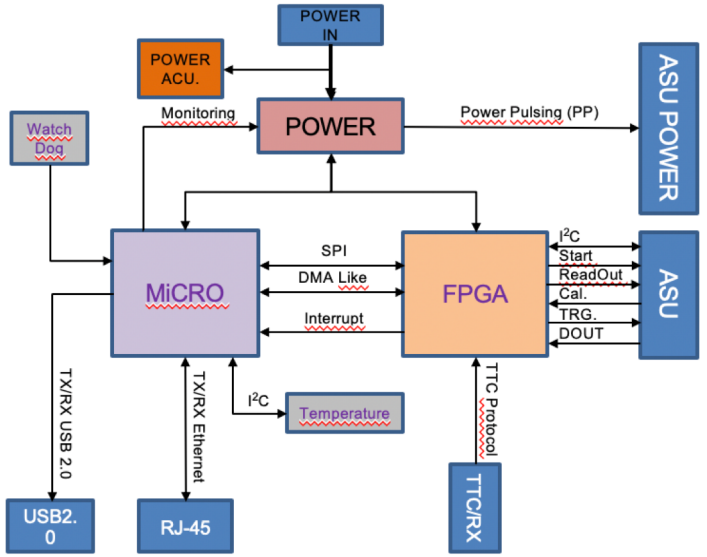
SDHCAL DAQ architecture

A *central PC* collects data from all the *ASUs* (containing de *ASIC chips*) through an *Ethernet switch* acting in such a way as data concentrator and generates the required commands for *ASU* and *DIF* configuration generating at the same time synchronization signal required for a correct data acquisition process.



DIF architecture

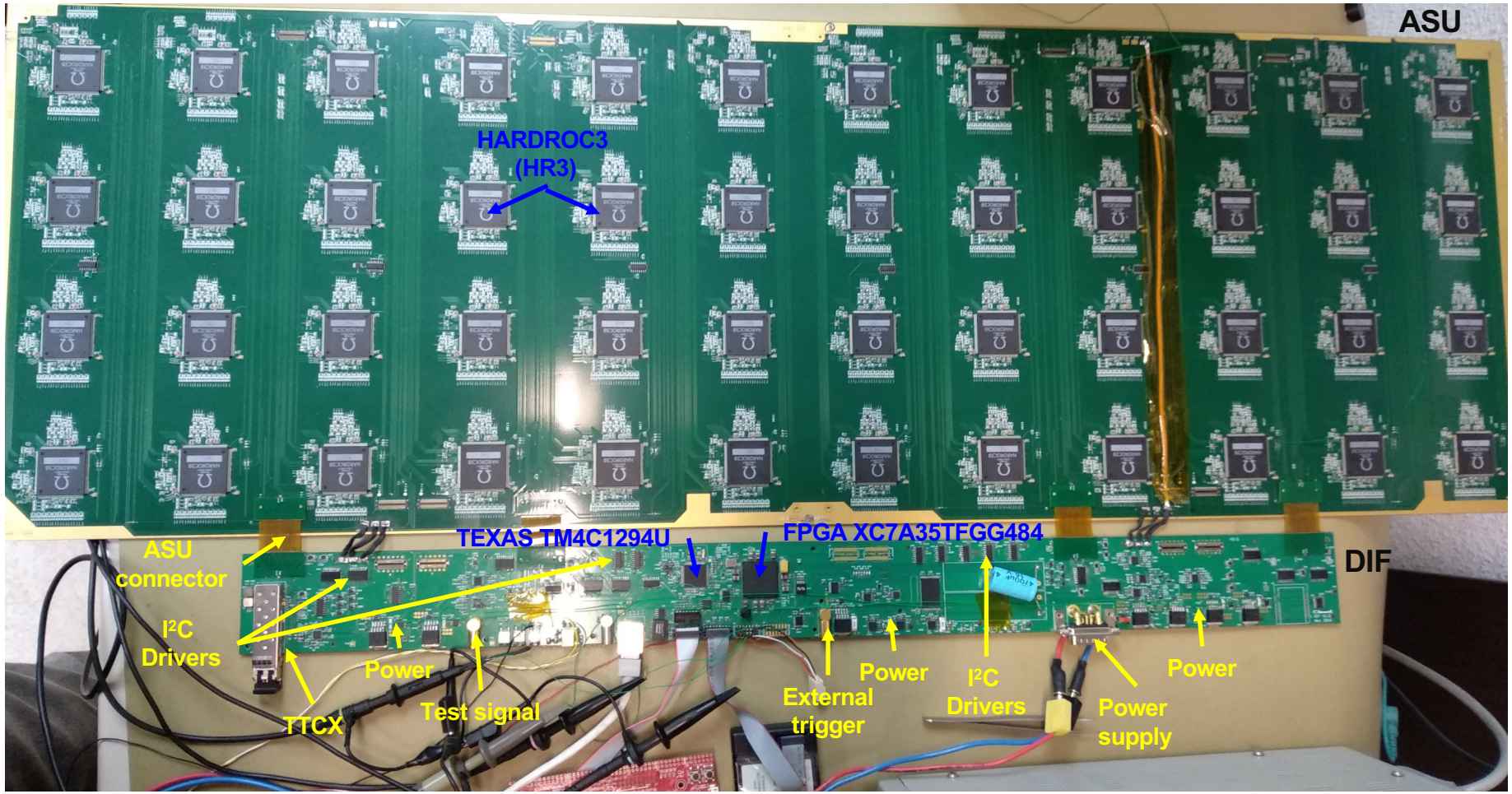
- Only one DIF per plane (instead of **three**)
- DIF handle up to 432 HR3 chips (vs **48 HR2** in previous DIF)
- **Clock and synchronization** by TTC (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**



DIF+ASU under tests

ASU

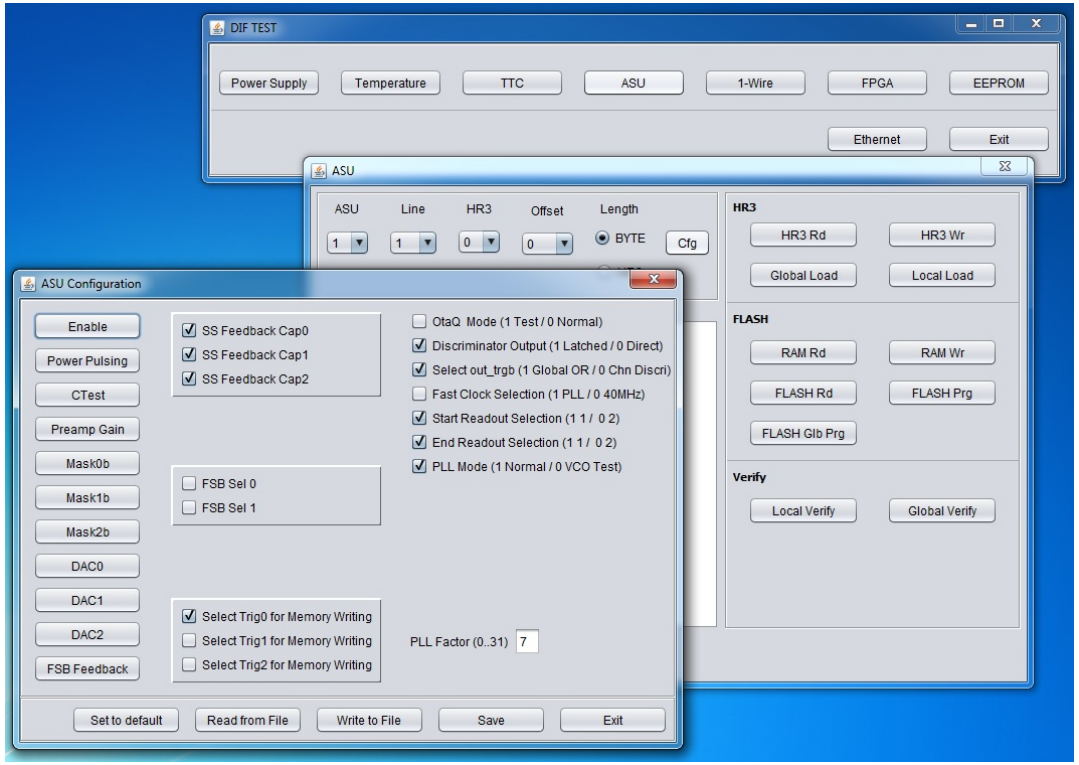
DIF



Java Aplication

➢ **A Java application** has been designed to **test the different functionalities** of the **DIF and ASU** boards.

- The application **communicates with DIF using the Ethernet link.**
- The user can **read and write the registers of the different ICs** (power supply, temperature, TTC) **and those implemented registers using the microcontroller and FPGA**. On the other hand, it is possible to **read and write the registers of the HARDROC and 1wire chips.**



All the functionalities of both boards can be tested using this application

➢ **Another Java application** has been developed to allow the **remote programming** of the **FPGA memory**
Other allowed actions are: blank checking, erasing, etc.

DIF Status

- **Firmware development:**
  - Micro-processor Done
  - FPGA Done except Power Pulsing

- **Functional tests:**

Power	√
FPGA	√
Micro-Processor	√
TTC Synchronization / commands	√ / χ
Power Pulsing (super-cap) / ASU	√ / χ
Old slow control test with ASU	√
I2C slow control test with ASU	√
Data acquisition test with ASU	χ

Remaining tests

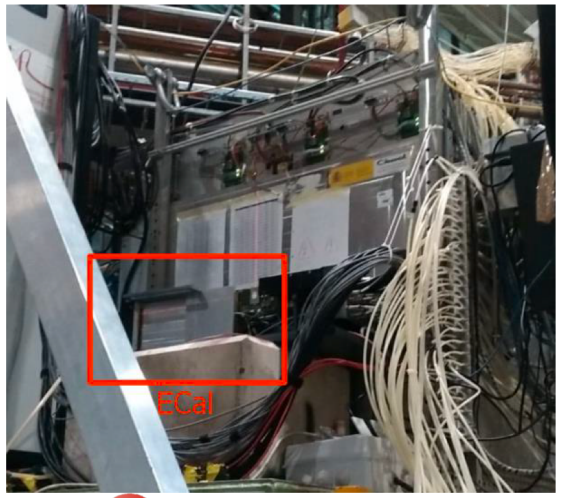
1.Power Pulsing (PP) mode → PP will be tested using one ASU and simulating powering ON the ASICs (beam) and OFF (the rest of the time).

The super-capacitors were tested with an active charge simulating real conditions (5 ms of every 200 ms). Both a resistive and a capacitive charges were used.

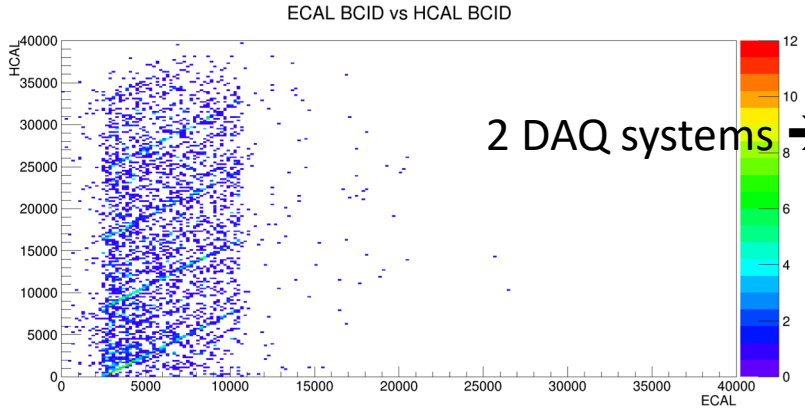
2.Data acquisition → PC-microcontroller and microcontroller-FPGA interfaces have been tested. FPGA-ASU interface tests are being carried out.

3.TTC commands → in the synchronization part.

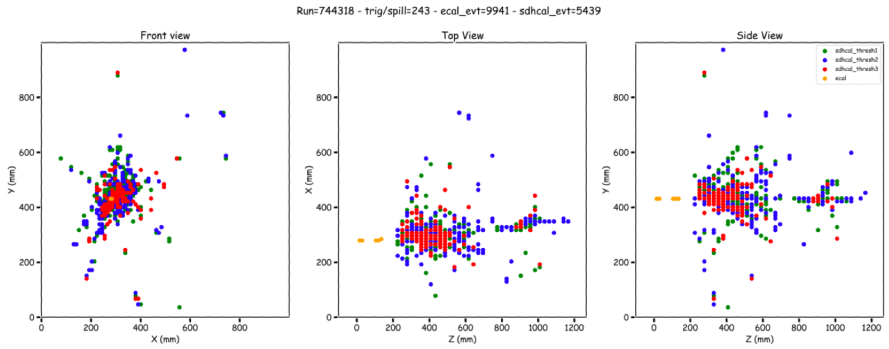
SiECAL + SDHCAL Common tests

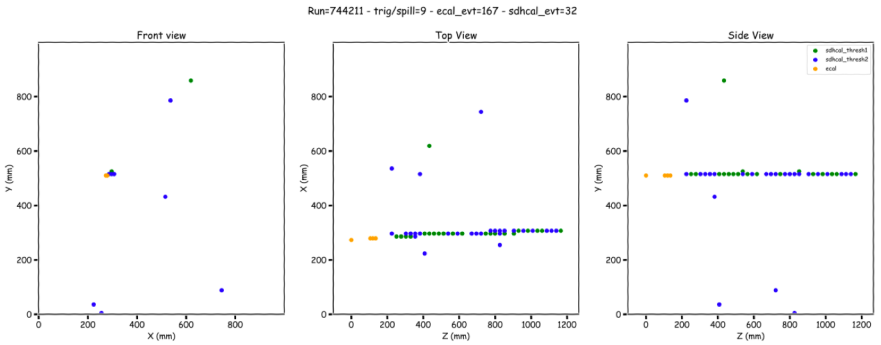


SiECAL details
See A.Irles' talk

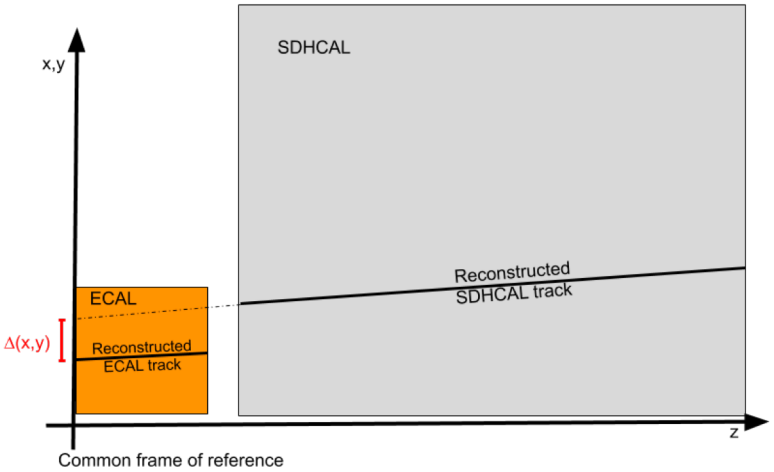


2 DAQ systems ➔ Event synchronization done offline





Alignment between both prototypes needed
Using tracks of muons



Analysis is ongoing
Not public results yet

ILD software/physics studies

- Working on a procedure (and software program) for ***validating SDHCAL Monte Carlo ILD releases/production in the framework of ILCSoft***

  Some ideas using hit multiplicity, longitudinal an radial profiles, reconstructed energy vs MC truth.

  Being also compared with present real data .

  Work ongoing, not yet presented at the ILD

- ***Montecarlo*** studies of ***using the time information*** given for the calorimeter (***5D readout***) in the event identification and reconstruction

  Just starting to dig inside what is available to the code

- Some **Higgs studies** in our ***long term plan (Not started yet)***


THANK YOU FOR YOUR ATTENTION!
ANY QUESTIONS?
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