Belle II VTX CMOS

IFIC

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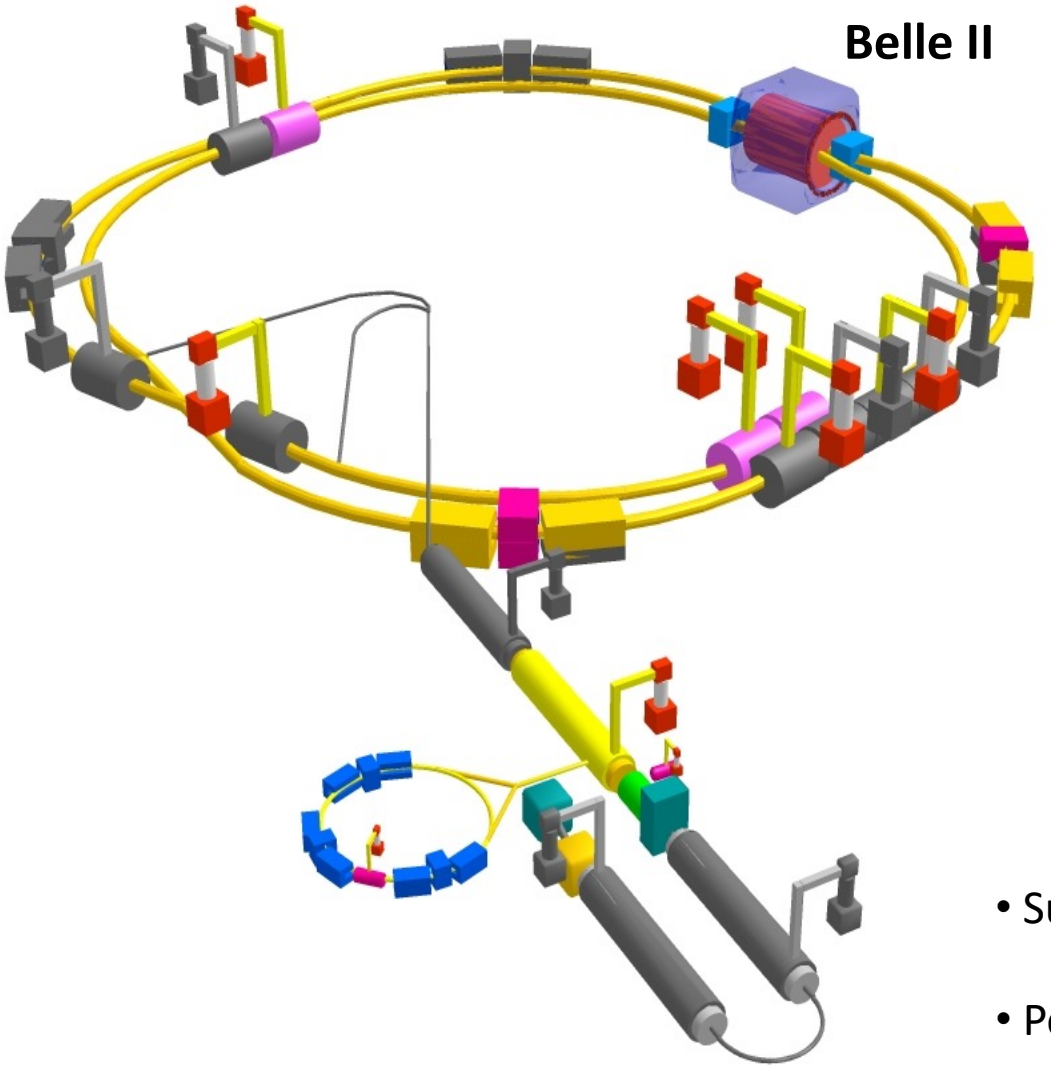
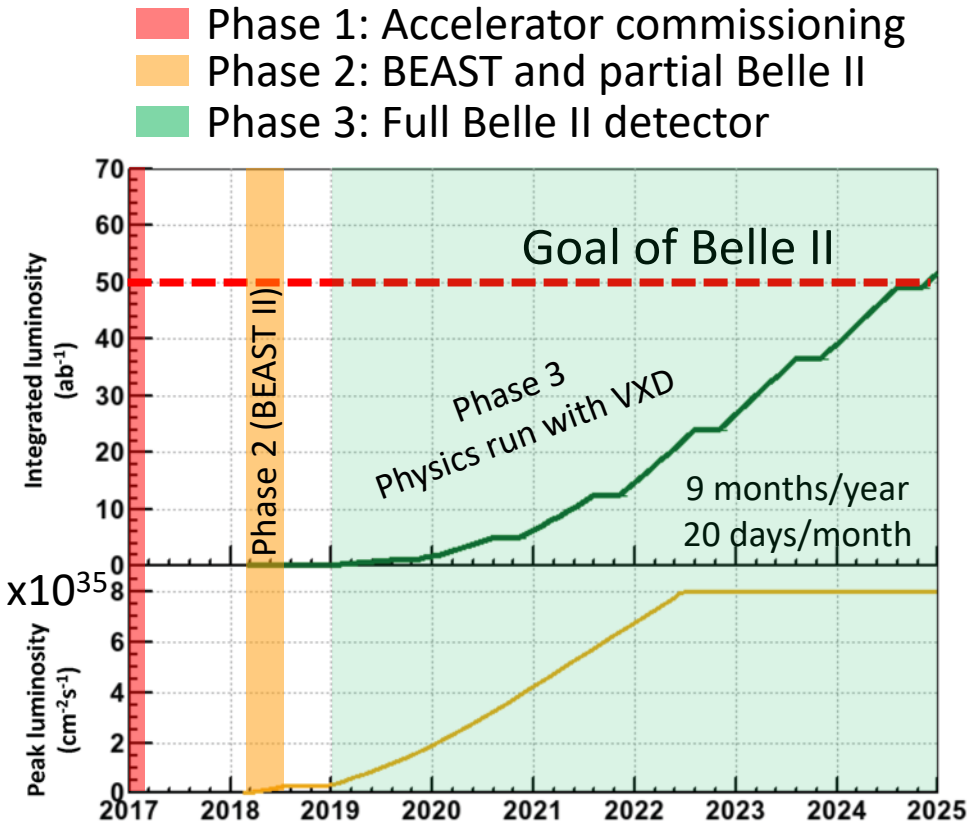
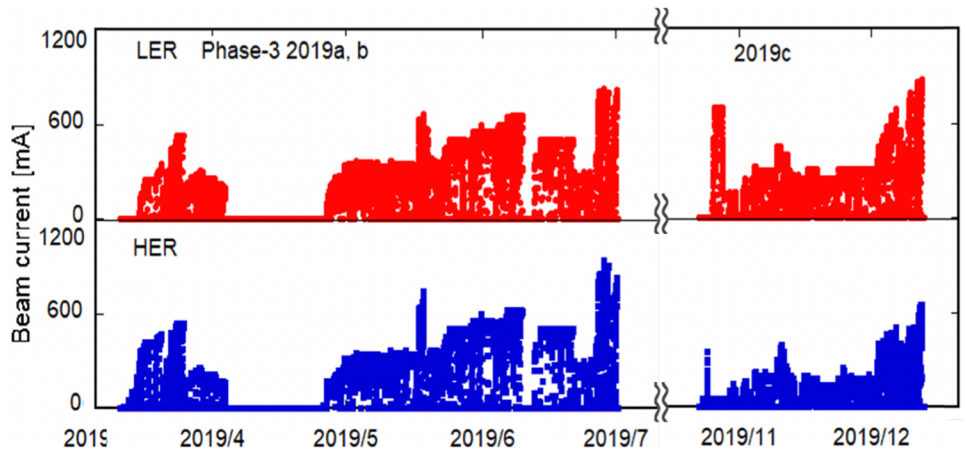
SuperKEKB Operation

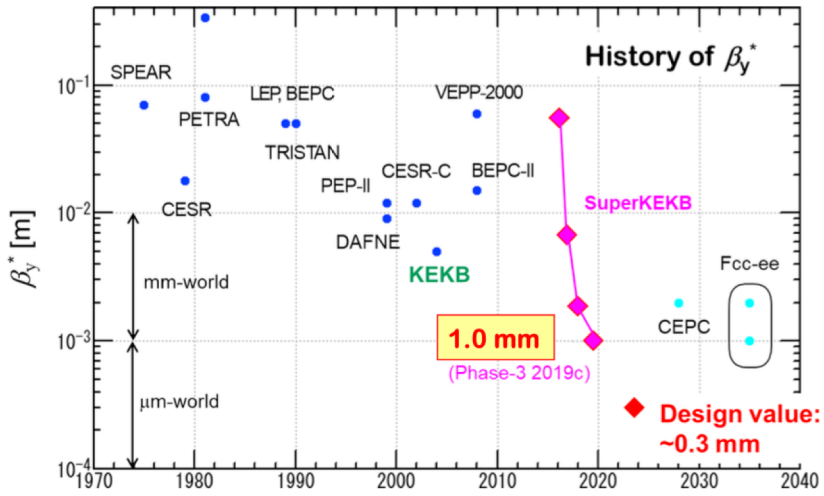




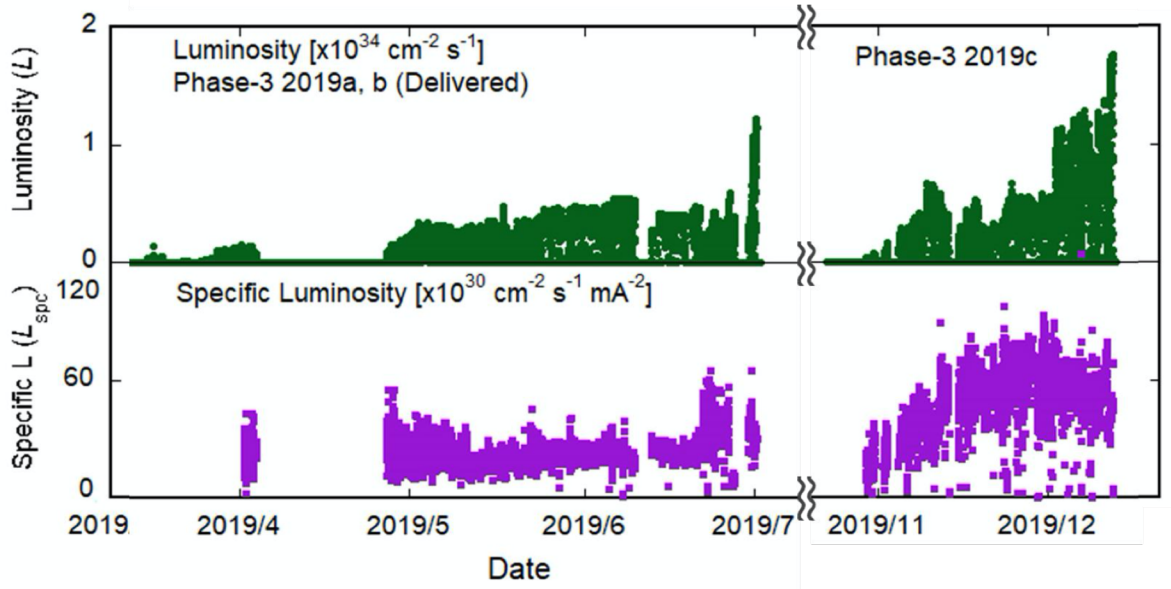
- SuperKEKB: Asymmetric energy e^+e^- collider
  $E_{cm} = m(\Upsilon(4S)) = 10.58$ GeV
- Peak luminosity: $\mathcal{L} = 8 \cdot 10^{35}$ cm^{-2} s^{-1} (x40 than KEKB)
  Beam size reduction. Higher current (x2 higher).

SuperKEKB Operation



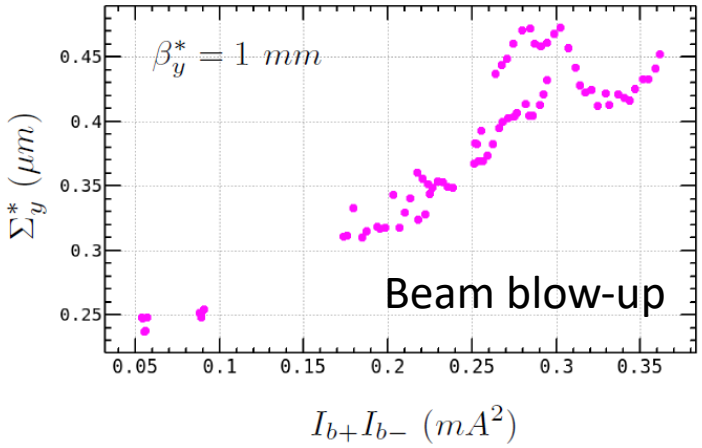


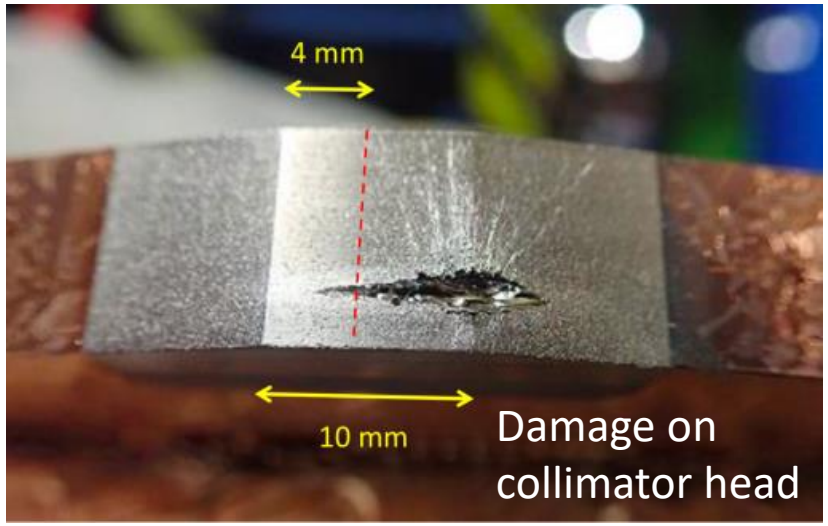
$$\mathcal{L} \sim \frac{N_1 N_2}{\sigma_x \sigma_y}$$

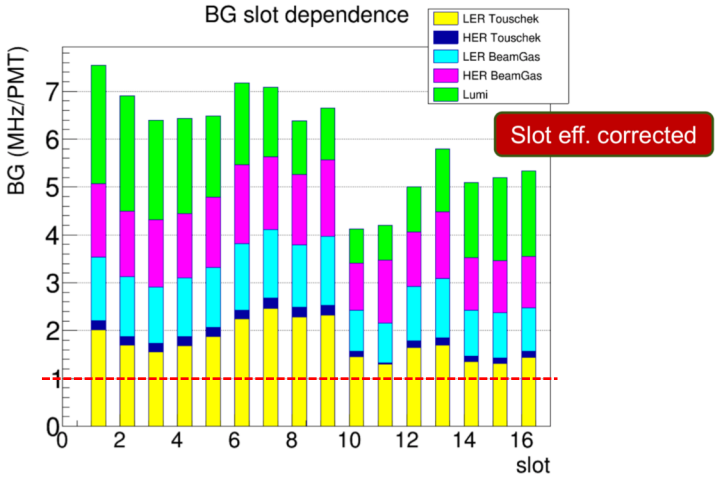


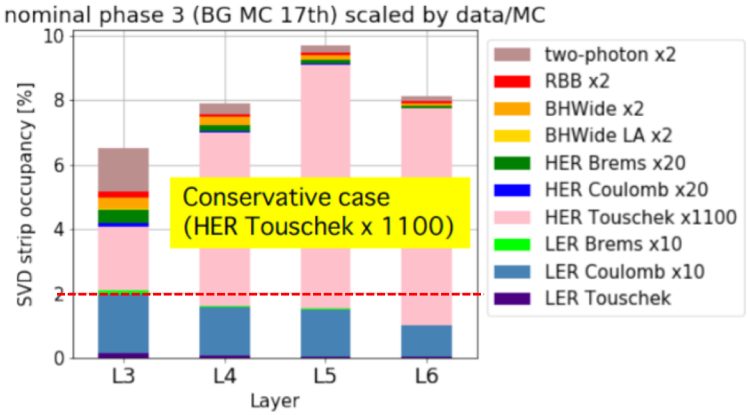
1.88x10^{34} cm^{-2}s^{-1}
HER (LER) = 880 (650) mA
β^*_y = 1 mm

SuperKEKB Operation: Hiccups



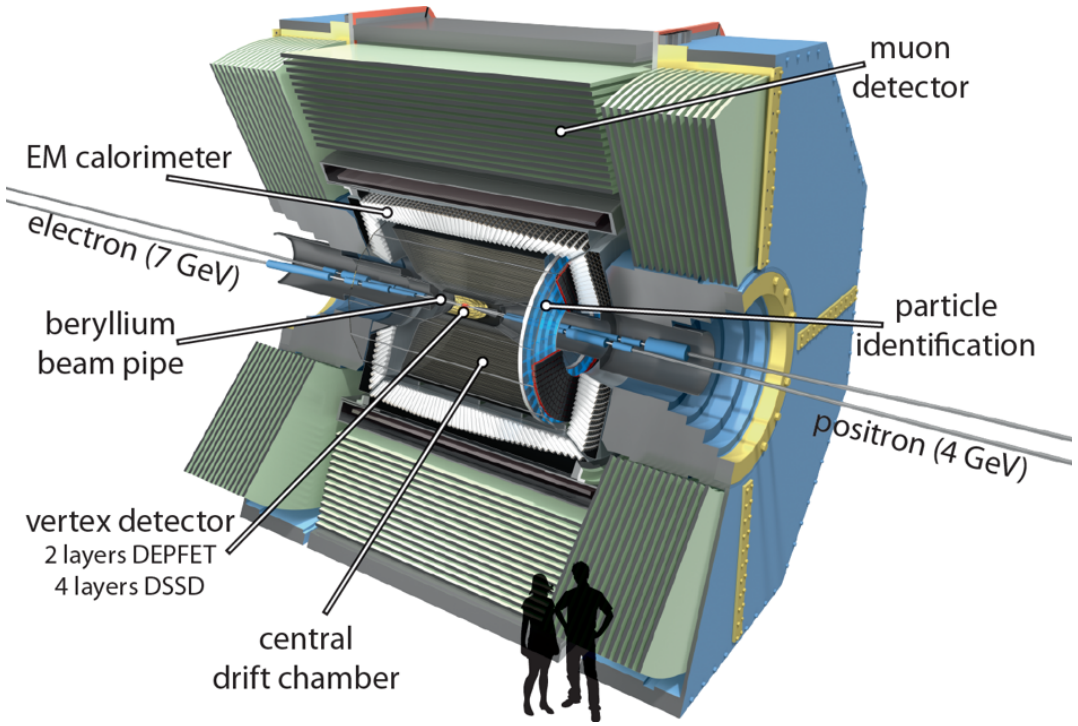






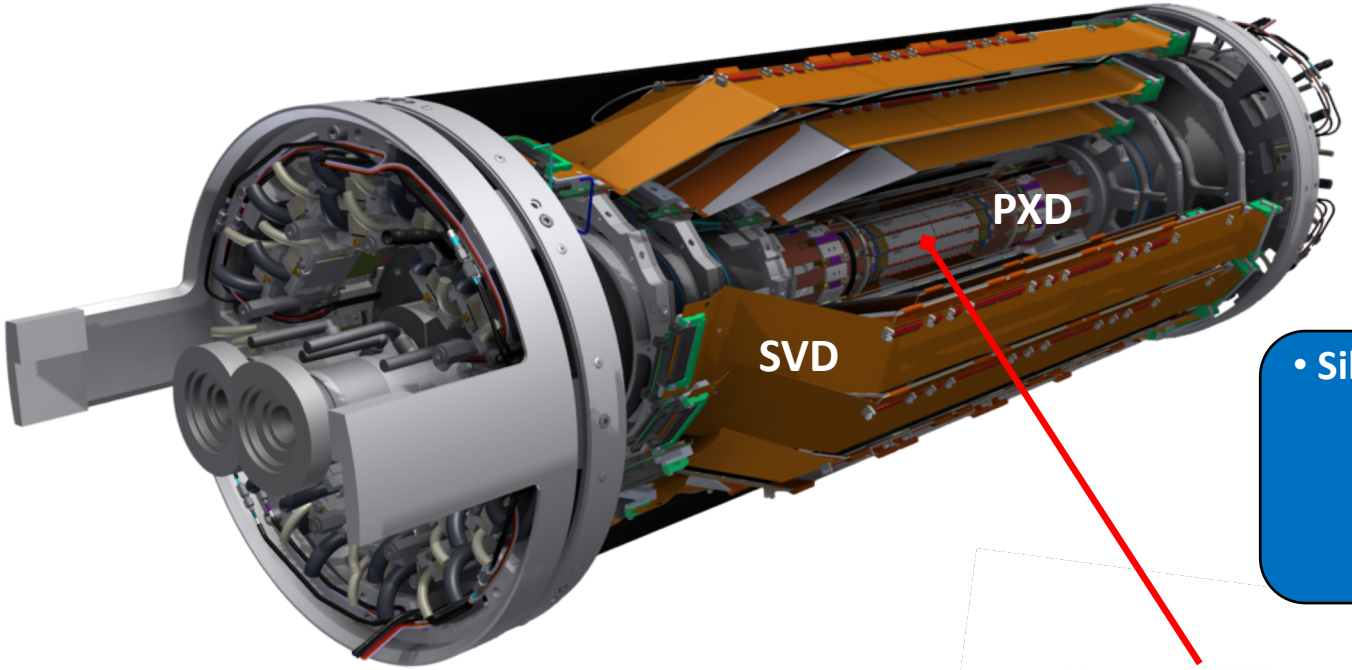
Background projections (TOP, SVD)

Belle II VXD: Backgrounds



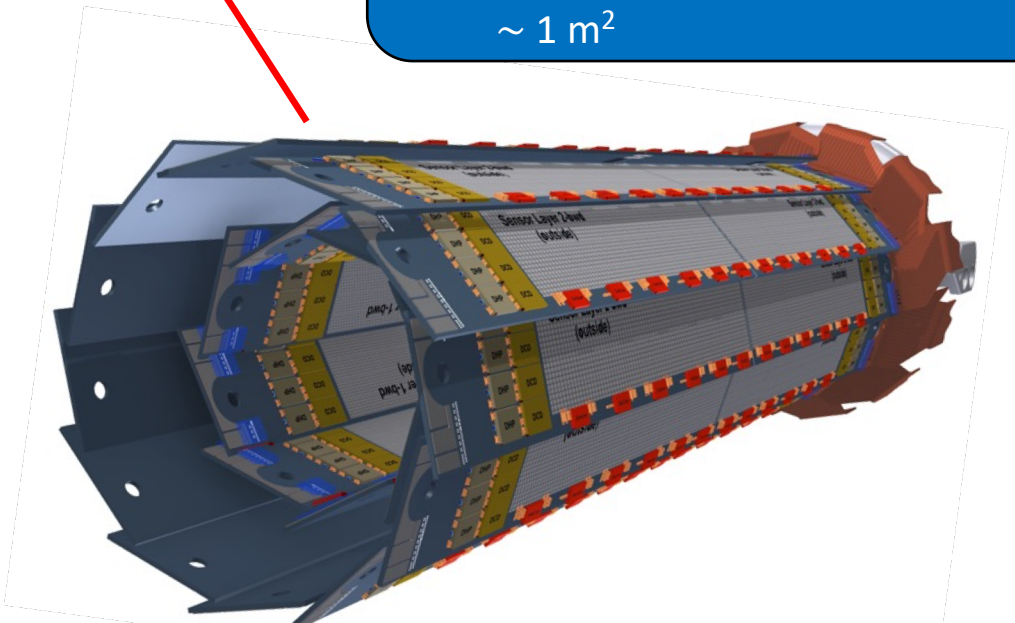
- Backgrounds are higher than anticipated
  → Higher VXD occupancy and rad dam.
- Vacuum scrubbing, optics tuning, collimator optimization will be central but in case we run into troubles in the long term…
- The only way to overcome this limitation:
  - Faster and more granular pixel detectors

Belle II VXD



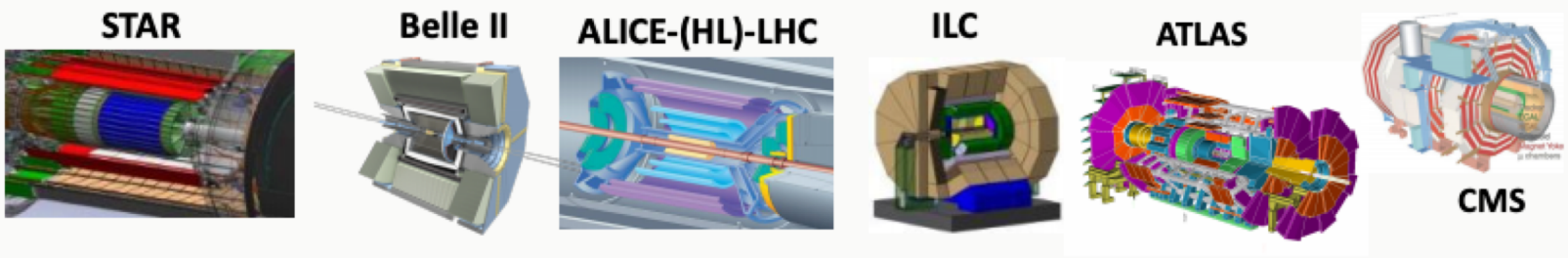
Goal: Replacement of actual VXD with a fully monolithic pixel detector VTX

- **Silicon Vertex Detector (SVD)**
  - 4 layers of DSSD
  - r = 3.8 cm, 8.0 cm, 11.5 cm, 14 cm
  - L = 60 cm
  - ~ 1 m^2



- **Pixel Detector (PXD)**
  - 2 layers of DEPFET pixels
  - r = 1.4 cm, 2.2 cm
  - L = 12 cm
  - ~ 0.027 m^2

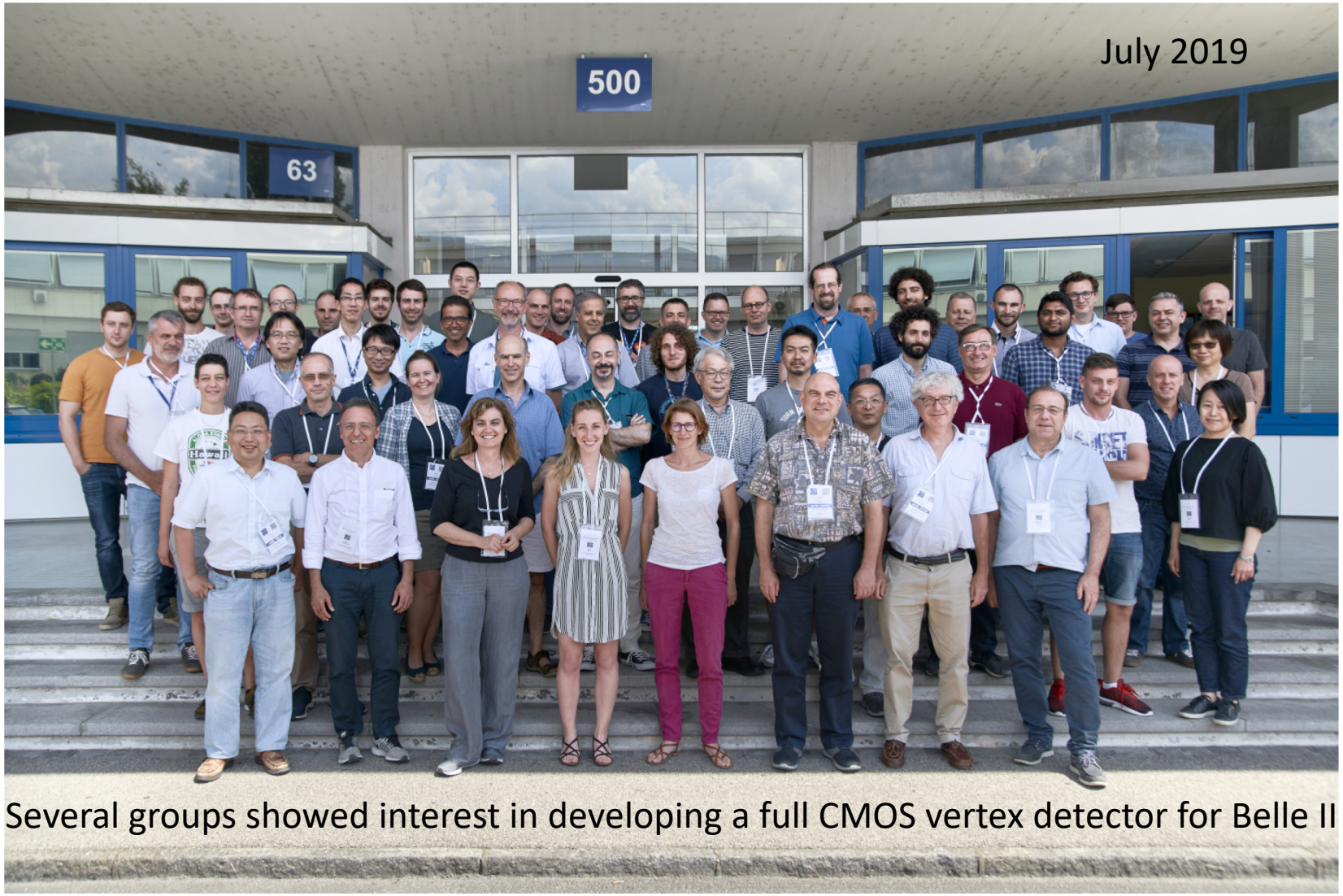
Rates and Radiation Levels



	STAR	Belle II	Belle II upgrade	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
							Outer	Inner
BX-time (ns)	110	2	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	1 100	10	250	1 000	> 1 000	> 10 000
Φ (n_{eq}/cm^2)*	> 10^{12}	10^{14}	10^{15}	> 10^{13}	10^{12}	2×10^{15}	1-2 × 10^{15}	2×10^{16}
TID (Mrad)*	0.2	20	500 (?)	0.7	0.4	80	100	> 1000

Belle II upgrade approaches (exceeds) the harsh environment at HL-LHC (outer barrel pixels)

Belle II VXD Upgrade Workshop at CERN



Several groups showed interest in developing a full CMOS vertex detector for Belle II

Follow up – Belle II CMOS Upgrade

Belle II CMOS Upgrade - Agenda

Large blocks to introduce the overall concept:

- Mechanics, cooling, ladder design, integration
- Software, layout optimization
- Technology options, sensor design
- Off detector electronics, DAQ

Presentations of each of the interested groups
(potential external members)

Informal and with plenty of time for discussions

https://indico.ific.uv.es/event/3862/timetable/#20191217

09:00	**Introduction**	*Carlos Marinas*	
	Universe	09:00 - 09:15	
	Overall concept. Ladder design.	*Carlos Marinas*	
	Universe	09:15 - 09:45	
	Detector geometry	*Benjamin Schwenker*	
	Universe	09:45 - 10:00	
10:00	**CMOS Sensors. Technology 1.**	*Jerome Baudot*	
	Universe	10:00 - 10:15	
	CMOS Sensors. Technology 2.	*Tomasz Hemperek*	
	Universe	10:15 - 10:30	
	Off-detector electronics. DAQ 1.	*Tomasz Hemperek*	
	Universe	10:30 - 10:45	
	Off-detector electronics. DAQ 2.	*Ricardo Marco*	
	Universe	10:45 - 11:00	
11:00	**Break**		
	Universe	11:00 - 11:30	
	Bonn	*Norbert Wermes*	
	Universe	11:30 - 12:00	
12:00	**Strasbourg**	*Jerome Baudot*	
	Universe	12:00 - 12:30	
	Marseille	*Pierre Barrillon*	
	Universe	12:30 - 13:00	
13:00	**Barcelona**	*Raimon Casanova*	
	Universe	13:00 - 13:30	

General Ideas: High Rate CMOS VXD

- Light. Thin DMAPS silicon pixel sensors: 0.1% X_0 (inner) - 0.3%-0.5% X_0 (outer)
- Precise. Small pixel pitch: 30-40 µm
- Fast. Full electronics circuitry per pixel: 25-100 ns, sparsified readout
- Simplified services: Warm operation and fewer cables
- Reduced costs and production time
- Easy to assemble, test and exchange

Stage 1 Upgrade

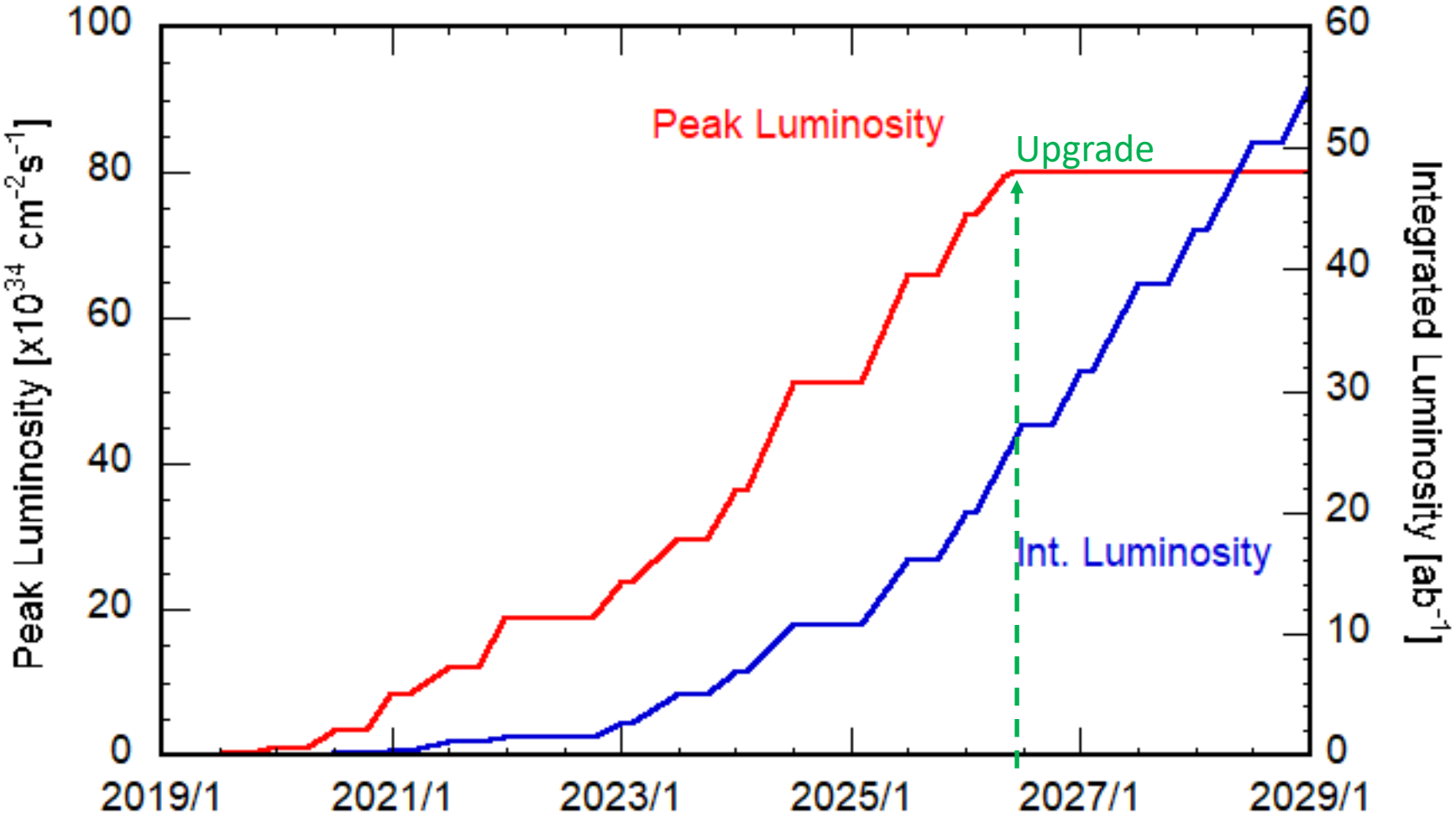
A two-stage vertex detector upgrade can be considered:

1) Replacement of actual VXD with CMOS pixel sensors keeping current boundary conditions between sub-detectors and machine-detector.

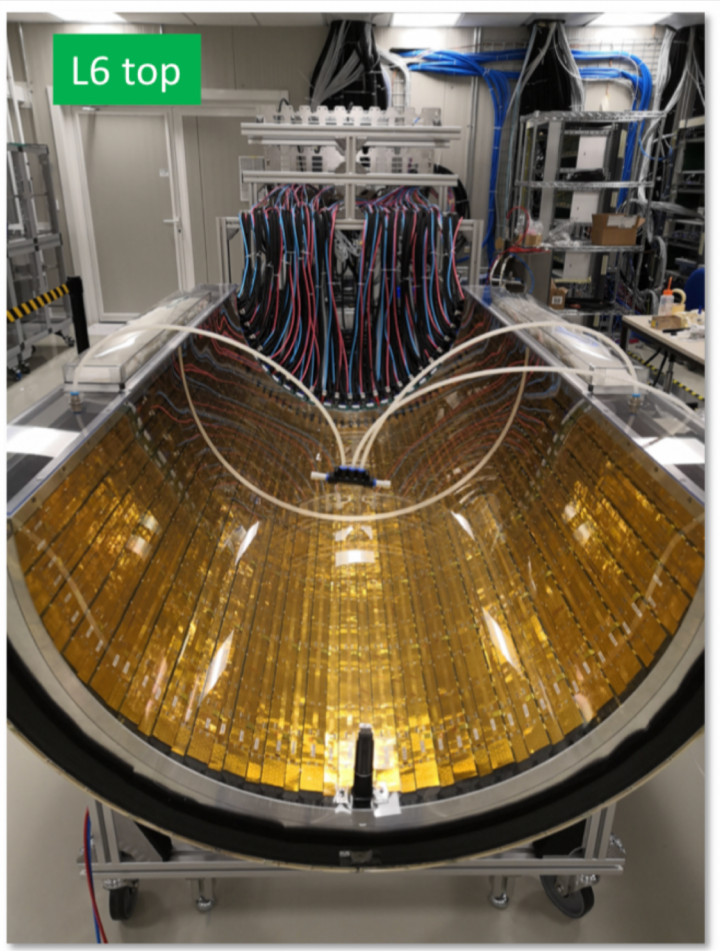
The **'Make it boring'** *(not so boring anymore…)* option to cope with harsher environment
Conservative option aiming 2026 evolving the sensors we have already in hand

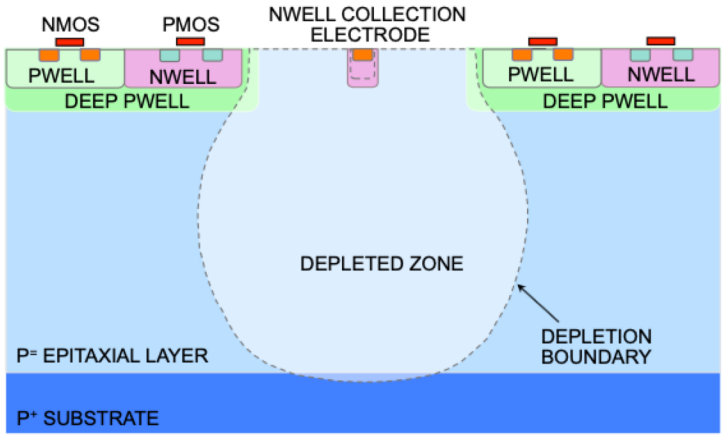
2) Belle III: Long term option aiming >2030 moving to 65 nm, stitching, …

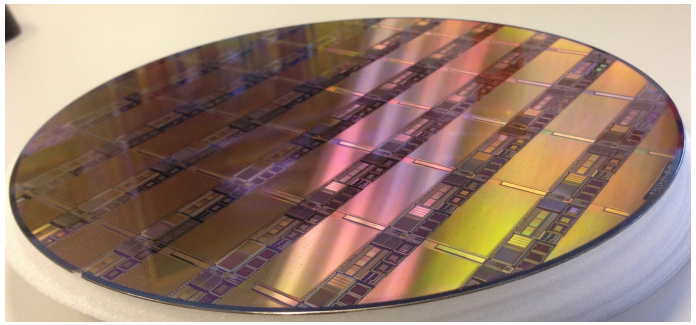
Why 2026?


Peak Luminosity
Upgrade
Int. Luminosity
Peak Luminosity [x10^34 cm^-2 s^-1]
Integrated Luminosity [ab^-1]
100
80
60
40
20
0
60
50
40
30
20
10
0
2019/1
2021/1
2023/1
2025/1
2027/1
2029/1

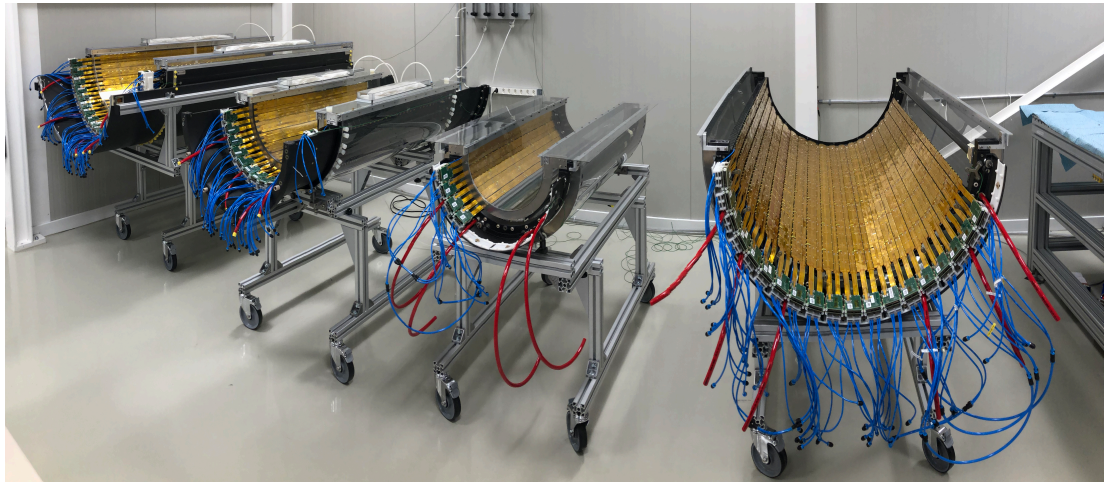
ALICE ITS Upgrade







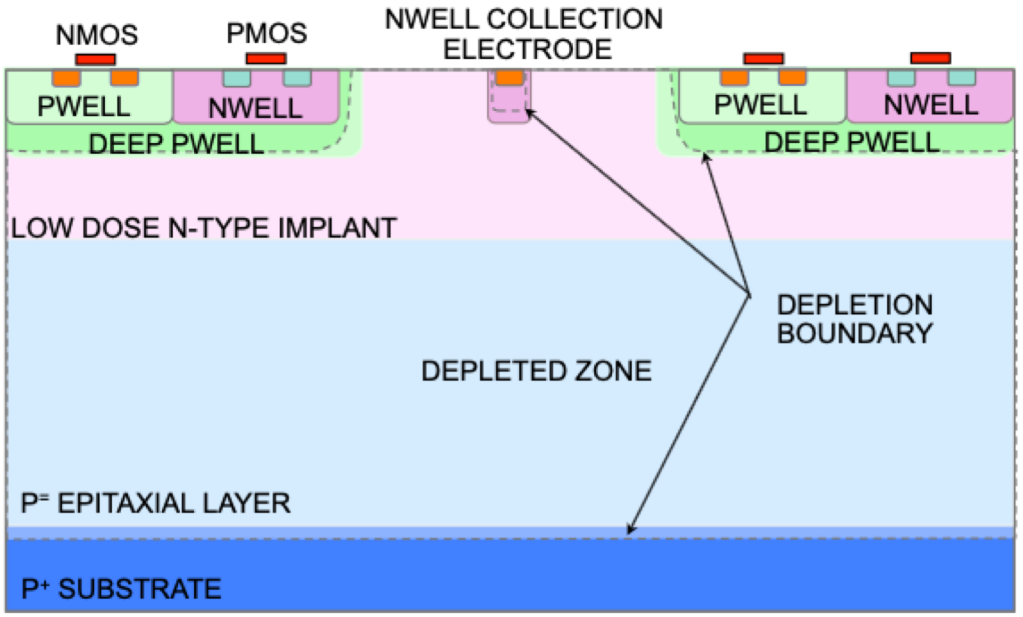
- 10 m^2 (24 kchips)
- 12 Gpixels
- 50 µm thin
- 30 µm pitch



→ This proposal goes in the direction of evolving the ALICE concept

Small Electrode Sensor Design

Monolithic detector: Combine sensor and readout on the same wafer



Electronics outside the collection well
Small fill factor

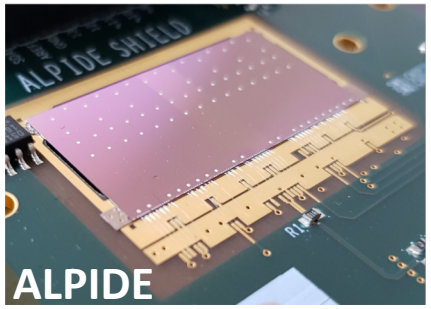
- Very small sensor capacitance
- Low noise and power

TowerJazz 180 nm CIS

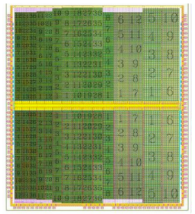
- Deep pwell allows for full CMOS in pixel
- High resistivity epi-layer 1-8 kOhm.cm
  Epi thickness 18-40 µm
- 3 nm gate oxide for good TID
- Modified process: Additional planar n-type implant
  Full depleted volume
  Fast charge collection
- Derived from ALICE development (CERN)

TowerJazz Development Line

Demonstrators to match ATLAS specifications of outer pixel layers



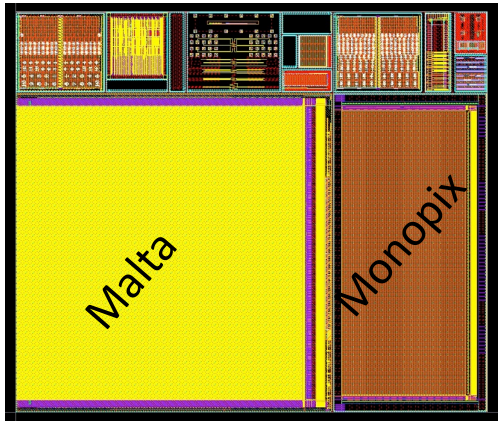
5x5.7 mm^2



Investigator

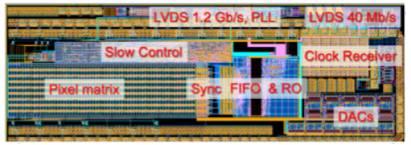
2016

20x20 mm^2
10x20 mm^2



2018

5x1.7 mm^2



MiniMalta

2018

20x18 mm^2

Submission 2020

- Small fill factor seems more adequate to our needs
  Small pixels, low power and noise
- TowerJazz seems a reliable fab for the long term
- TJ-Monopix2 (+Mimosis) seems to be good tailored to this specific application

80 Mrad and 10^{15} n_{eq}/cm^2
25 ns response time
33x33 µm^2 pitch
200 MHz/cm^2 hit rate

The Gaulish Family: Asterix, Ideafix and Obelix

20x18 mm^2

Submission 2020

Full matrix readout:

- Charge collection properties
- Timing
- Radiation hardness
- (+Mimosis' digital part)

Goal MPW late 2020

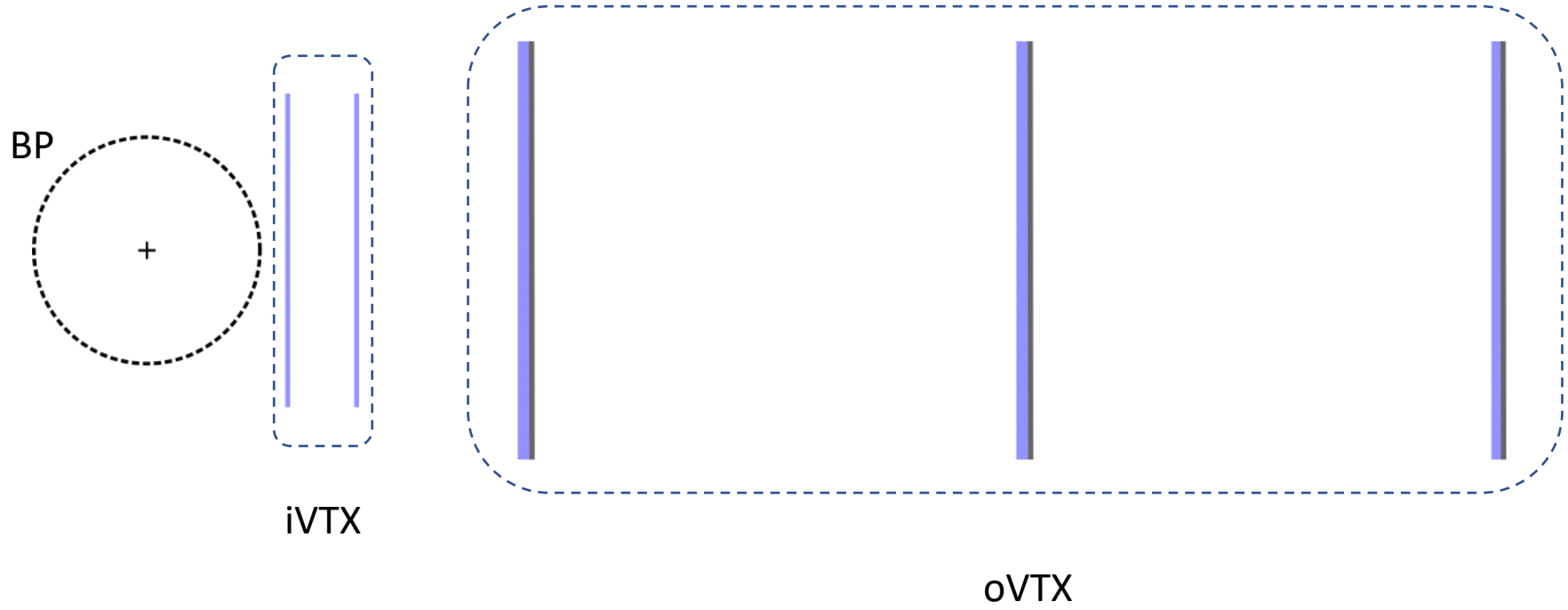
Block prototyping:
(LDO, communication interface and monitoring)

- Power distribution
- Data integrity

Goal 2022-2023

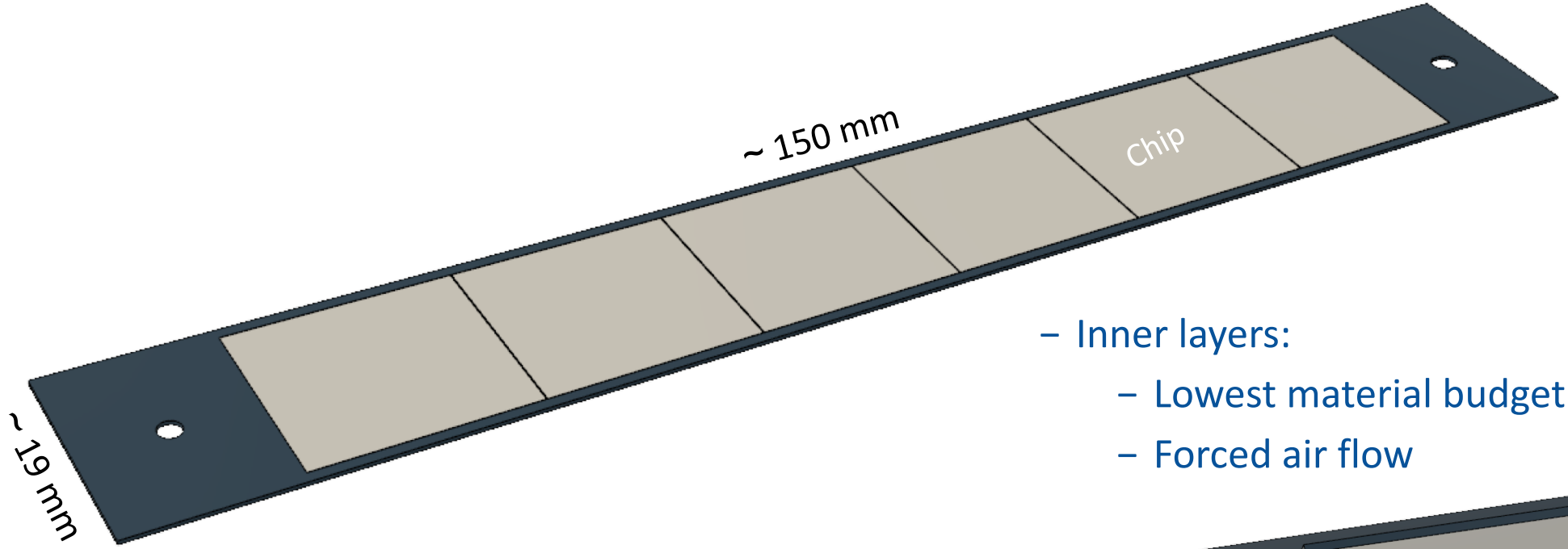
Full size for Belle II

VTX - Vertex Detector



- Same CMOS chip design (iVTX and oVTX) but differences in the support structure, cooling and integration

iVTX: Ladder Concept



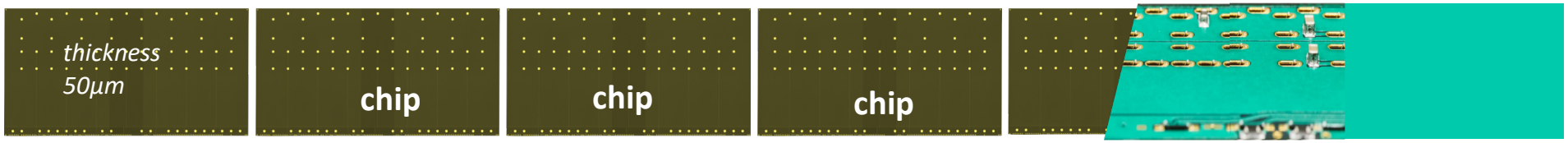
- Inner layers:
  - Lowest material budget
  - Forced air flow

Single piece of silicon

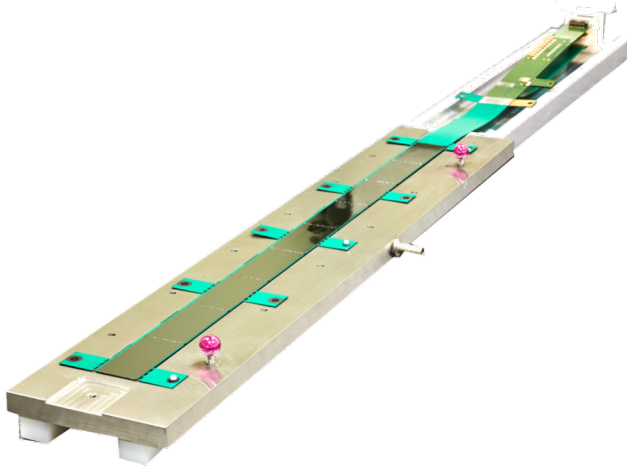
6 sensors per ladder

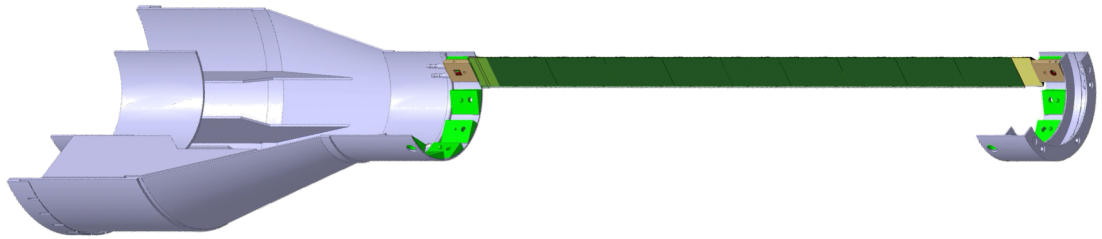
100 µm gap between sensors

oVTX: Ladder Concept



- Outer layers:
  - Active cooling
  - Electrical substrate (chip on a Kapton)





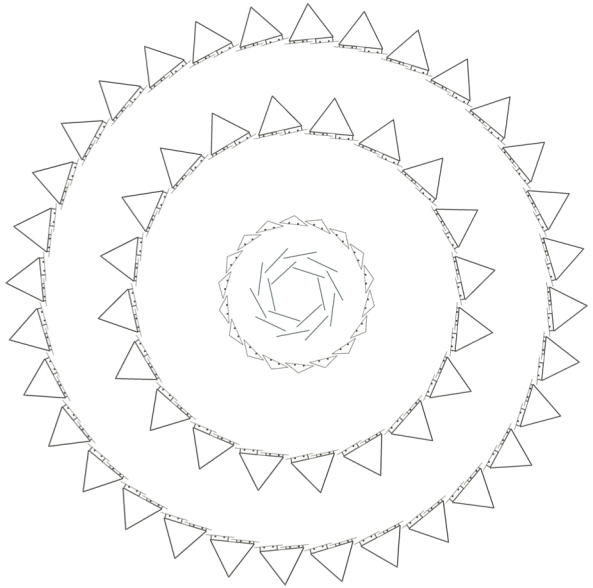
Attempt of putting the concept together

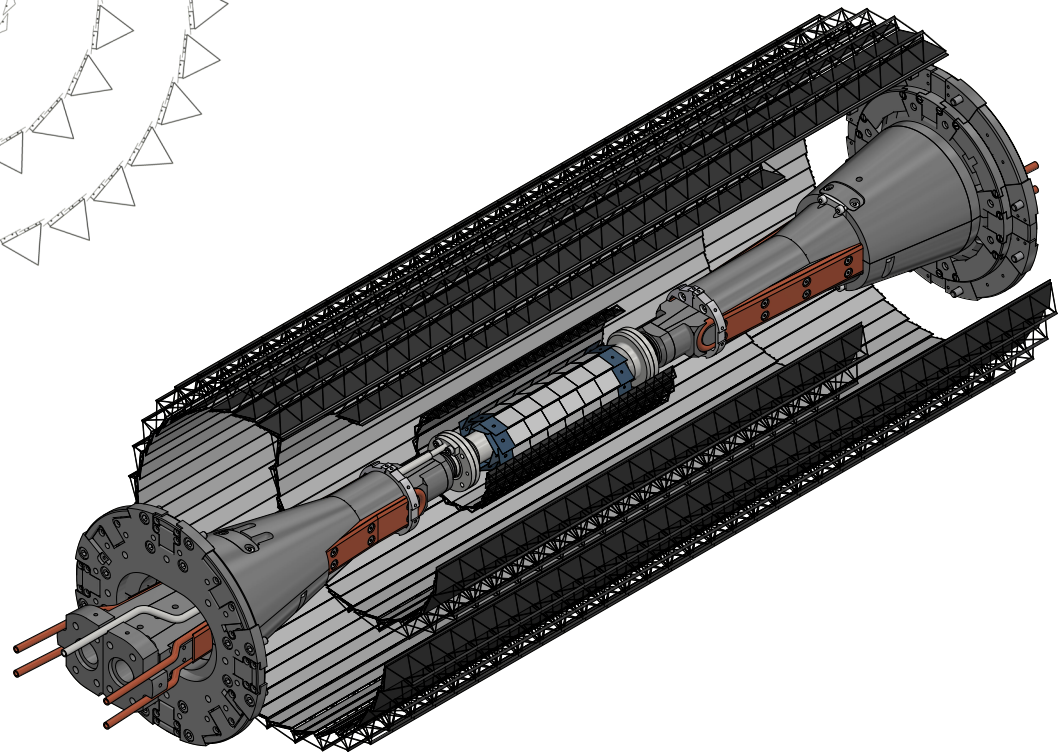
- 5 VTX layers design

L1+L2: Full silicon

L3: oVTX based on ALICE inner space frame

L4+L5: oVTX based on ALICE outer space frame





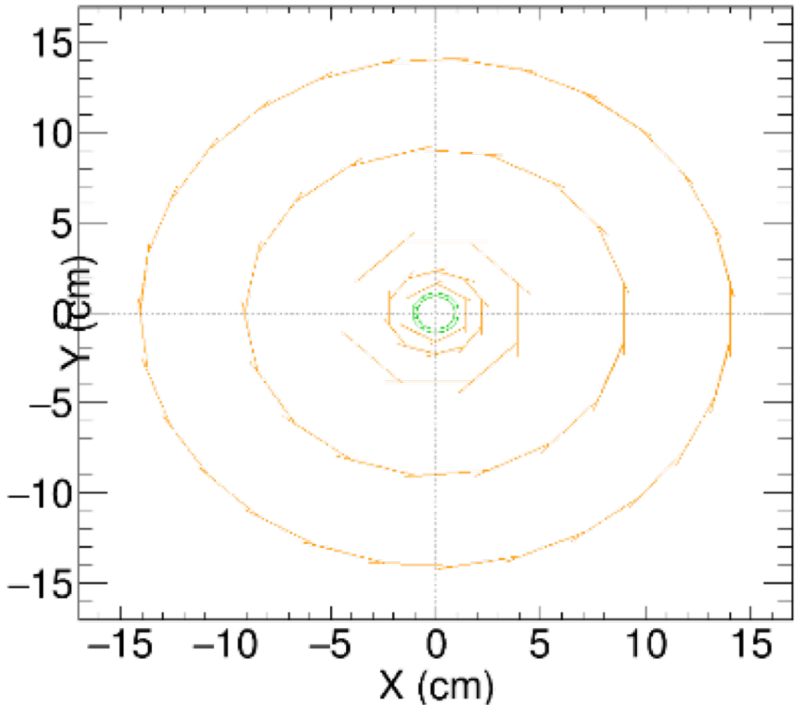
Layout Optimization

5 layers

3 outer layers = 52 ladders

Total # sensors ~ 3000

Material budget ~ 1.3 % X_0

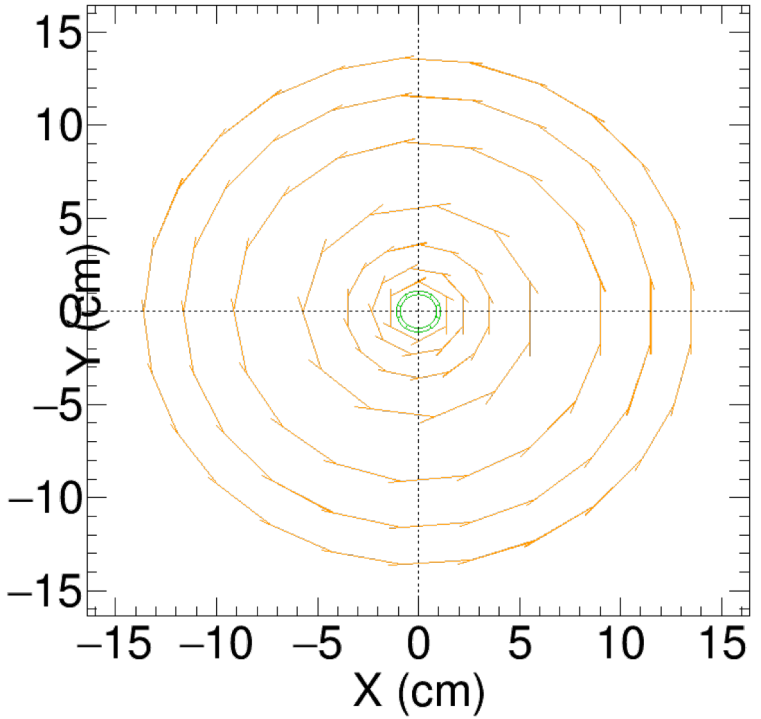


7 layers

5 outer layers = 74 ladders

Total # sensors ~ 4000

Material budget ~ 2.9 % X_0



Layout Optimization

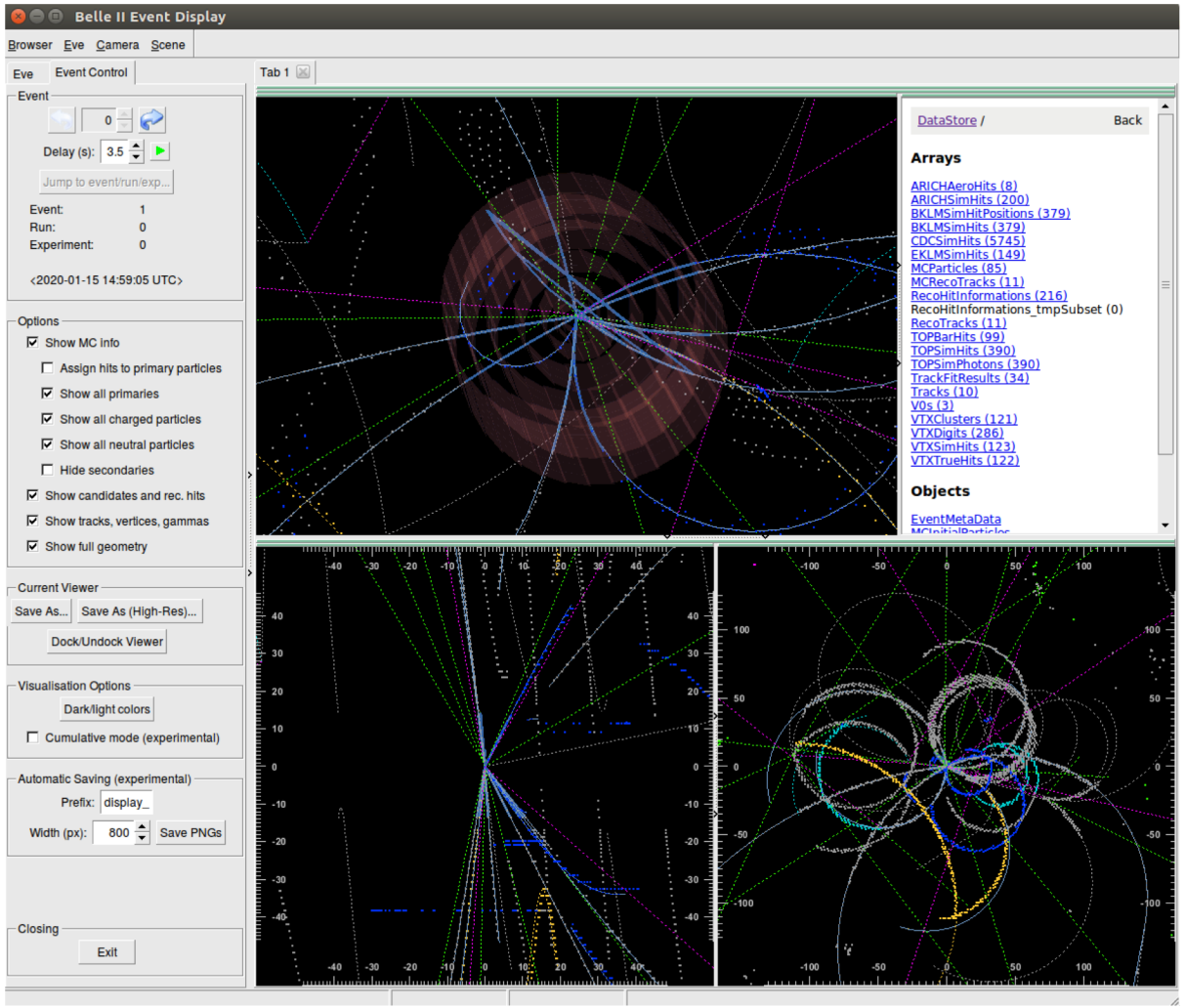
- Focus on 2-3 geometries (technology independent)

- Early implementation with 5 and 7 layer VTX with 40x40x40 μm^3 pixels and binary readout are ready for testing in the Belle II software framework

- Simulated VTX response to background particles and physics generators (digits, clusters)

- Find tracks (using MC truth info) and fit tracks using reconstructed clusters

- Adding background hits and integration into VXDTF will follow



BBar event display: VTX objects, RecoTracks, Tracks and TrackFitResults

Executive Board: Oct B2GM 2019

Upgrade Status Report

Areas of activity (simplified)

- VXD – possible partial or total replacement of system
- Monolithic CMOS sensors (replacement of full system)
- Thin Double-Sided-Strip-Sensors (only SVD replacement)
- CDC – improved electronics
- PID – possible replacement of photon detectors (SiPM ?)
- ECL – study of pre-sampler to get ũ direction
- KLM – possible replacement of RPC with scintillator
- Rad monit. – Continuous monitoring with radiochromic films
- Det Control – advanced platform for detector control
- DAQ upgrade – already ongoing

EB endorsed the creation of the VXD Upgrade R&D Working Group under the Upgrade Working Group organization

- Ad interim coordinator will be F.Forti, with the idea of identifying suitable coordinator(s) as soon as possible

1) EB created the VXD R&D upgrade group (CMOS explicitly mentioned)

Executive Board: Feb B2GM 2020

VXD R&D Collaboration and technologies

- We plan to have the following organization:
  - Most activities will be within the Belle II collaboration, with open participation of external members.
  - Independent collaborations and associations will be probably needed for funding applications and local organization: encourage full transparency and shared information
  - Different technologies can develop their own working group and strategies, but need to share the general structure of working areas and contribute to common developments
    - CMOS VTX proposal is the most developed at the moment
  - Identify point of contact for the various areas, with the purpose of collecting information and coordinating activities.
- Maintain flexibility to adapt to changing needs

1) EB created the VXD R&D upgrade group (CMOS explicitly mentioned)

2) EB acknowledges CMOS VTX proposal (i. e. ours) as the most developed

Executive Board: Feb B2GM 2020

Request to EB

- Endorse the proposal to start negotiations with CERN to develop an agreement between Belle II and CERN to facilitate the exploitation of existing technologies and the organization of common developments.
- General framework for collaborative work and access to CERN infrastructure
- Specific addendum for CMOS development
  - Allow access of TJ process through CERN contracts
  - Allow collaboration with CERN engineers for design and verification.
- No money involved in the agreement
  - It will have to come from R&D project funding
- I believe the Belle II spokesperson should sign
  - Other options ?

EB approved this and proposal for Belle II Spokesperson to sign

University of Victoria

1) EB created the VXD R&D upgrade group (CMOS explicitly mentioned)

2) EB acknowledges CMOS VTX proposal (i. e. ours) as the most developed

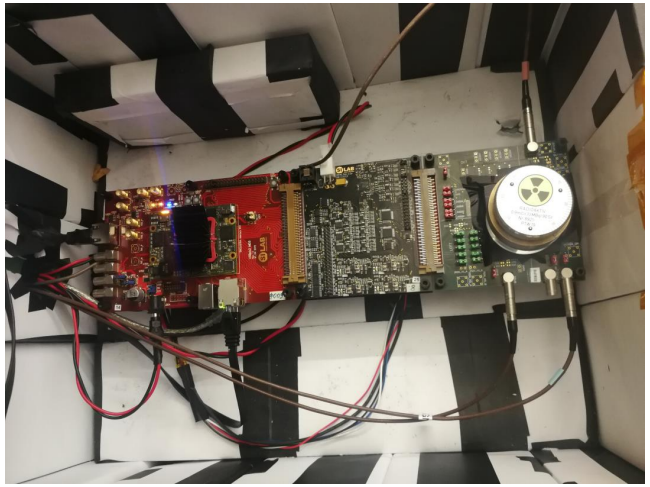
3) Renovation of Belle II as a recognized CERN experiment including a specific addendum for joint (Belle II and CERN) CMOS developments

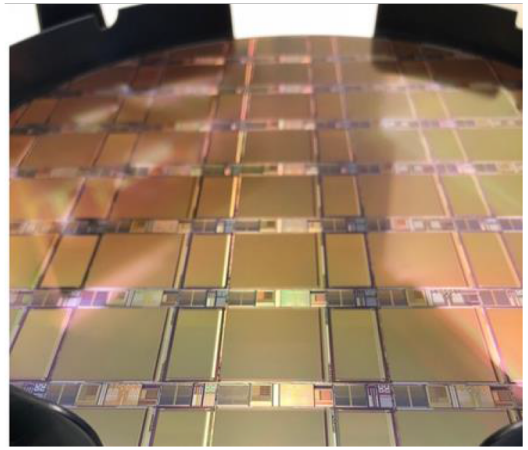
VTX Rough Timeline

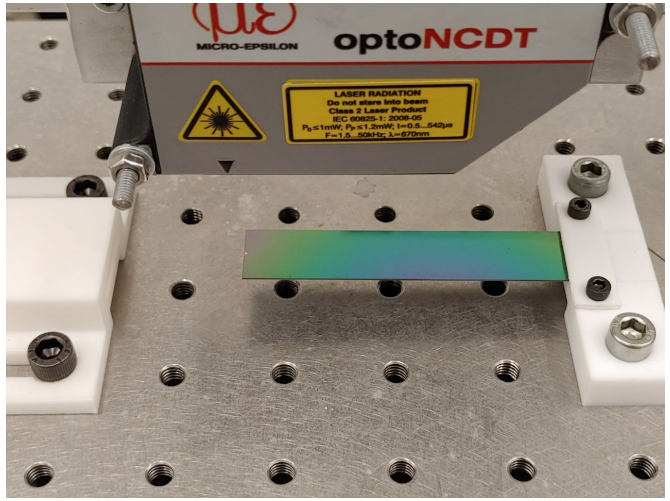
- 2020
  - Physics impact benchmarking of layout and solutions
  - Prototypes and concept development
  - Develop agreement with CERN for access to TJ technology and tools
  - Establish mission need: what is needed and when
- If mission need is established, go through the other steps
  - 2021 - EOI
    - Expression of Interest: **understand which groups are interested**
  - 202x - CDR
    - Conceptual Design Report: produce a technically sound concept for the upgrade, with an initial cost estimate. Options can still be open
  - 202y - TDR
    - Technical Design Report: a detailed, construction ready design of the system. Detailed cost estimate and funding sources. Very few open options can remain, if any

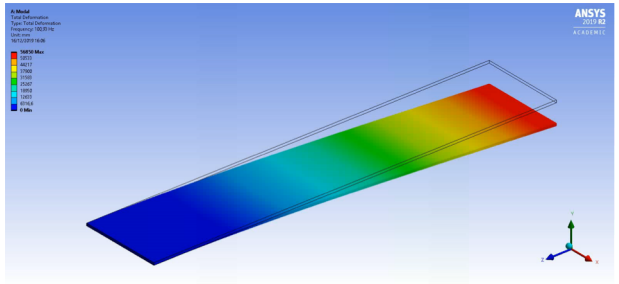
Belle II CMOS Activities at IFIC

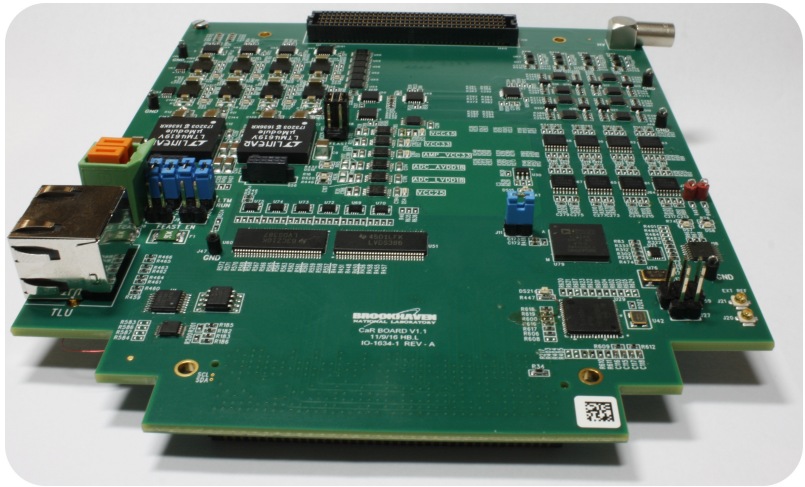
- Leading the Belle II VTX CMOS upgrade effort
- Characterization of TJ-Monopix1 (laser+sources+test beam+irradiation)
- Develop a DAQ system based on Caribou
- Mechanical characterization of the ladders
- CAD integration of the whole tracker











Outlook

- Held a workshop at IFIC in Dec'19 with interested groups in developing a VXD upgrade with CMOS sensors
- TowerJazz Small electrode DMAPS seems suited for this application and is the baseline of our proposal
- Full size demonstrator chips suited for Belle II in fall 2020
- We are getting organized (AIDANova, CSIC-Platform, …) and things are moving very fast…
- Great opportunity to work with (be part of) 'The CMOS Club'

THANK YOU

iVTX: Services

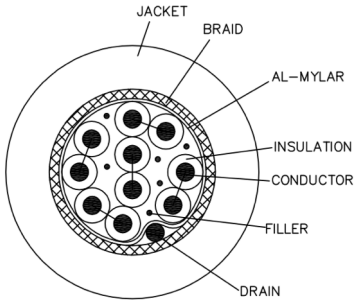
- 6 chips per ladder
- Access from both sides
- All cables LSZH

Power

1 common power
1 common bias
1 common ground
+ Regulators on each chip

ϕ = 12 mm

Control
Data

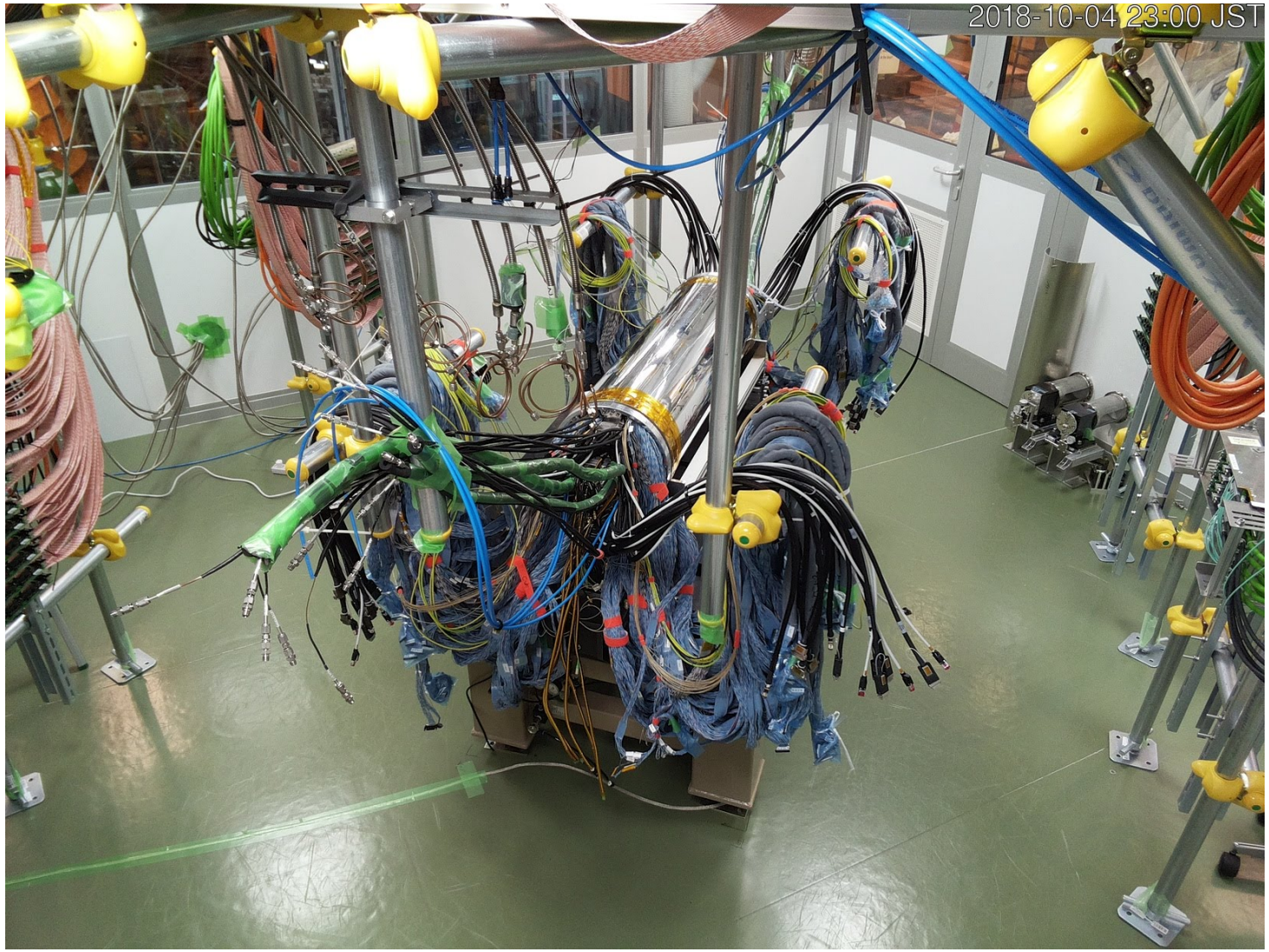


1 data per chip (serial output, ~30 Mbit/s))
1 command per module
1 clock per module
10 pin LVDS

ϕ = 5 mm

Most conservative option: 1 set per module (x16 per side) → 40% of actual PXD cross section

VXD Services



Note: Only less than 50% of PXD installed here