Readout Electronics for the ATLAS Tile Calorimeter at the HL-LHC

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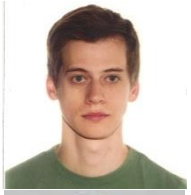
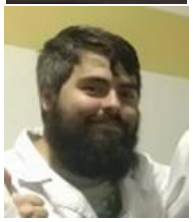
Introduction

- Our TileCal electronics group:
  - Fernando Carrió Argos
    - Electronics Engineer with PhD
    - Personal Técnico de Apoyo (2015) (UV)
  - Alberto Valero Biot
    - Electronics Engineer with PhD
    - Titulado Superior Especializado (2011) (CSIC)
  - Francisco García Aparisi
    - PhD student in Electronics Engineering (2017) (UV)

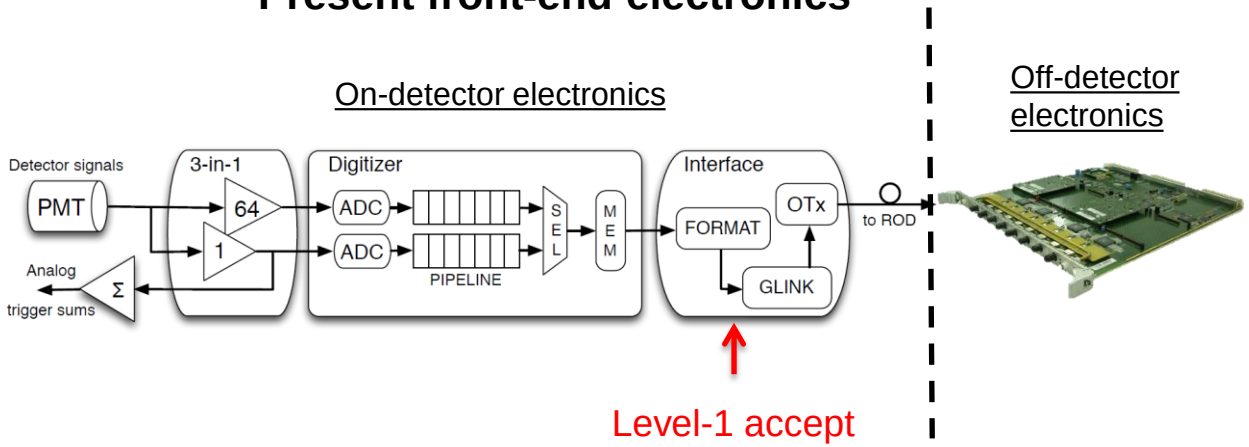




- Main tasks in the Upgrade:
  - Complete design and production of the back-end electronics for the TileCal Upgrade → Tile PreProcessor
    - High speed board design up to 16 Gbps
    - Firmware for FPGAs: Data acquisition, detector control system, energy reconstruction, synchronization and high speed links
    - Contributions to the development of DAQ software
  - Coordination of the TileCal Upgrade project

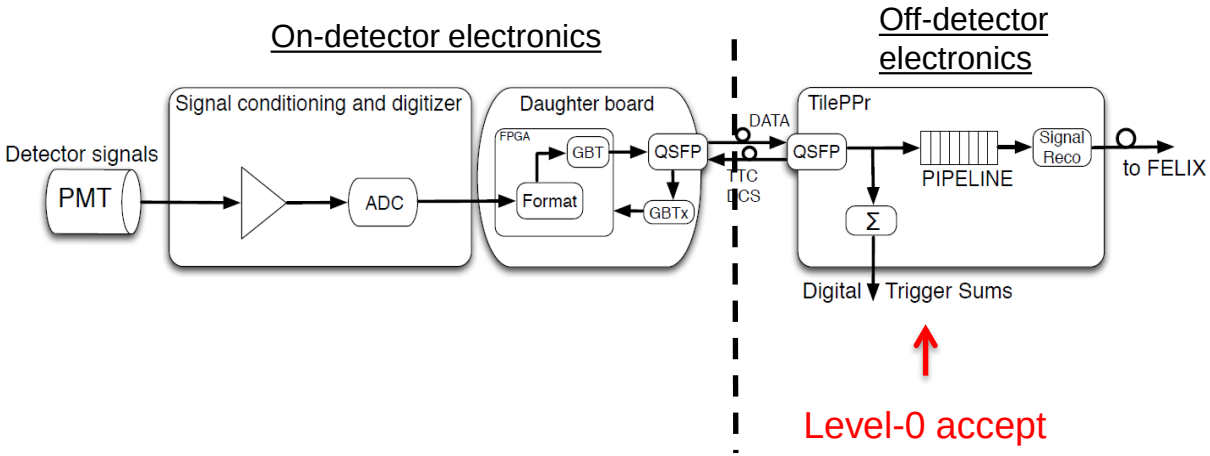
Tile Calorimeter Phase II

Present front-end electronics



	Present	Phase II
Total BW	~205 Gbps	~40 Tbps
N. Fibers	256	4096
BW / module	800 Mbps	160 Gbps
Nb. boards	32 (ROD)	32 (TilePPr)
Nb. crates	4 (VME)	4 (ATCA)
Out BW / board$_{DAQ}$	2.56 Gbps (ROS)	40 Gbps (FELIX)
Out BW / board$_{L1/L0}$	Analog	500 Gbps

Equivalent electronics for Phase II Upgrade

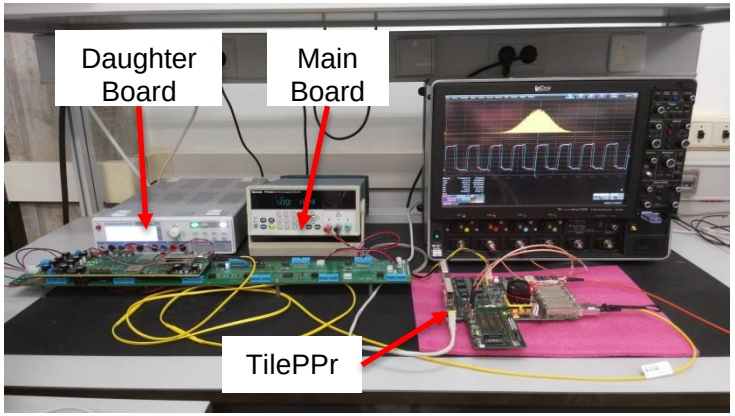


- Front-end electronics transmits all the samples@LHC frequency
- Pipelines are moved to the back-end electronics (TilePPr)
- Clock is distributed from the back-end electronics

TilePreProcessor Demonstrator

- **Design of the TilePreProcessor Demonstrator**
  - Double mid-size AMC (µTCA / ATCA carrier)
  - Xilinx Virtex 7, Kintex 7, 4 QSFPs
  - 1/8th of the final PreProcessor
  - 4 mini-drawers → one module
- 8 Tile PreProcessor were produced between 2015 and 2017
  - Installed in different setups: University of Heidelberg, University of Texas at Arlington, University of Stockholm, CERN and IFIC
- Qualification tests were done with a standalone testbench at IFIC
  - Clocking circuitry, Ethernet communication, TTC reception, power configuration
  - Optical jitter measurements with Keysight DCA-X86100D oscilloscope
  - Bit Error Rate Tests: BER better than $5 \cdot 10^{-17}$ for a confidence level of 95%

TilePPr Demonstrator



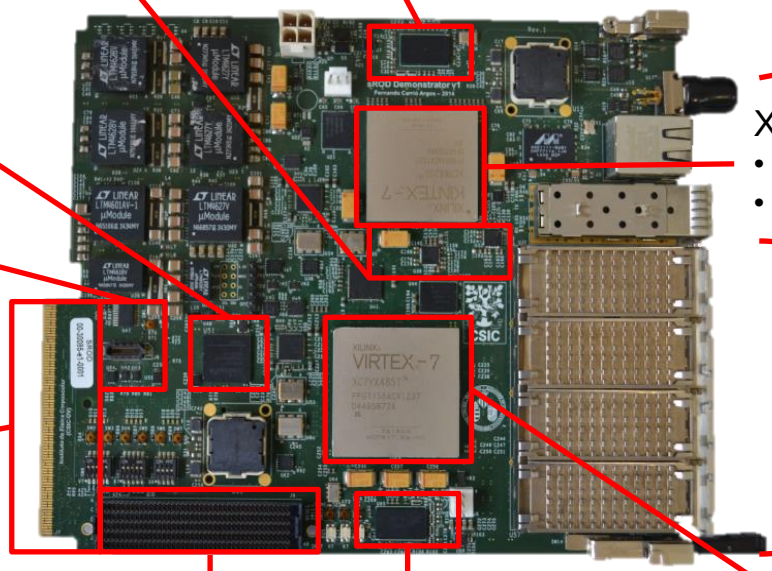
Complete testbench

TilePPr prototype

- Hardware design between 2013-2014
- First prototypes delivered at the end of 2014
- Double AMC form factor (ATCA)
  - Dimensions: 148.5 mm x 180.6 mm

- PCB stack-up: 16 layers
  - Dielectric Nelco N4000-13: low dielectric losses
- Two high-performance FPGAs
- 4 QSFP modules: 160 Gbps
- Avago MiniPOD: 120 Gbps
- Backplane: 40 Gbps

320 Gbps

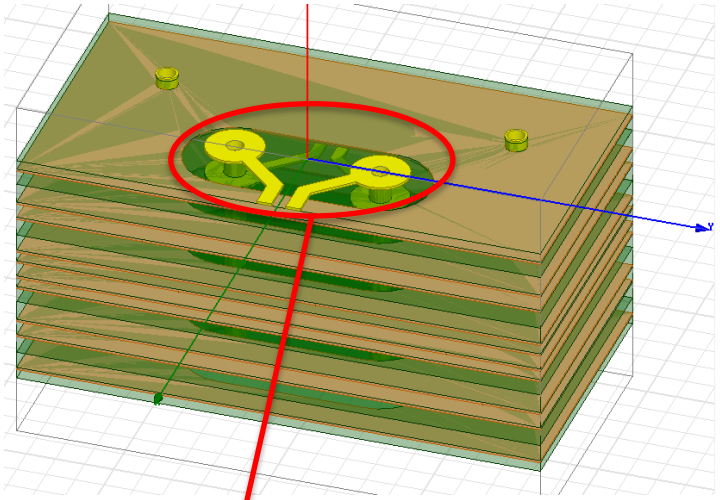


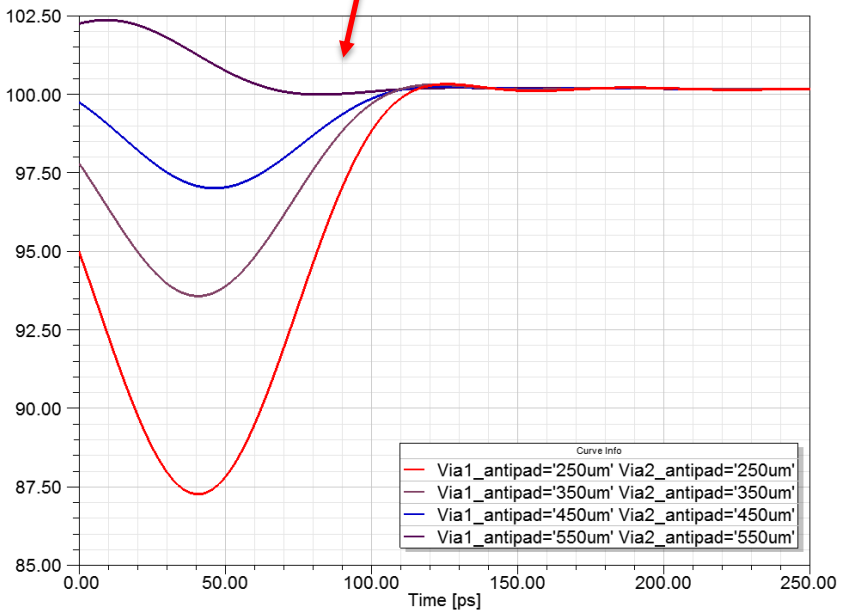
Layout design

- Signal and Power Integrity simulations with ANSYS tools: HFSS, SIwave

- Design of over 10 Gbps lines
  - Differential and characteristic impedances
  - Supression of impedance discontinuities
    - Via design, DC-coupling capacitors
  - Pre- and post-layout signal integrity studies to evaluate the total jitter

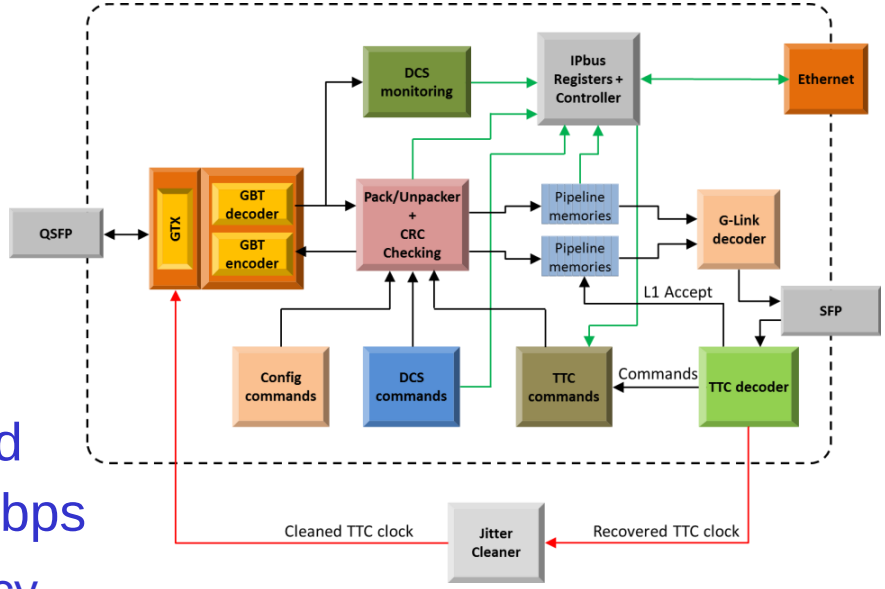
- Power Distribution Network design
  - Low noise design
  - Simulation of the decoupling stage for adequate capacitor selection
  - Simulation of voltage drops due to high currents (IR drops)





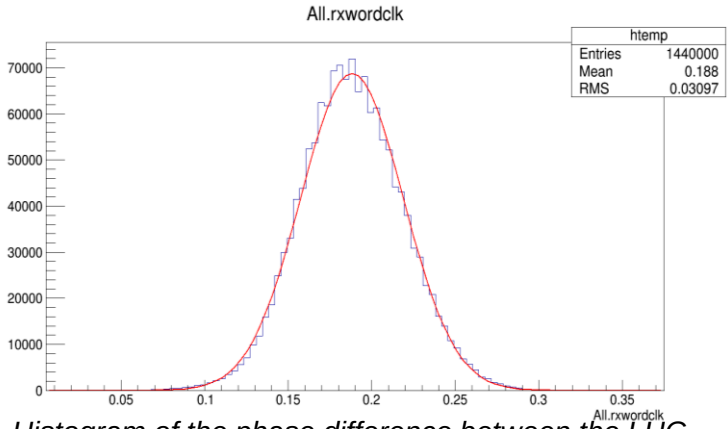
Firmware

- Development of the TilePPr firmware
  - Encoder / decoder modules, DCS, TTC decoder, G-Link emulator, IPBus, etc…
  - Three different readout paths: FELIX, G-Link (ROD), Ethernet port (IPBus)



- Implementation of 16 Latency Optimized GBT links operating at 9.6 Gbps / 4.8 Gbps
  - Fixed and deterministic latency → latency variations below 100 ps between resets

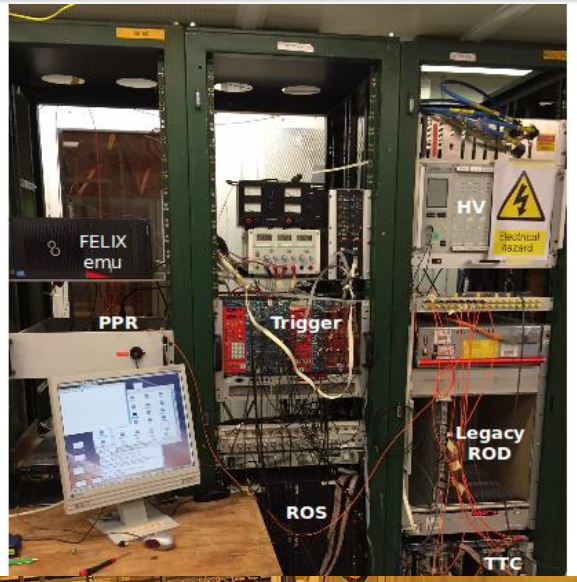
- Development of new phase measurement techniques based on subsampling and oversampling
  - Monitoring of the phase drifts due to temperature changes or latency variations
  - Accuracy ~30 ps_{rms}



Histogram of the phase difference between the LHC clock and the received clock from the DBs (nanoseconds)

Testbeam campaigns

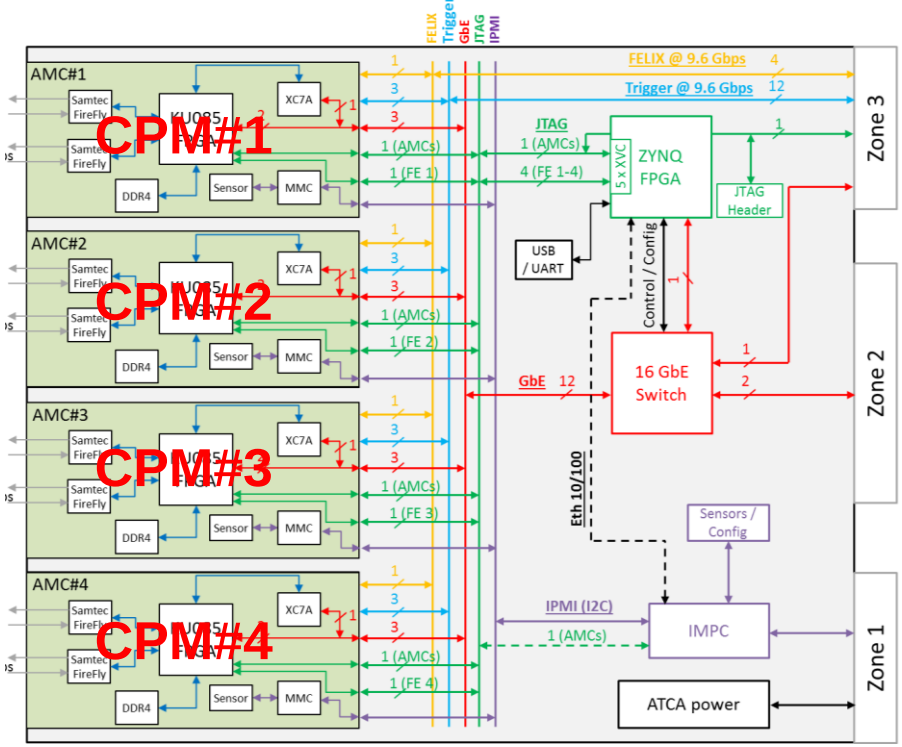
- Five campaigns of 2 weeks between 2015 and 2017
  - ***Two TilePPr Demonstrator boards***
- Three detector modules instrumented with legacy and upgrade electronics
  - 1 Long and 1 Extended module with legacy electronics
  - ½ Long module with the upgraded 3-in1 option readout electronics (Demonstrator)
  - ½ Long Barrel module with FATALIC and QIE options
- Valencia group is highly involved in the operation and data taking of the Demonstrator
- Demonstrator is fully integrated with the TDAQ software and legacy systems

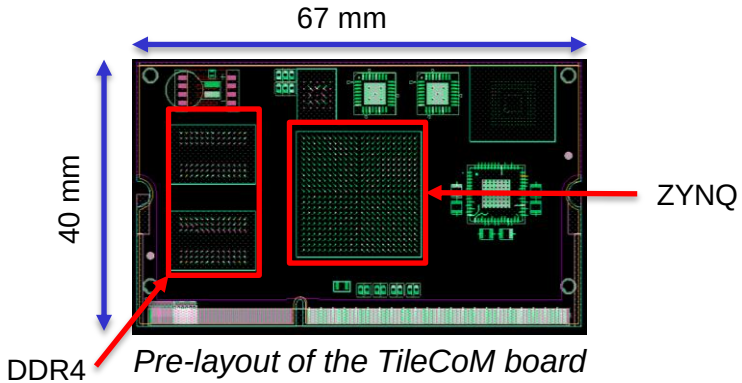


- **Two more testbeams during 2018**
  - TilePPr operation from the ATCA shelf
  - Integration of the FELIX with the TDAQ
  - Tests with the final TilePPr board

Final PreProcessor Prototype

- Full-size ATCA blade (carrier + 4 AMCs)
  - Up to 1.6 Tbps of aggregated bandwidth
  - Scalability and latency
  - Connectivity through Zone 2 connector
- 16 GbE Ethernet switch module
  - Broadcom GbE port switch
  - Connectivity between AMCs, blades and SM
  - DDR3 SODIMM form factor
- Computer on Module (TileCoM)
  - Xilinx ZYNQ XCZU2CG
  - DDR4 memory, flash memory, clocking
  - Diagnostics, monitoring, remote programming
- IPMC mezzanine board – Designed by CERN
  - Hot swap, sensor monitoring, power management
  - DIMM-DDR3 VLP form factor

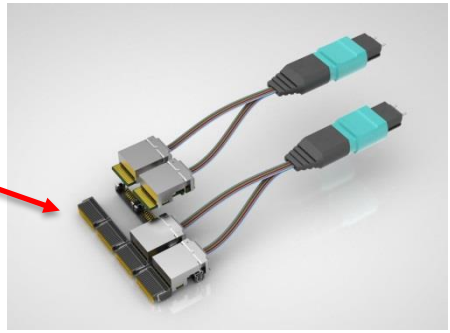




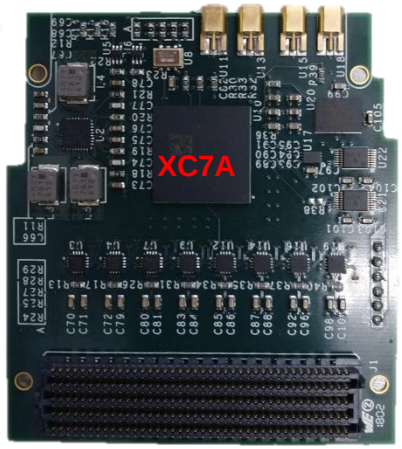
Pre-layout of the TileCoM board

Compact Processing Module

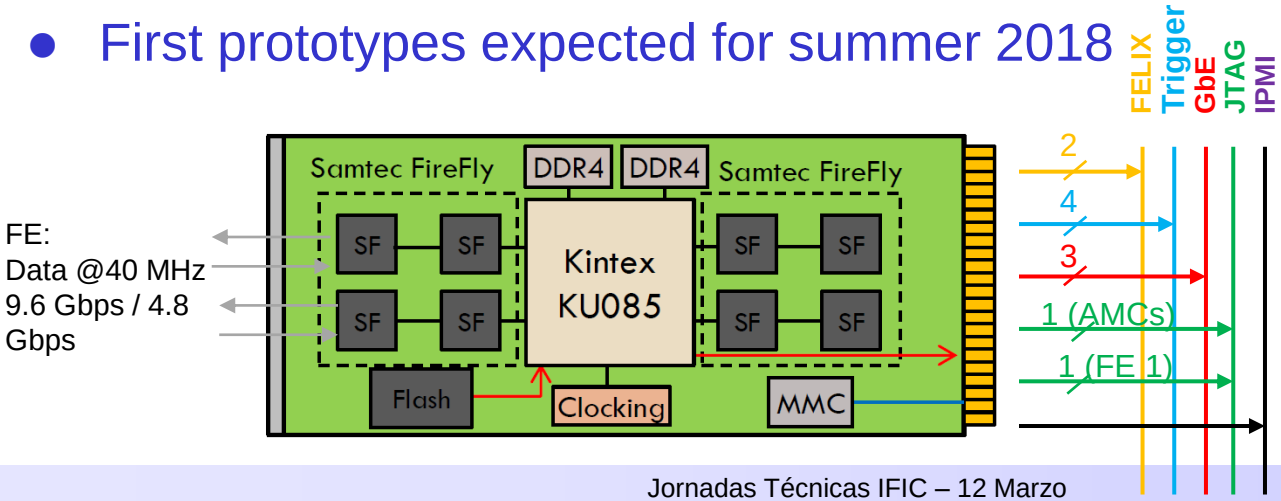
- Each CPM will readout and operate 2 modules
- Single AMC form factor
- 8 Samtec Firefly high-density optical connectors (up to 32 links) – 400 Gbps
- Kintex UltraScale KU085 FPGA
  - Data reception, clock distribution + commands, reconstruction algorithms
- Artix XC7A35T FPGA → *Prototype working*
  - Clock configuration, remote reset, etc
  - Phase stability monitoring tools
- First prototypes expected for summer 2018



4 x Samtec FireFly modules connected to 2 MPO connectors

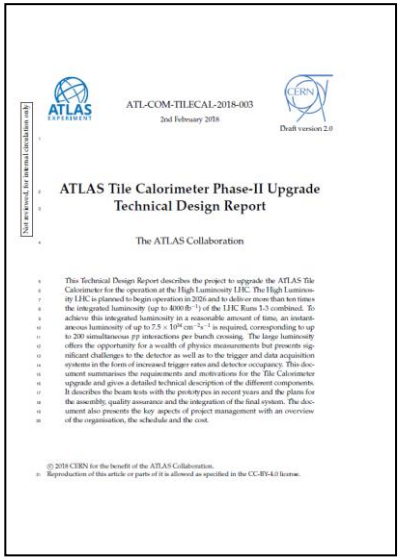


Artix FMC prototype



Milestones

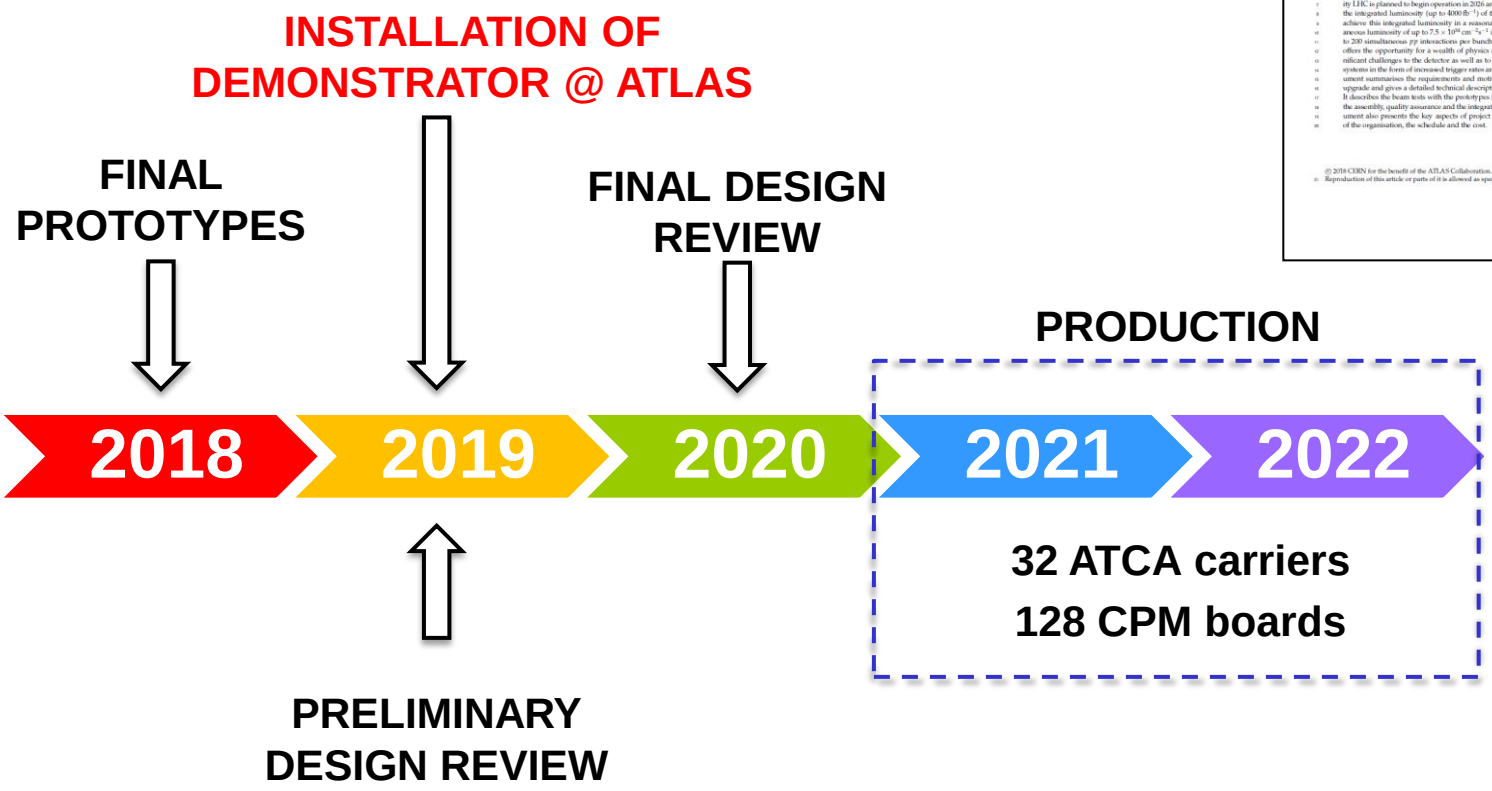
- Technical Design Report approved in March!


ATL-COM-TILECAL-2018-003
2nd February 2018
Draft version 2.0

ATLAS Tile Calorimeter Phase-II Upgrade
Technical Design Report

The ATLAS Collaboration

This Technical Design Report describes the project to upgrade the ATLAS Tile Calorimeter for the operation at the High Luminosity LHC. The High Luminosity LHC is planned to begin operation in 2026 and to deliver more than ten times the integrated luminosity (up to 4000 fb^{-1}) of the LHC Runs 1-3 combined. To achieve this integrated luminosity in a reasonable amount of time, an instantaneous luminosity of up to 7.5 × 10^{34} cm^{-2}s^{-1} is required, corresponding to up to 200 simultaneous pp interactions per bunch crossing. The large luminosity offers the opportunity for a wealth of physics measurements but presents significant challenges to the detector as well as to the trigger and data acquisition systems in the form of increased trigger rates and detector occupancy. This document summarises the requirements and motivations for the Tile Calorimeter upgrade and gives a detailed technical description of the different components. It describes the beam tests with the prototypes in recent years and the plans for the assembly, quality assurance and the integration of the final system. The document also presents the key aspects of project management with an overview of the organisation, the schedule and the cost.

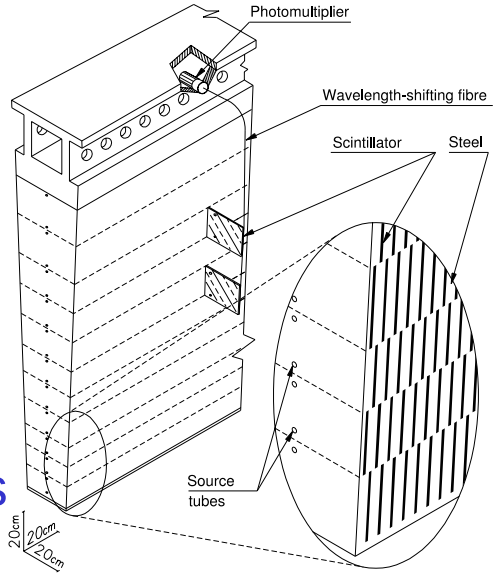


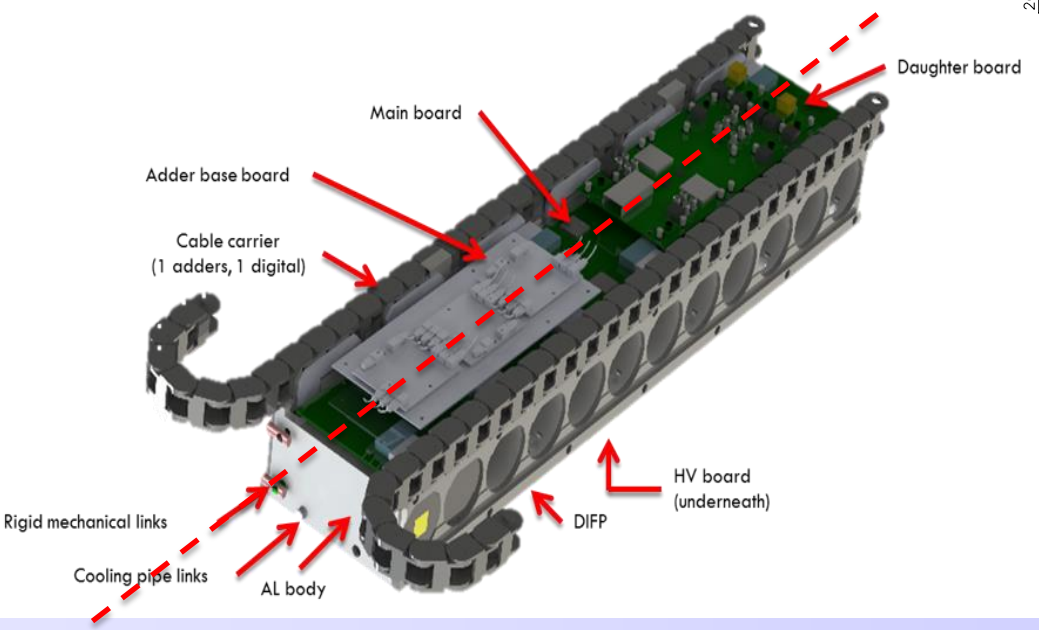
Gracias por su atención

BACKUP

Upgraded front-end electronics

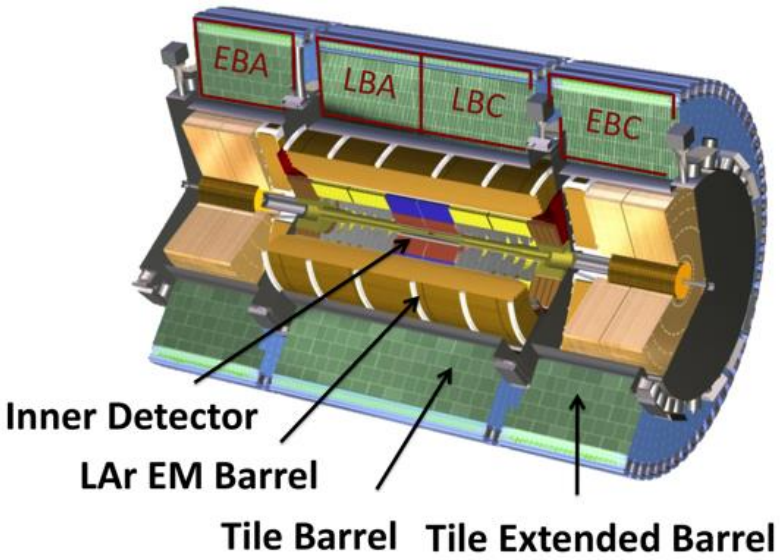
- **New mechanics** and extraction tools
  - Allow access in reduced detector standard opening
- Each module hosts 4 mini-drawers:
  - 12 PMTs + 12 Front-End cards (3-in-1 cards)
  - 1 MainBoard + 1 DaughterBoard
  - 1 HV regulation board: Internal or Remote option
- 1 LVPS: low power distribution for readout electronics

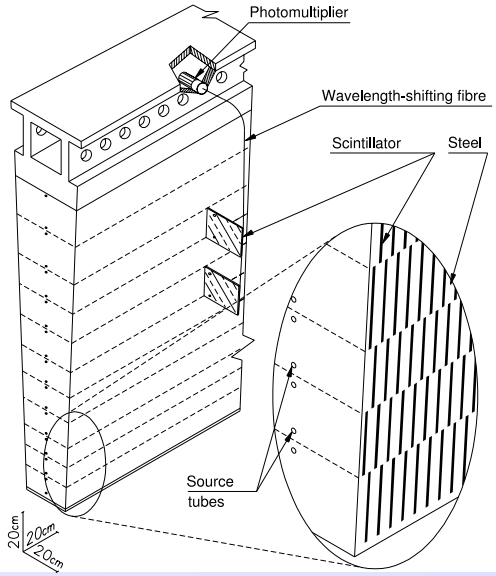




Tile Calorimeter

- Measures energies of hadrons, jets, τ-leptons and E_T^{miss}
- Segmented calorimeter of steel plates and plastic scintillator tiles which covers the most central region of the ATLAS experiment (up to $|\eta| = 1.7$)
- 4 partitions: EBA, LBA, LBC, EBC
- Each partition has 64 modules
  - One drawer hosts up to 48 PMTs



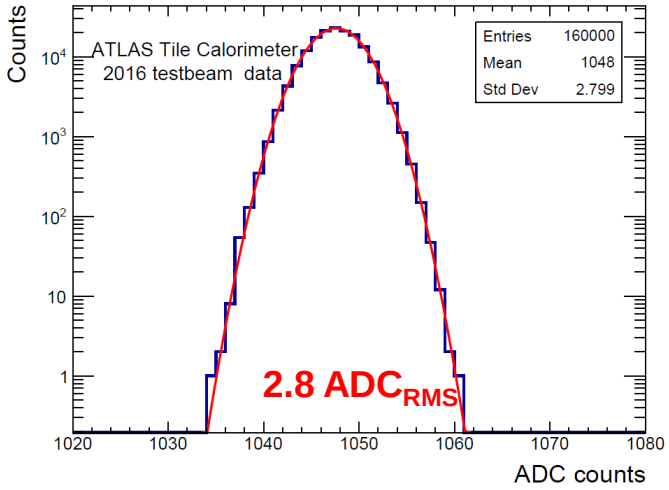


- Scintillator tiles are read out using wavelength shifting fibers coupled to PhotoMultiplier Tubes (PMTs)
- Around 10,000 readout channels

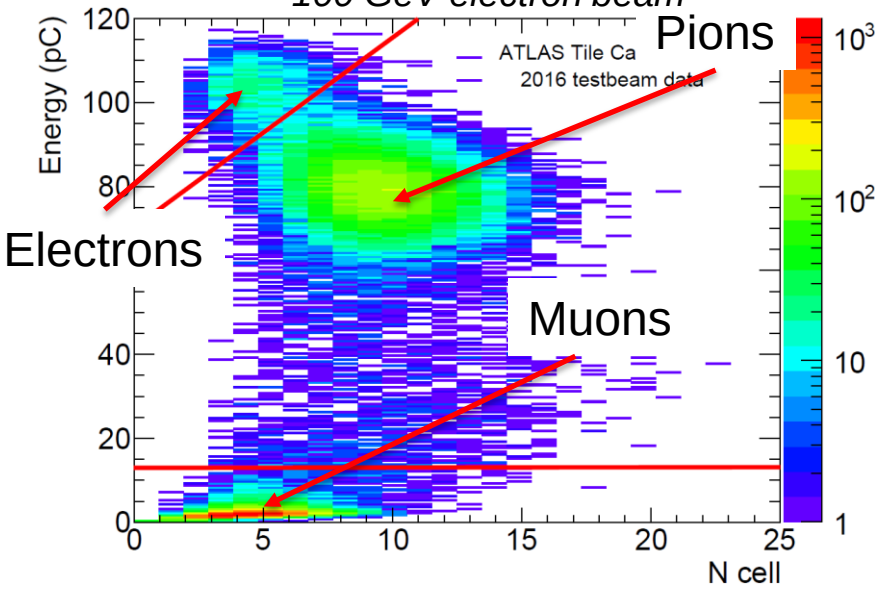
Testbeam Results

- Characterization of the electronics performance
  - Robustness and stability of the system
  - Electronics noise in PMT signals
- Extense physics program
  - Study response to muons, electrons and hadrons with different energies
  - Beam positions at 20º, 90º and η positions

Pedestal run with the upgraded 3in1 card



100 GeV electron beam



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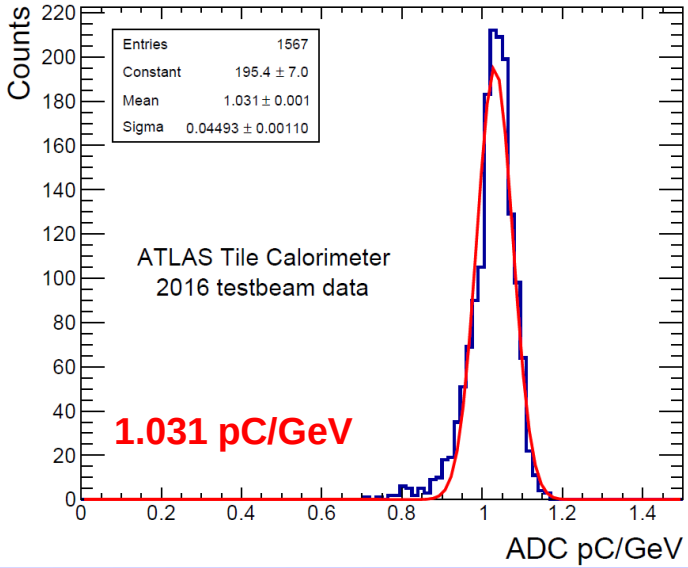
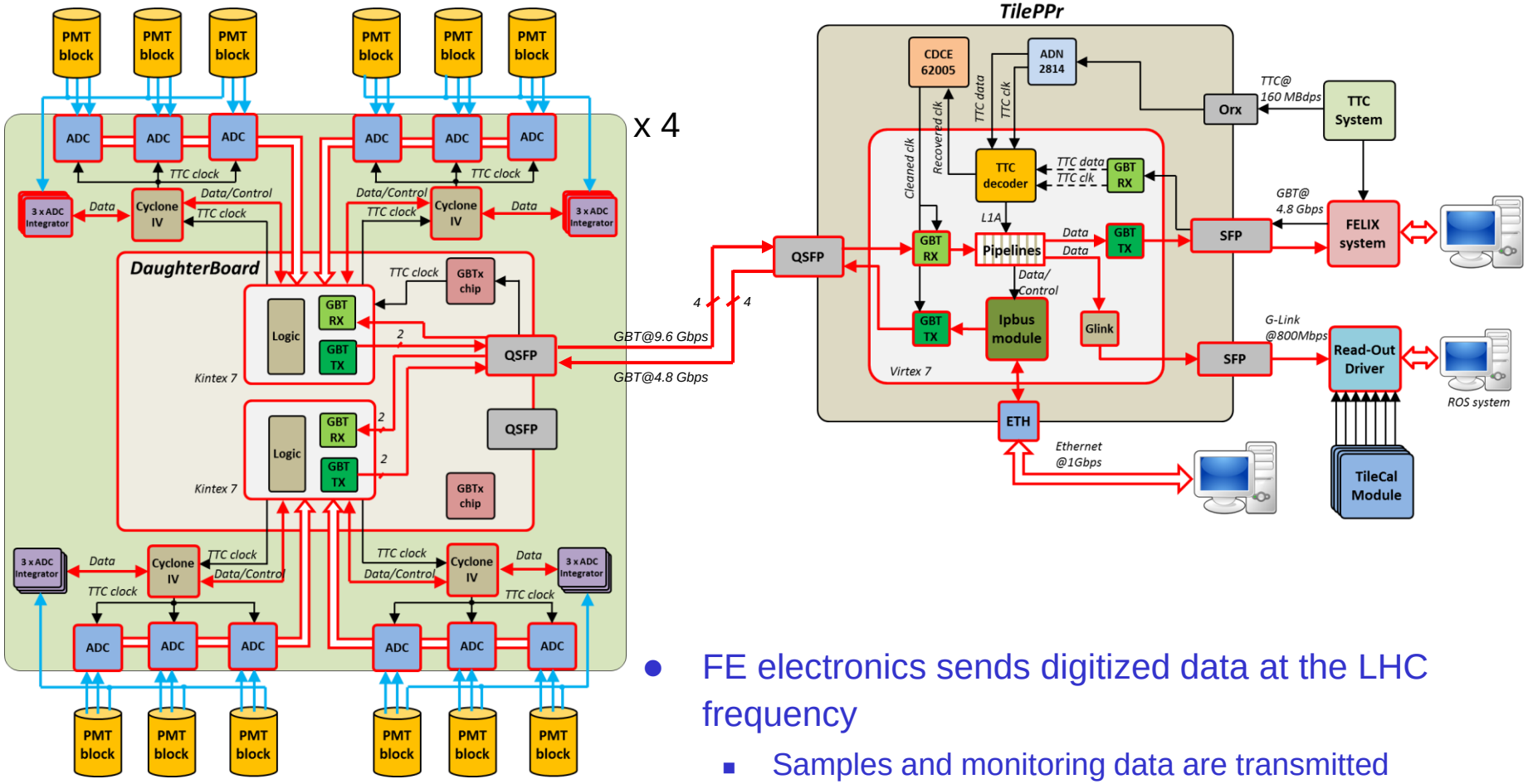


Clock and dataflow in the TB



- FE electronics sends digitized data at the LHC frequency
  - Samples and monitoring data are transmitted
- Two independent readout paths through the TilePPr
  - FELIX system prototype
  - Legacy Read-Out Drivers