Design and fabrication of HV-CMOS chips for the LHC upgrade

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Outline

- Overview
- Project proposal & status:
  - WP1 : RD50 Design
  - WP2 : Test
  - WP3 : Exploitation and RD
- Conclusions

Overview

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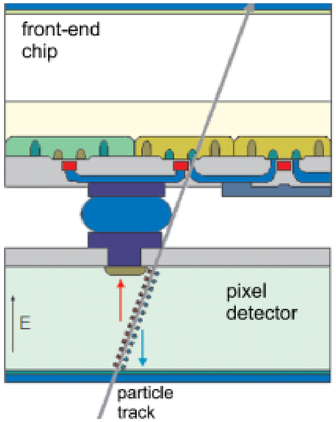
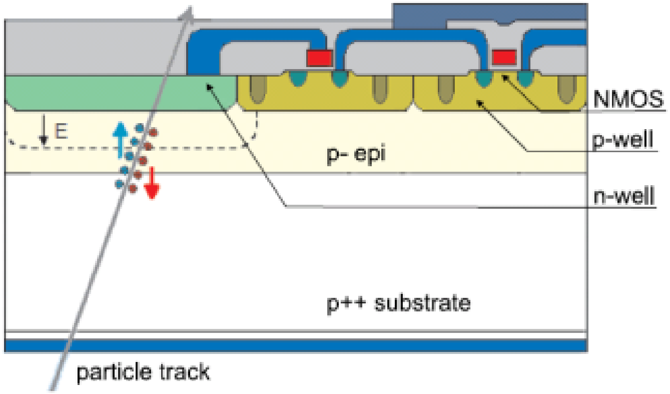
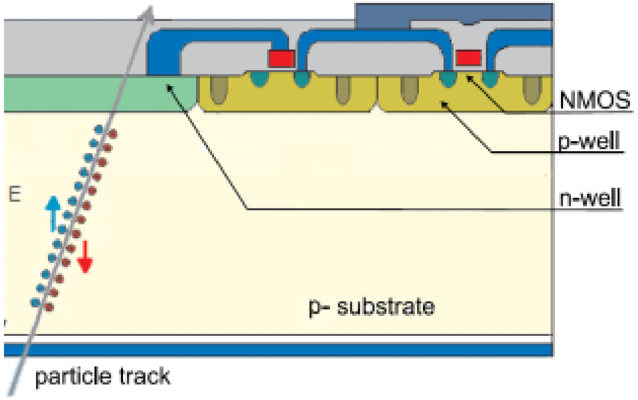
Hybrid Pixel Detectors



Monolithic Pixels



Depleted Monolithic Pixels



- Standard Hybrid Pixels vs **Active CMOS Sensor Hybrid Pixels**
  - Possibly no reduction of assembly cost: capacitive coupled CMOS sensors (glued instead of bump bonded) still need electrical connections
  - CMOS sensors have higher analog power consumption
  - Physics case for inner layers: improved spatial resolution with sub pixel encoding (still needs to be proven)

➔ No strong use case for Active CMOS Sensor Hybrid Pixels for HL-LHC

- Standard Hybrid Pixels vs **Monolithic Pixels**
  - Competition only for outer layers (rad. tolerance, pixel size)
  - Challenging task to integrate digital R/O (x-talk, logic density)
  - Huge savings in silicon and assembly costs

Let's prove it!

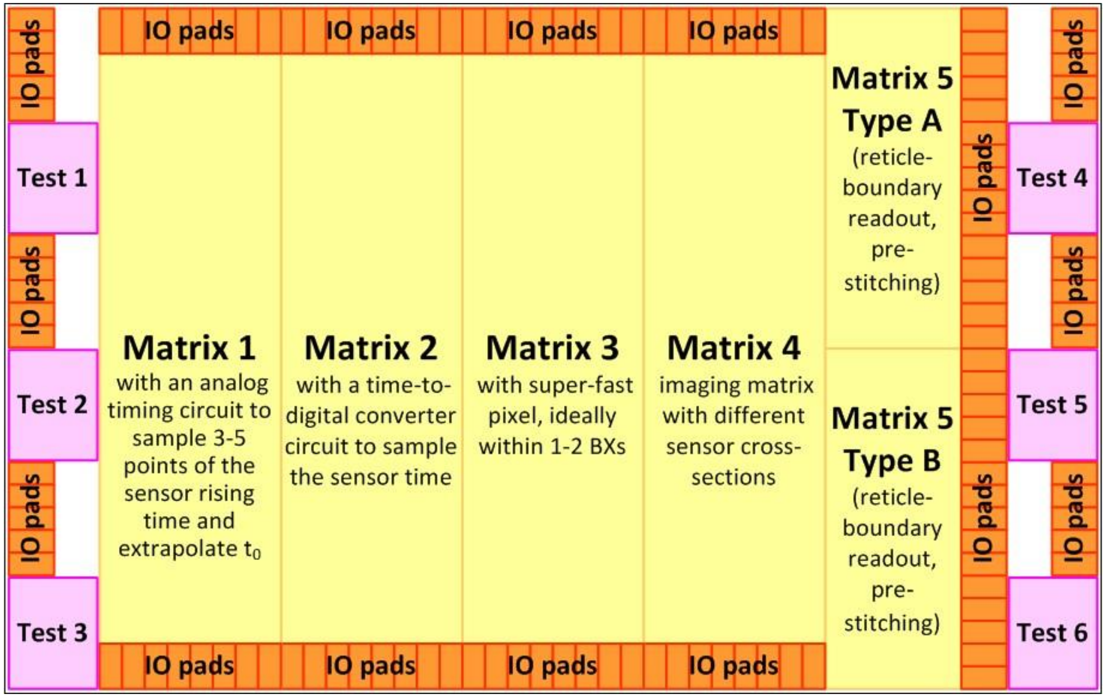
H. Krüger, FEE 2016, Krakow

Project proposal

The project is divided in 3 tasks:

- WP1:Hybrid and Monolithic HV-CMOS chip designs
  - Analog sampling matrix in RD50
  - Test structures
- WP2:Test of Hybrid and Monolithic HV-CMOS chip prototypes
  - Collaboration with Uni. Bonn
- WP3:Exploitation of results and RD for future colliders
  - Exploitation of the results from previous projects
  - New tests/new collaborations

WP1: RD50 Design



Test structure 1	Simple CMOS capacitors to study oxide thickness
Test structure 2	10 x 10 matrix of very small pixels with passive readout
Test structure 3	10 x 10 matrix of very small pixels with 3T-like readout
Test structure 4	Small matrix of pixels for TCT, e-TCT and TPA-TCT measurements
Test structure 5	Single pixels for sensor capacitance measurements
Test structure 6	…

<u>CERN/RD50 collaboration</u>:

- International project to develop radiation hard semiconductor devices for very high luminosity colliders

<u>Target of this submission</u>:

- Improve the timing resolution of HV-CMOS sensors with different solutions implemented at the readout circuit level
- Study new sensor cross-sections
- Study pre-stitching options (increase the device area beyond the reticle size limitation)

<u>Technology</u>:

- 150 nm HV-CMOS from LFoundry

<u>Design effort</u>:

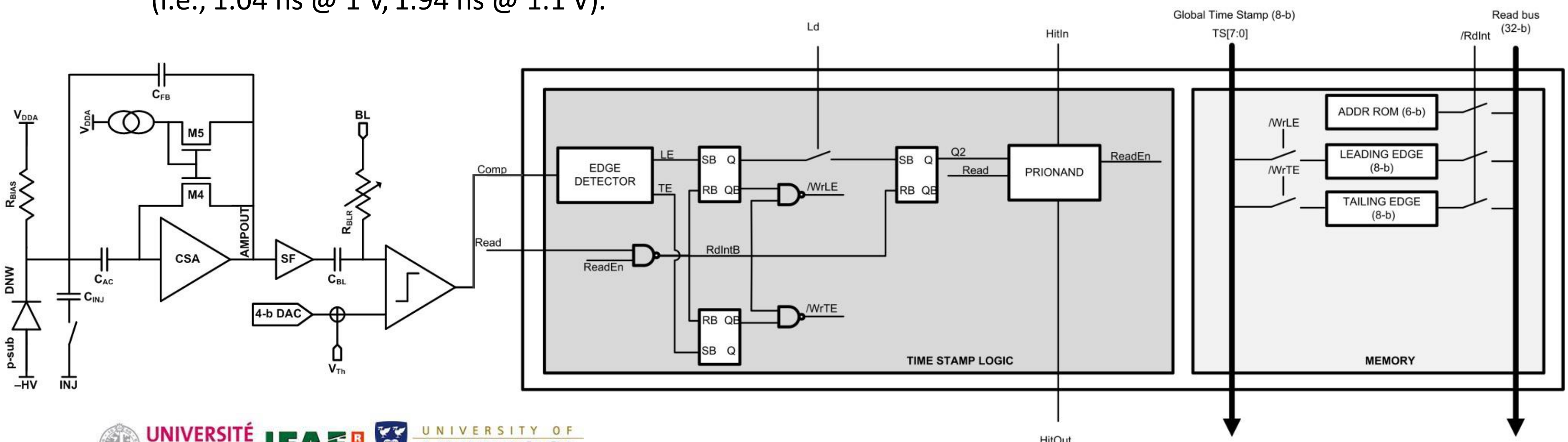
- IFAE (R. Casanova)
- Uni. Barcelona (O. Alonso)
- Uni. Liverpool (S. Powell, E. Vilella and C. Zhang)
- FBK (N. Massari and M. Perenzoni)

WP1: RD50 Design

RD50

The pixel in Matrix 1 includes:

- Sensor → 50 µm x 50 µm (~200 fF parasitic capacitance)
- Analog readout electronics → CSA, shaper, filter and comparator.
- Digital readout electronics → Electronics that sense the leading edge of the comparator and store the corresponding time-stamp in an 8-bit memory. The electronics also store the pixel address in another 8-bit memory (this info is not needed for the analysis presented in these slides).
- Sampling electronics → Chain of delay elements and sample & holds to store 5 analog voltages. The sample & holds sample the output voltage of the shaper. The delay elements put the sample & hold in hold mode when there is an event in the pixel. We can tune the delay with an external voltage (i.e., 1.04 ns @ 1 V, 1.94 ns @ 1.1 V).



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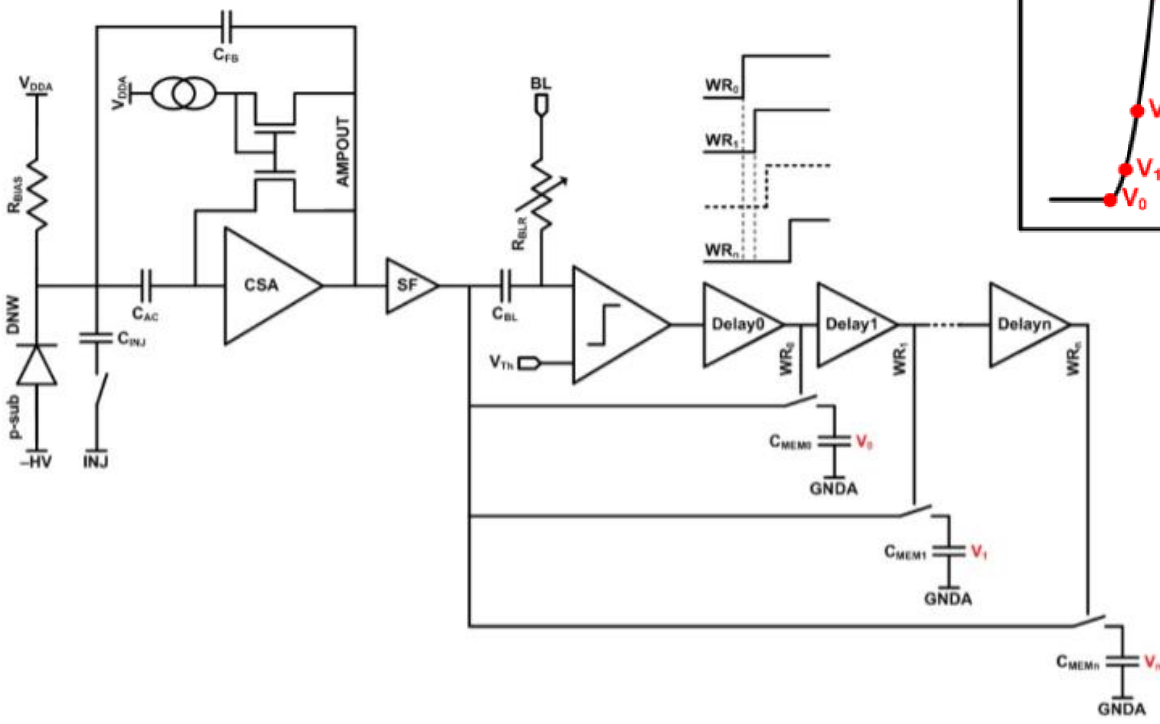
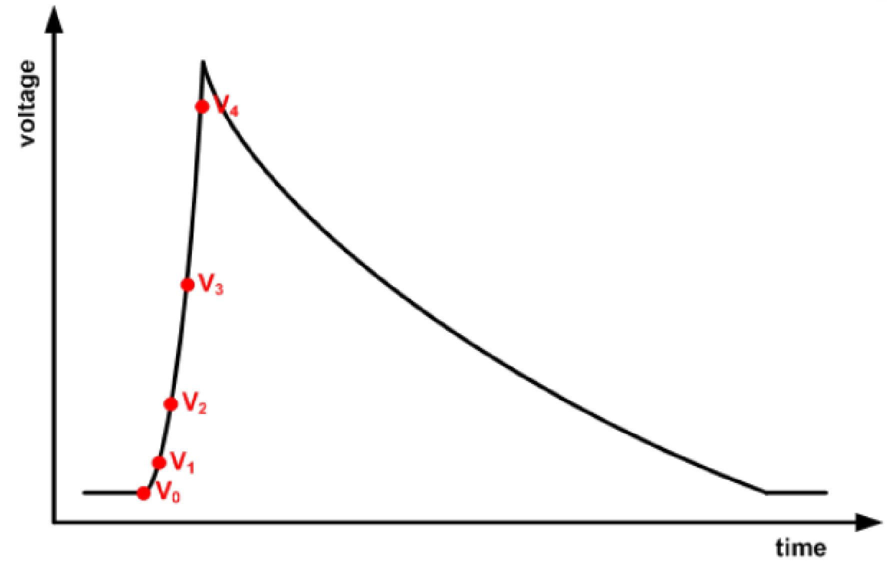
WP1: RD50 Design

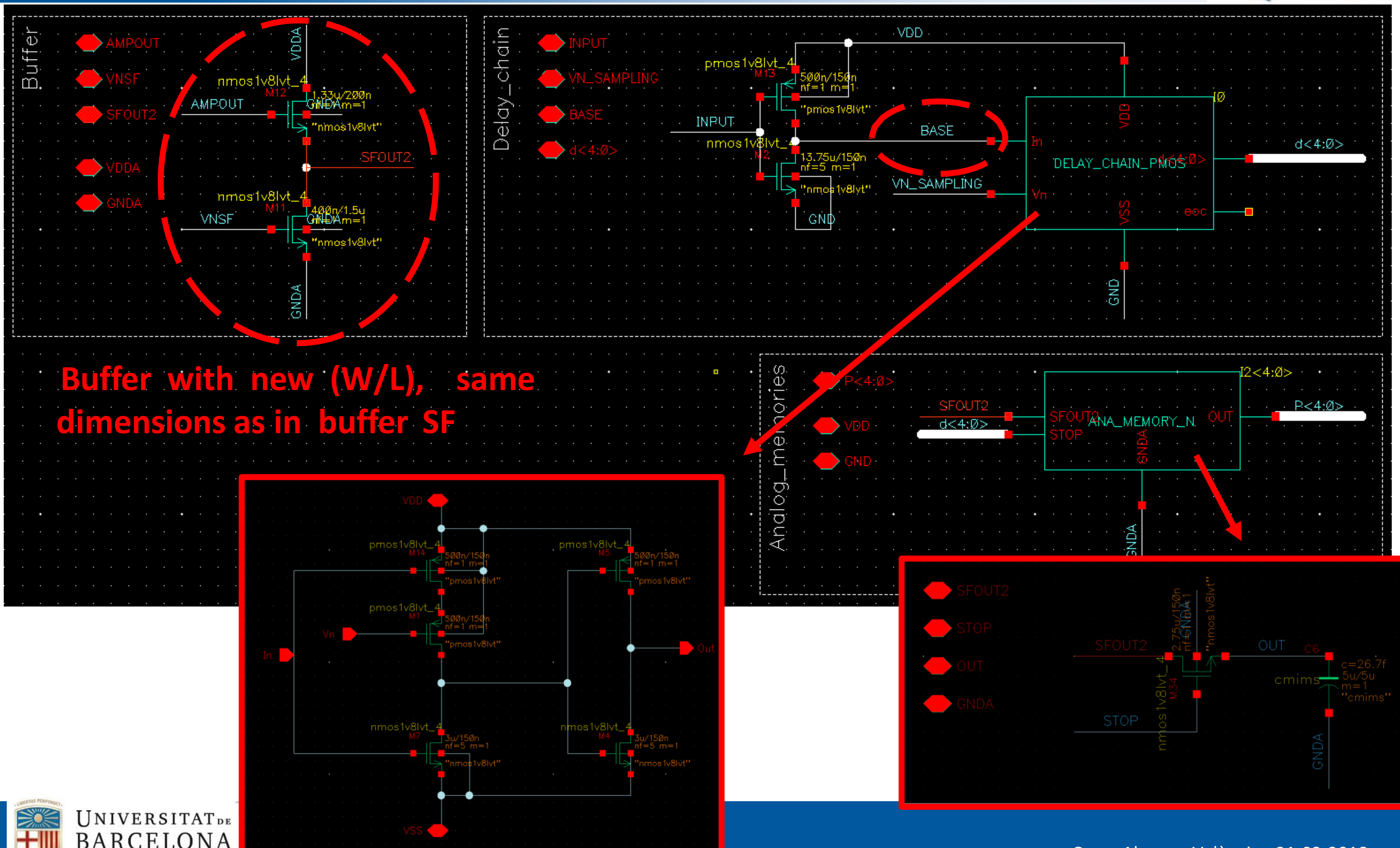
Simplified schematic and functionality





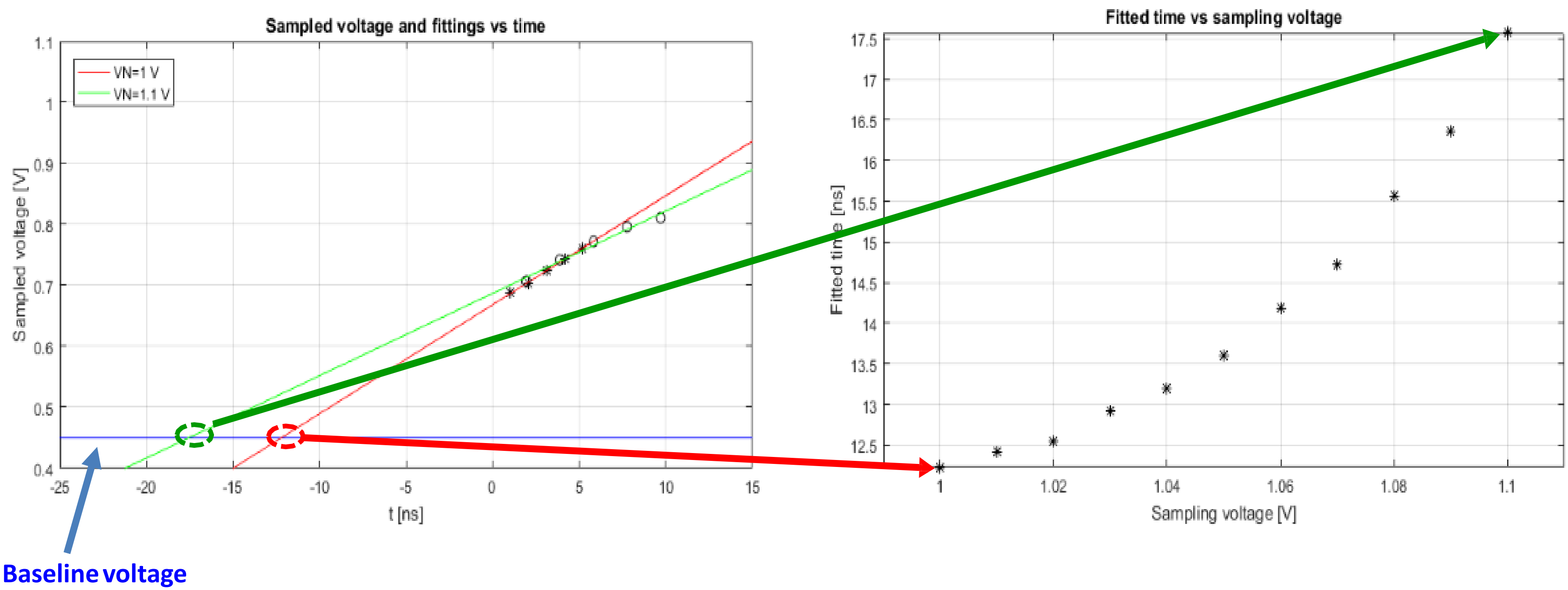
The main idea is to store up to 5 analog voltages.

WP1: RD50 Design

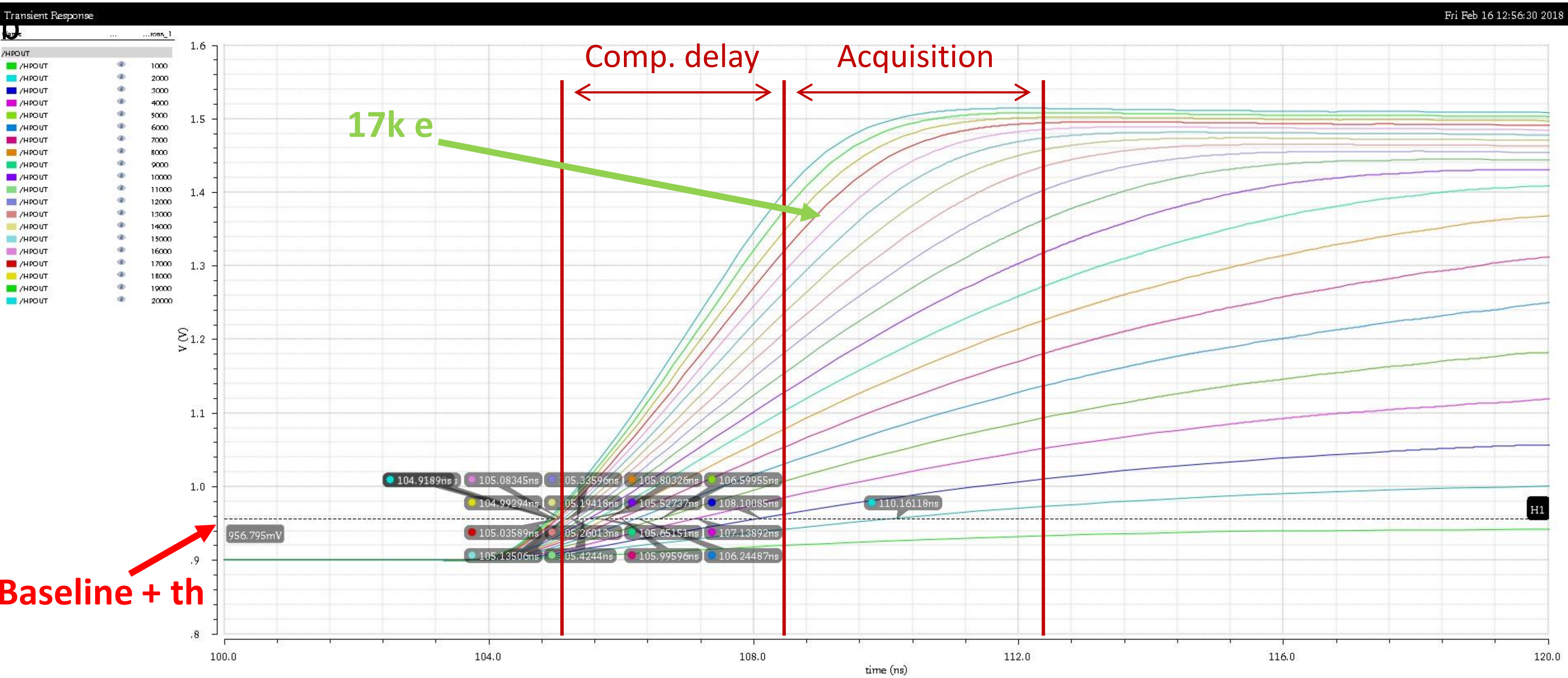


Buffer with new (W/L), same dimensions as in buffer SF

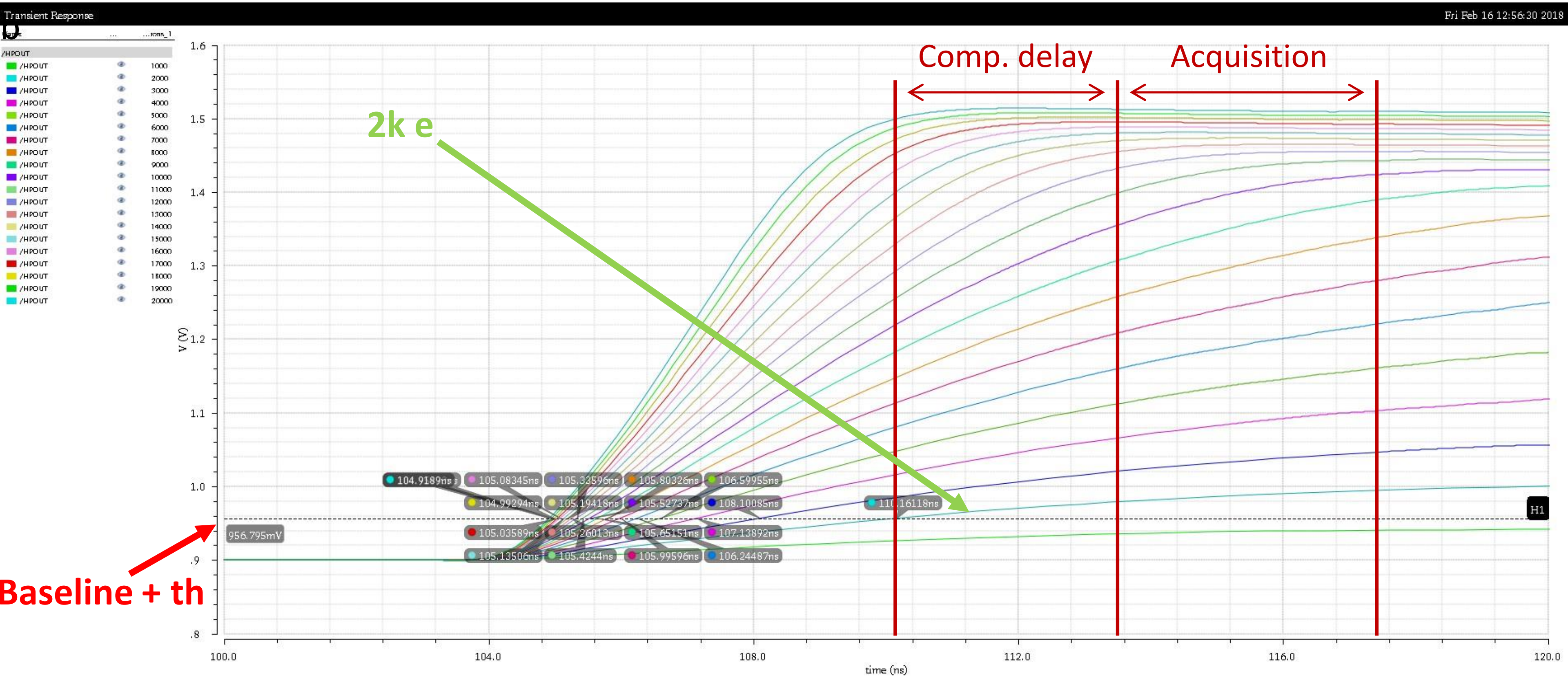
Input charge 6k e⁻ – Event time=1.022 µs



WP1: RD50 Design



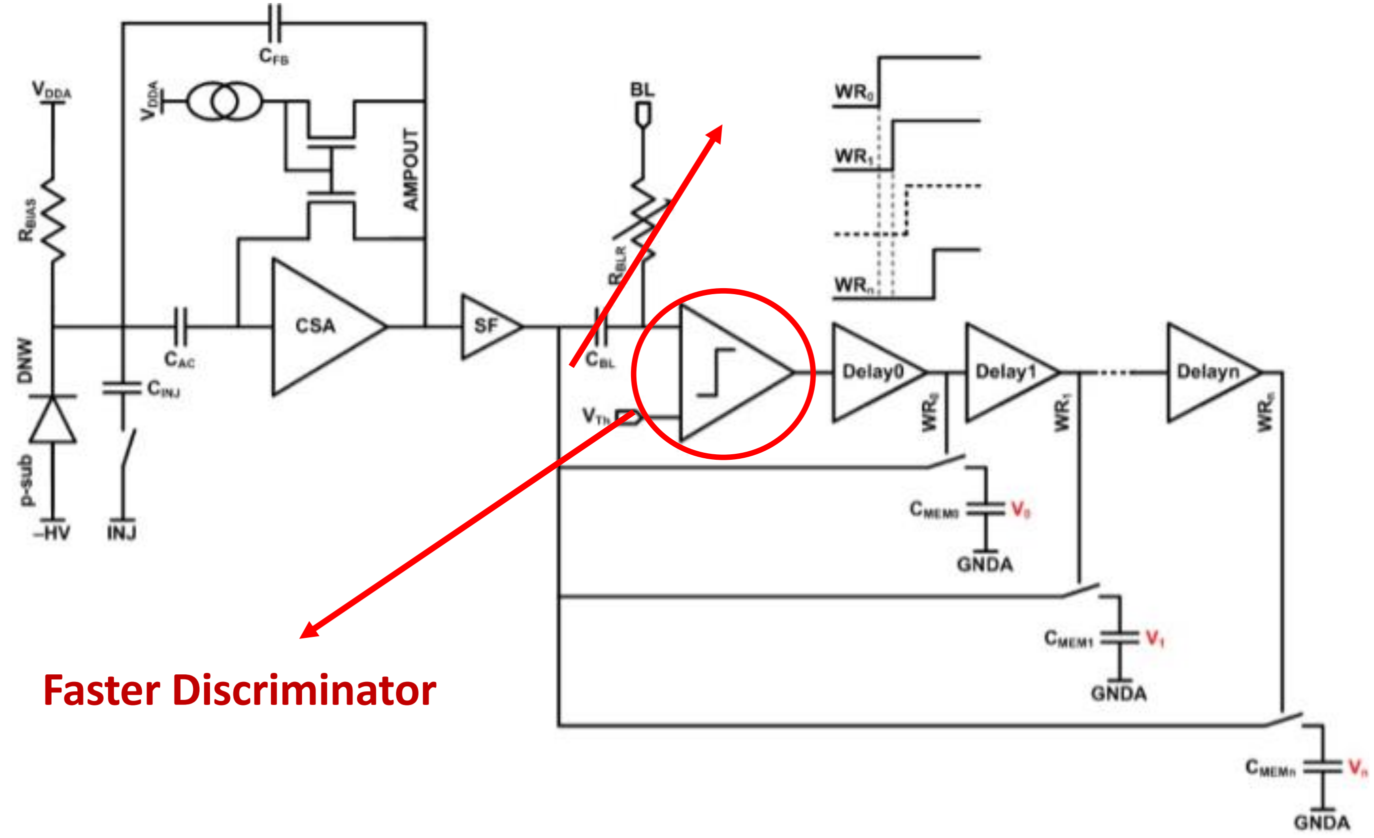
WP1: RD50 Design



Summary

- The quality of the method depends on:
  - Value of VN → How do we choose the appropriate value of VN?
  - Comparator time response
  - It also depends on the amount of input electrons
    - Better time resolution at larger amounts of input electrons
  - It also depends on the proximity of the real event time to the Cadence/chip time-stamp
    - An event happening at 1.022 μs gives a better time resolution than an event happening at 2.385 μs, as 1.022 μs is closer to the time-stamp (1 μs = 20 * 50 ns) than 2.385 μs (2.35 μs = 47 * 50 ns).
  - Time-stamp period

WP1: RD50 Design



Faster Discriminator

WP2: Test

WP2 activities are in collaboration with Uni. Bonn

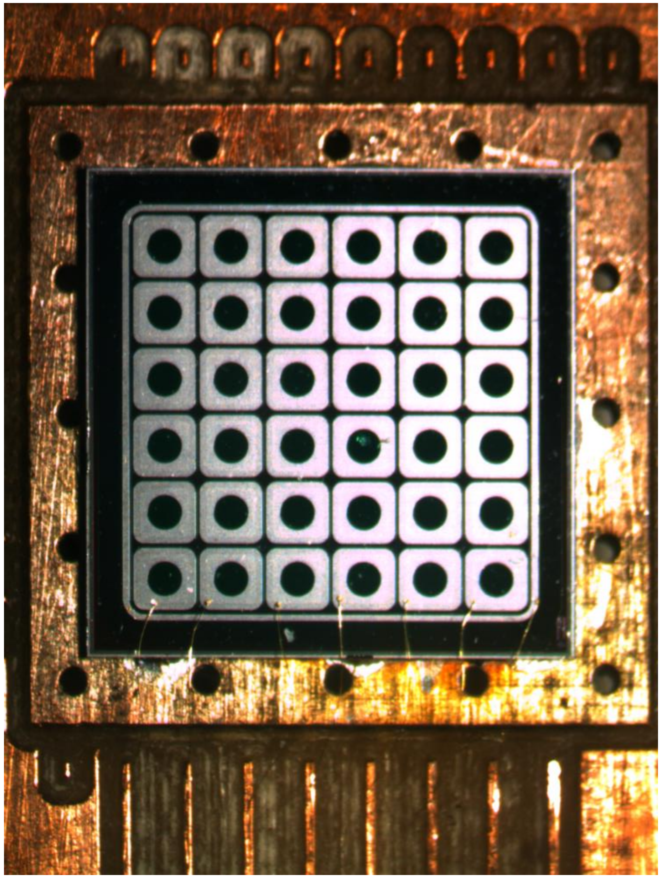
- Test of a fully monolithic CMOS Sensor (LF-Monopix)
  - DAQ and ASIC from Bonn
  - DAQ arribed to Bcn, waiting for Monopix
- Design of blocks for new submissions
  - Biasing ?
- Test of new submissions

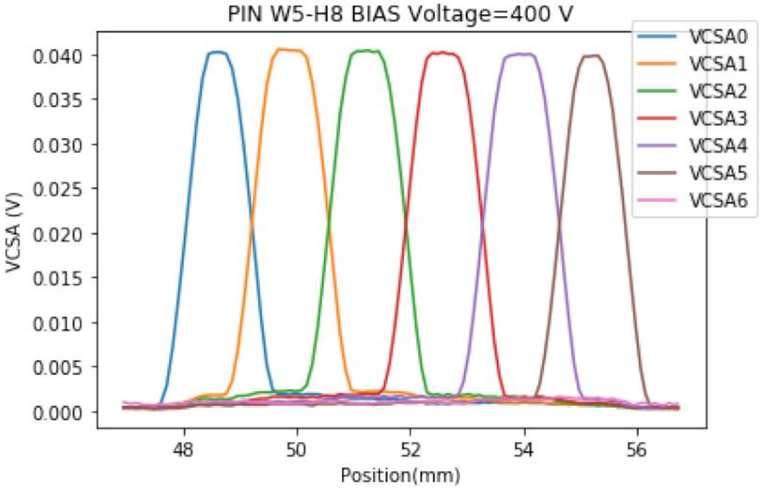
WP3: Exploitation and RD

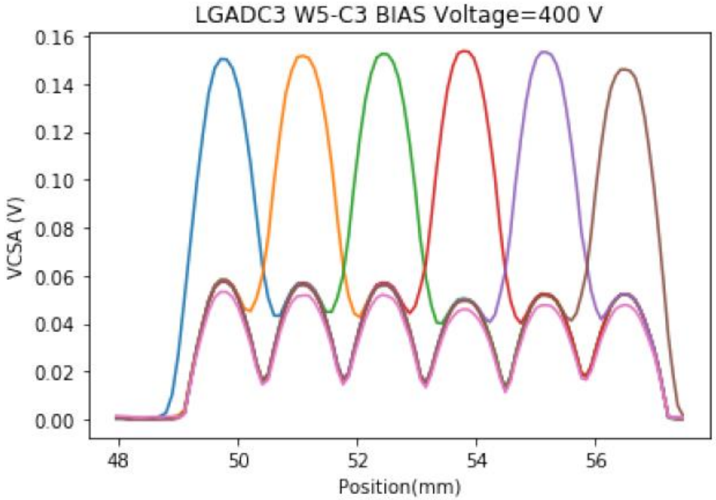
WP3 activities related to the previous project

- Test with PiN, LGAD and iLGAD pixels
- Test with LGAD strips
- Exploitation of results

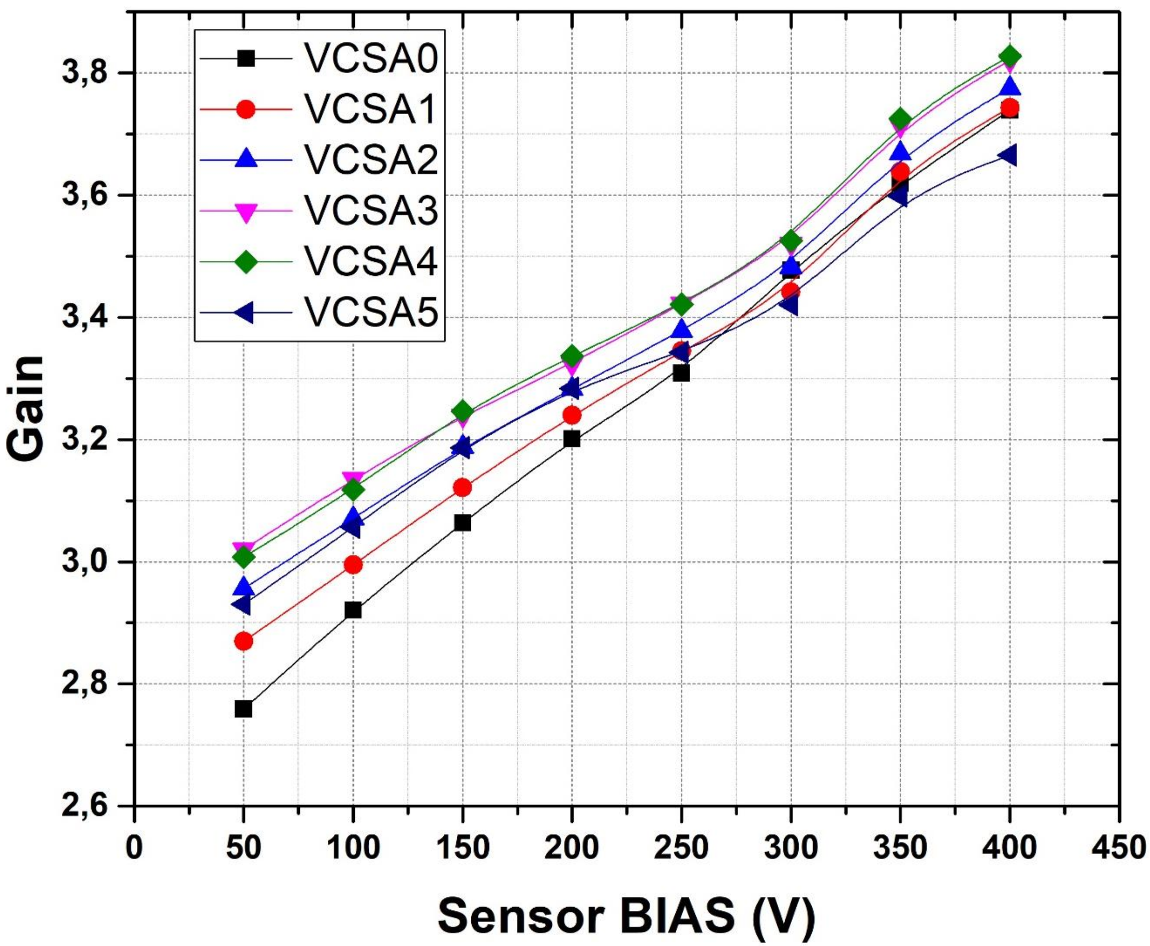
WP3: Exploitation and RD



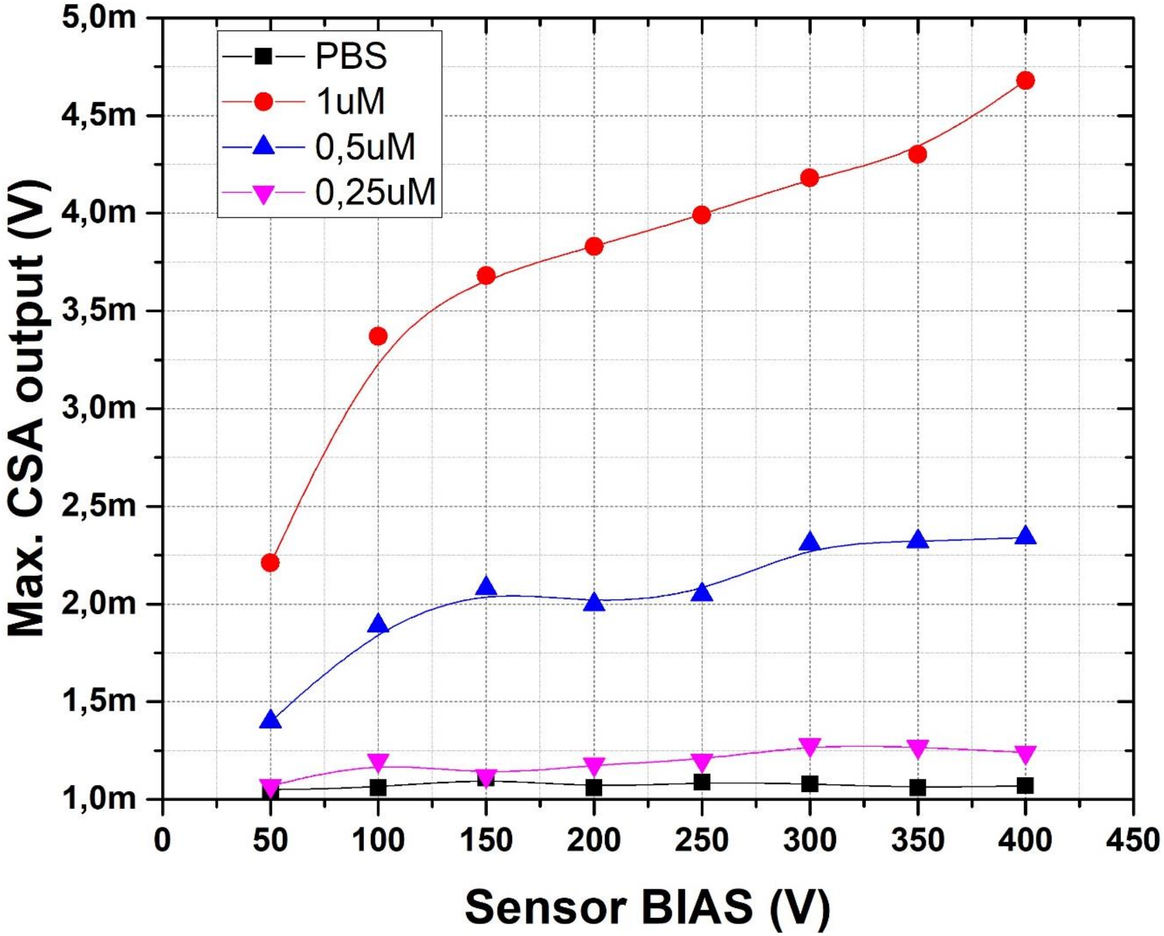




WP3: Exploitation and RD



WP3: Exploitation and RD



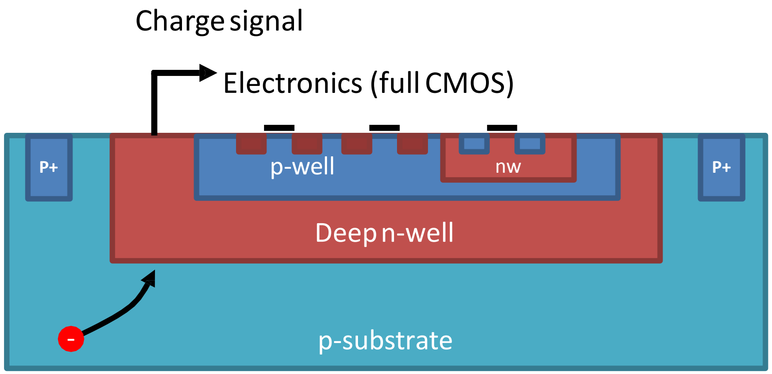
Conclusions and future plans

- The proposal has been granted with 110 k€ (approx.)
- The project is highly related to design activities:
  - RD50 submission (on going)
  - Future designs in collaboration with other entities
- Exploitation of old collaborations
  - Focused on Uni. Bonn
  - Opened to everybody
- Special WP devoted to test and exploit past projects

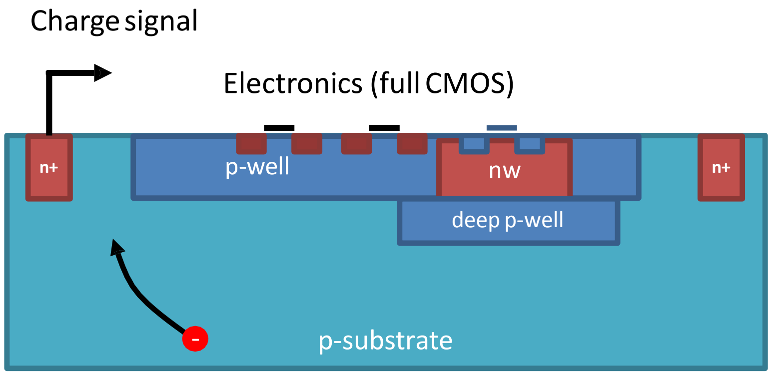
Concepto	Coste Imputable
Gastos de Personal	88.000 €
Viajes y dietas	17.395 €
Otros gastos	15.900 €
Adquisición inventariable	2.500 €
Alquiler inventariable	0 €
Mantenimiento inventariable	6.000 €
Fungible y similares	25.350 €
Total Costes Directos	**155.145 €**

Backup slides

Implementation Concepts – Read-out Node



Electronics **inside** charge collection well



Electronics **outside** charge collection well

- Collection node with **large fill factor** → no low field regions, radiation hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

- Very **small sensor capacitance** → low power
- Less radiation hard (longer drift lengths)
- Full CMOS with additional deep-p implant

H. Krüger, FEE 2016, Krakow