The Readout Driver for the ATLAS Hadronic Tile Calorimeter

Alberto Valero[a], Carlos Solans[a]

[a] *Instituto de Física Corpuscular*

Contents

1. Abstract

ATLAS is an experiment for the Large Hadron Collider (LHC) at CERN which will study proton-proton collisions with a 14 TeV center of mass energy. TileCal is the Hadronic Tile Calorimeter of ATLAS which is contains roughly 10000 photomultiplier channels. The Read-Out Driver (ROD) system is placed between the first and the second levels of trigger and it is responsible for receiving and packing the data collected in the detector and to provide reconstructed magnitudes for every channel at the first level of trigger rate (100 kHz) without introducing latency. The Optimal Filtering method has been selected to compute the energy deposited and the timing of the signals. In addition, the ROD system has to synchronize the data with the trigger information, provide online monitoring and perform algorithms for Level 2 triggers. In this paper it is described the complete Tile Calorimeter acquisition chain, followed by a detailed description of the ROD system covering the hardware and firmware of the ROD module, the online reconstruction algorithms and the control and configuration software.

2. Introduction

ATLAS [1] a general purpose experiment for the Large Hadron Collider (LHC), an accelerator where proton beams will collide each 25 ns with a 14 TeV centre of mass energy. TileCal is the Hadronic Tile Calorimeter [2] of the ATLAS detector within the LHC collider at CERN. The central element of the back-end system in the TileCal detector is the Read-Out Driver (ROD). The ROD system is located between the first and the second levels of trigger in the ATLAS data acquisition chain. The data produced in the detector is gathered and digitized in the front-end electronics and transmitted to the RODs through high-speed optical links. At the first level trigger rate the ROD system has to compute in real time information from 9856 front-end channels in less than 10 μs. Finally, the processed data are transmitted through optical links to the Read-Out System (ROS) located in the second level trigger.

3. The ATLAS Tile Calorimeter Read-out

TileCal is divided into 3 barrels, a central barrel 5.6 m long and two extended barrels 2.9 m long. The inner radius of the detector is approximately 2.2 m and the outer radius approximately 4.2 m. Each barrel is divided azimuthally into 64 wedges, the so-called modules. The TileCal modules are sampling devices made out of steel as the passive medium and scintillating tiles as the active material. The absorber structure is a laminate of steel plates of various dimensions, connected to a massive structural element referred to as a girder. The tiles are read out on both sides by wavelength shifting fibers which carry the light to the photomultiplier tubes (PMT) located in the front-end electronics. The tiles are distributed in three radial samplings, A and BC type cells with η x ϕ = 0.1 x 0.1, and D type cells with η x ϕ = 0.1 x 0.2.

3.1. The TileCal Read-out chain

The front-end electronics are located in the outermost edge of each TileCal module in so called super-drawers [3]. Each superdrawer can hold up to 48 PMTs and the electronics for their read-out. The signal collected in the PMT is shaped in the 3-in-1 cards [**?**], where it is sent to the integrator system used for calibration and minimum bias monitoring, to the trigger summation cards for the trigger decision and to the amplifiers. In order to achieve the required 16-bit dynamic range a bi-gain amplification system with a high gain to low gain ratio of 64:1 is used. The high and low gain data is digitized in 8 digitizer boards at a sample rate of 40 Mbps. All samples are stored in a pipeline of about 2 μs while the first level trigger decision is received. If an event is selected the 7-sample event frame, 2 samples for the pedestal and 5 sample for the peak measurements are transmitted to the Interface Board (IB) [4]. One IB collects and packs the digitized data for all the channels of each module. Then, the IB computes a CRC for error detection and sends the event data through two different optical front-end links to the off-detector electronics. In the back-end electronics the data is received redundantly in the Optical Multiplexer Board (OMB) which recomputes the CRC and transmits the correct data to the RODs. The RODs are placed after the Level 1 Trigger decision (Figure 1) and provide reconstructed data to the Read-out system (ROS) for Level 2 Trigger algorithms.

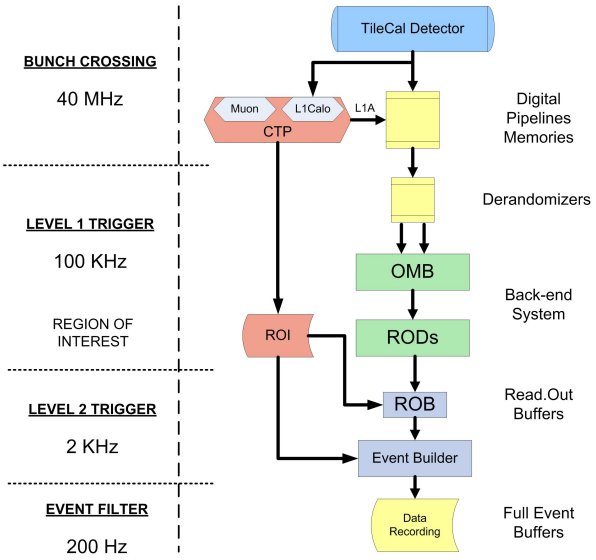

Figure 1: Trigger Levels for TileCal detector.

3.2. Regions of Interest

A geometrical region of the ATLAS detector described in units of pseudo-rapidity (η) and azimutal angle (ϕ) defined by the Level 1 trigger is a Region of Interest (ROI). These are used by subsequent trigger levels to perform High Level Trigger (HLT) algorithms on the data. TileCal is segmented into different η regions with ϕ symmetry with the purpose to serve different physics searches in transverse momentum (p_T). TileCal electronics are divided into two high p_T regions ($-0.7 < \eta < 0$ and $0 < \eta < 0.7$) and two low p_T regions ($-1.2 < \eta < -0.7$ and $0.7 < \eta < 1.2$). Each one with its own TTC units for synchronization and trigger [5], so they can be operated as independent detectors. Each partition is composed by a TTC and a ROD crates which has communication with the Central Trigger Processor (CTP) for trigger management, reception of Level 1 Accept trigger signals as well as the TTC commands and data to handle reset messages, calibration triggers and control and test parameters. The handling of this information is done through the TTC crate. In addition, the TTC crate collects the busy signal from RODs and transmits it to the CTP when the input buffers of RODs are nearly full. The ROD crate holds a Trigger and Busy Module (TBM) [6] as interface with the TTC crate. The TBM is used to collect and transmit to the TTC crate the busy status of all the RODs in the crate and to distribute to all the RODs the TTC information received from the TTC crate. The ROD crate also hold 8 ROD modules for data processing and 8 Transition Modules (TM) for data transmission to the Read-Out System (ROS). According to the ROIs found in the event by the CTP, the HLT proccessors receive a sub-set of the event data from the ROS, which reduce considerably the network bandwidth required for the trigger decision. In addition, the TileCal back-end partitioning allows the HLT to access ROI data from individual hardware, reducing the number of connections needed to get the ROI data (Figure 2).

3.3. The ROD module

The ROD motherboard represents the core implementation of the ROD crate. It is based on a standard 9U VME64x board. A ROD can be equipped with up to four Processing Unit (PU) which are Digital Signal Processor (DSP) based pluggable daughterboards responsible for the data processing. Nevertheless, for TileCal requirements, only two PUs are used. A 9U TM is plugged in the rear part of the crate to hold up to 4 S-Link Source Cards which convert the electrical output data to a high speed optical line. For TileCal ROD with only two PUs, only 2 S-Link Source Cards per TM are needed. The block diagram of

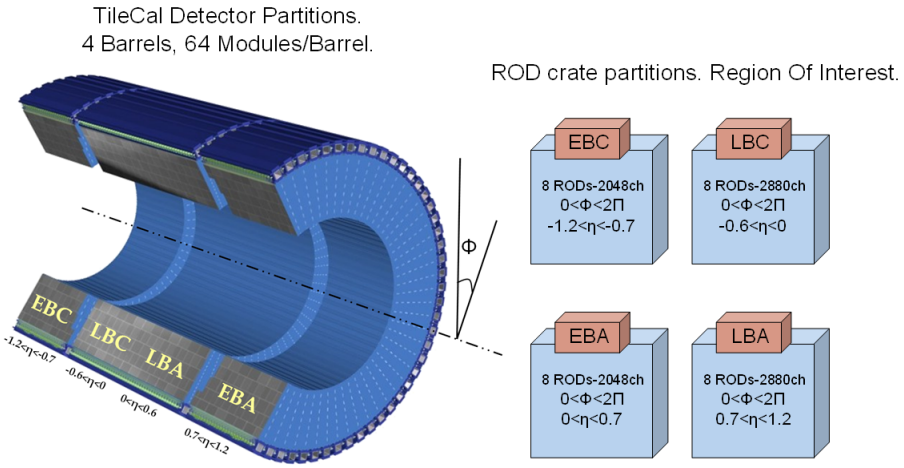

Figure 2: TileCal detector and back-end system partitions.

the motherboard and the rear TM is shown in Figure 3. There are three main important data paths to be emphasized due to the different tasks they perform in the board (Figure 4).

- Dataflow: the input data coming from an optical fiber is received by eight optical receivers and deserializer G-Link chips to be distributed into four Staging FPGAs. The main function of the Staging FPGA is to configure the distribution of the superdrawer data into the PUs. In the PU, the data is processed and formatted in less than 10 μs and the output data are buffered in the PU FIFOs and received by the Output Controller FPGA (OC). There are four OCs in the ROD motherboard which configure the output data distribution. For TileCal requirements only 2 OC are used. The OC may store the data either in an SDRAM to send the event fragment through the VME bus or send it directly to the ROS through the TM S-Link LSC cards. The S-Link mode read-out is used for ATLAS operation whereas the VME read-out is used for Detector Verification System (DVS) tests []. A FIFO and a small PLD device to control it, is mounted in the TM to get more output buffering than the provided with the S-Link LSC before asserting an XOFF signal which will stop the data transmission from the OC. The dataflow path is shown in Figure 4.

- Timing, Trigger and Control signals and Busy signals: the ROD receives the trigger clock and related information from the VME P3 backplane. These data are then decoded and managed by a TTCrx asic (REF) and the TTC FPGA before they are sent to the PUs to synchronize the front-end and TTC data. The Busy signal is issued by the DSP when its input buffer is almost full. There are 4 individual Busy signals which are OR-ed at the VME FPGA and sent through the VME P3 backplane to stop undesired triggers inducing dead-time.

- Control and monitoring from ROD controller (VME): the VME slave core of the ROD is implemented in the VME FPGA. The VME bus is usually used to configure and read the status of the motherboard devices. Furthermore, the ROD controller monitors the G-Links temperature, boot the PU FPGAs and DSPs and download online histograms also from VME. The main components of the ROD module are presented in Figure 3 and their main functionalities are described in the following subsections.

3.3.1. The optical receiver

The data coming from front-end through the OMB is received in small mezzanine cards called Optical Receivers (ORx). These ORx modules have an optical to electrical converter and an amplifier to provide constant-level output and controlled edge electrical signals in PECL. These signals contain the serial data

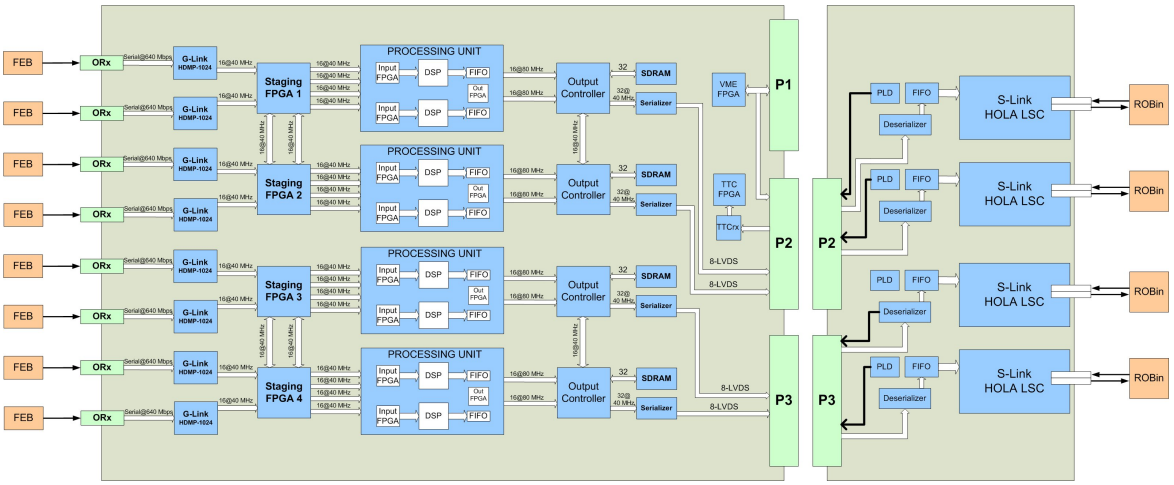

Figure 3: ROD motherboard block diagram and Transition Module.

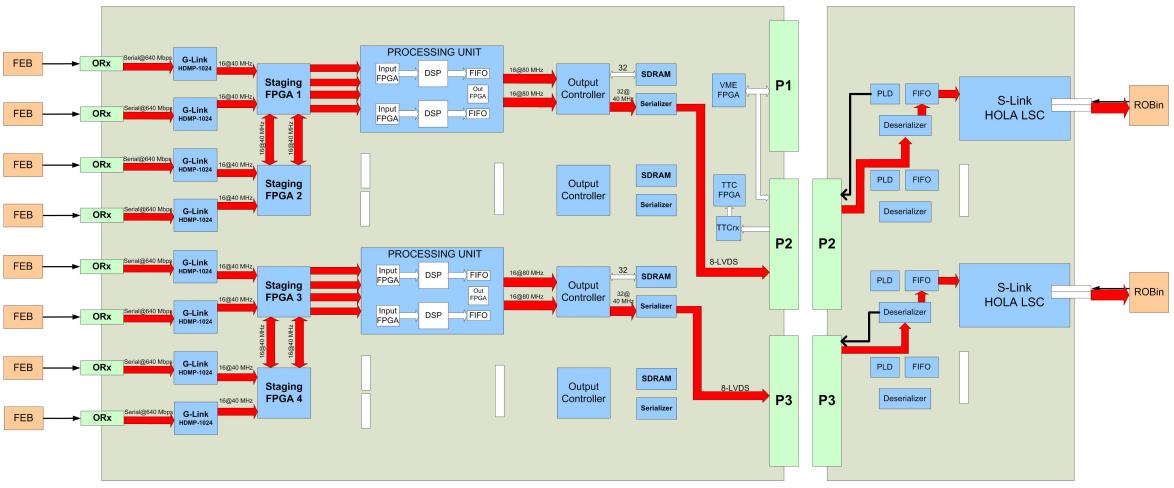

Figure 4: ROD motherboard block diagram dataflow in TileCal configuration.

to be sent to the G-Link chipsets in the motherboard. There are eight ORx per ROD located in the front panel which allow the read-out up to 8 FEBs with a single ROD motherboard.

3.3.2. The G-Link chip

There are 8 G-Link chips mounted in a ROD. The G-Link chip deserializes the data previously serialized in the other size of the optical link. The data is deserialized in the ROD motherboard by the HDMP-1024 and the 16bit@40MHz data sent to the Staging FPGA chip together with additional protocol signals. Two local oscillators chips and clock buffers provide 40.00 MHz reference clocks for the internal PLL of the 8 G-Link chips.

3.3.3. The Staging FPGA

There are 4 Staging FPGA chips per ROD. The Staging FPGA represents the input data distributor in the ROD. Each Staging FPGA receives the data directly from two ORxs. This data may be transmitted to the corresponding PU or to another PU through a neighbor Staging FPGA. The main functionalities of the Staging FPGA are:

- Receive deserialized data from 4 G-Links in TileCal operation Mode, so called Staging Mode, and to route them to a Processing Unit (PU).
- Provide a clock de-skew between the G-Link clock and the PU clock with a dual-clock FIFO implemented inside the device.
- Provide G-Link reset and configuration.
- Provide VME access for configuration and status.
- Monitor the G-Link temperature and make it available to the VME interface with a read only register (current, maximal and minimal values) and to the slow control system.
- Send test data from an internal RAM (VME writable) to the PU for debug and test purposes. The G-Link temperature is very important in order to monitor the chips performance (REF). The temperature measurement is implemented with a thermistor glued to each G-Link and with an ADC which also includes an internal voltage reference, an input analog multiplexer and a serial digital output to the Staging FPGA.

3.3.4. The Output Controller FPGA

There are 4 Output Controller FPGA per ROD, but only 2 are used due to the TileCal requirements. They act as the output data distributors of the ROD motherboard and send data to the ATLAS DAQ system. In TileCal operation mode, data from one PU is sent to one S-Link LSC card which is connected to one ROB input (ROBin) [**?**] through a read-out link. The tasks to be performed by the OC are:

- Read the DSP reconstructed output events from the PU output FIFO (16bits@80MHz) and to add S-Link header and trailers words to the output data according to the ATLAS TDAQ data format.
- Provide control (R/W) and status (R) registers accessible through VME.
- Transmit data either to the SDRAM (VME readout) or to the serializer (S-Link Readout).

3.3.5. The VME and Busy FPGA

There is one VME and Busy FPGA in each ROD to provide communication between the ROD controller and the devices in the ROD motherboard: 4 PUs, 4 Staging FPGAs, 4 OC FPGAs and 1 TTC FPGA. Additional features implemented in this device are:

- The Busy logic and Busy monitoring system.

- The interrupts handling from the controller devices to signal special actions to be taken by the ROD controller when some event occurs.
- The JTAG Boundary Scan, to be able to program the ROD FPGAs remotely from the ROD controller without physical access to the crate with a JTAG programming cable.

The communication of the VME FPGA with the ROD motherboard is handled with 2 protocols:

- Communication with the ROD controller: based as a standard VME64x slave core for single R/W cycles and block transfers with a D32 data bus and a A32 addressing for data transfer, and a A24 addressing for CR/CSR.
- Communication with the ROD motherboard devices: this is based in a custom protocol based in 5 serial lines. One unidirectional line managed by the VME FPGA to flag the control/address data, and 4 bidirectional lines for the serialized 4 bytes of the 32-bit word (Byte[3][0]). In case of the Staging FPGA the bus is daisy-chained to avoid extra routing lines in the PCB.

3.3.6. The TTC FPGA and TTCrx chip

The trigger information is received at ROD level coming from the TBM (after an optical to electrical conversion) and through the P3 backplane in differential LVDS format. All TTC connections are 100 Omh point to point (which corresponds to the characteristic impedance of the CP3) which are ended with a 100 Ohm resistor near the ROD LVDS receiver. The differential TTC signals contains information about the A and B channels of the TTCvi as well as trigger information and commands. They are decoded in the TTCrx chip and managed by the TTC FPGA which distributes the TTC information to each PU in a serialized point to point connection. The information needed by the ROD is:

- The Level 1 Accept (L1A) trigger signal.
- The TTC clock (40.08 MHz).
- The Bunch Crossing Identifier (BCID) (12 bits): sampled bunch crossing when an interesting event occurs (Level 1 Accept). It is cleared by the Bunch Counter Reset (BCR) signal.
- The Trigger Type (8 bits). This value is used to identify the type of event being acquired and to apply the appropriate treatment and algorithm at the DSP level (e.g., Charge Injection, Pedestal runs, Physics runs, etc).
- The Event Identifier (EVID) (32 bits) : The 24 LSB contain the value of a counter which is incremented by the L1A signal and reset by the Event Counter Reset (ECR) signal. The 8 MSB corresponds to a counter incremented by ECR signal. The EVID uniquely identifies an event during a run.

Another important feature of the TTC FPGA is to provide the clock source to be selected by VME. This clock source is distributed to all ROD motherboard devices through dedicated Zero-Delay clock buffers. There are two possible clock sources:

- VME/LOCAL: local clock oscillator installed in the motherboard or external clock coming from the connector in LOCAL mode. It must be selected with a jumper.
- 40.08 MHz TTC clock from TTCrx (Clock40Des1). When the TTC clock disappear for any reason, the system is able to automatically turn to use the local clock oscillator, and change back when TTC clock becomes present again.

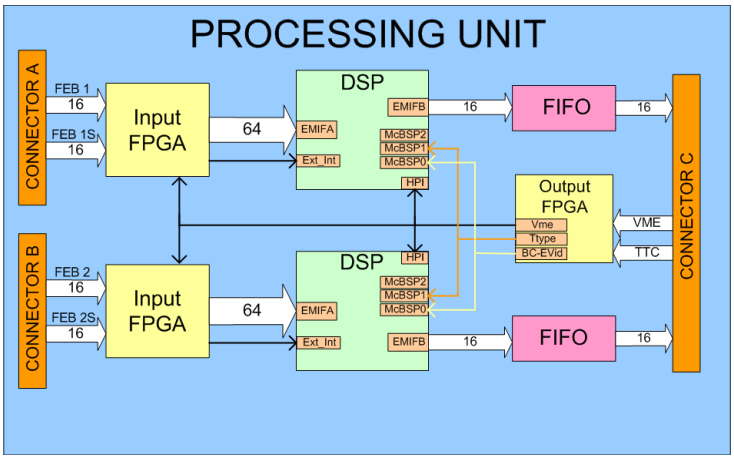

Figure 5: Processing Unit block diagram and data paths.

3.3.7. The Processing Unit

There are 4 slots for PUs per ROD, but only 2 are needed in TileCal requirements. The PU is a mezzanine board which allows flexibility for future upgrades related with exponential advances in processor capabilities versus time. The DSP PU is a mezzanine board able to handle up to 192 channels (4 superdrawers) in TileCal operation mode. The PU is equipped with two Input FPGA (InFPGA), two TMS320C6414@720MHz DSP (5760 MIPS) from Texas Instrument and two Output FIFOs. All these dual devices are used to get double processing power in a single PU and they are responsible for I/O dataflow and digital signal reconstruction. An Output FPGA (OutFPGA) for control and configuration implements the VME and TTC interfaces with the ROD motherboard as shown in Figure 5. The input superdrawer data enters into the InFPGA (from the Staging FPGA) where they are formatted and checked as needed for the DSP algorithms. When an event is ready, an interrupt is sent to the DSP which launches a DMA to read the data with the 64-bit EMIFA bus. After the DSP has finished processing an event, it writes the results in the output FIFO through the 16-bit EMIFB bus. The TTC data are received in the OutFPGA (from the TTC FPGA) and sent to each DSP via 2 serial ports. One serial port is used for the Trigger Type (McBSP1) whereas the other is used for the BCID and EventID (McBSP0). The OutFPGA allows the control of the PU board by the ROD controller through the VME layer and implements the following functionalities:

- Write DSP code for booting at initialization and read histograms through the 16-bits Host Port Interface (HPI) of the DSP.
- Full duplex communication via multi channel buffered serial port (McBSP2) with each DSP (write run number, DSP commands, status read)
- InFPGA configuration written (number of samples, number of gains, mode) and status read through a serial line.
- InFPGA code boot. The device allows dynamic online configuration without system shutdown. The main components in the PU are the DSPs. These devices are the responsible of data processing with online reconstruction algorithms for working at 100 KHz L1A trigger rate (10 μs). The DSP clock cycle is 1,38 ns and it has 8 parallel and independent Arithmetic and Logic Units (ALU).

3.3.8. The Transition Module

The Transition Module boards are placed just behind each ROD module in the rear part of the crate. Each TM can hold up to 4 S-Link Source Cards, but for TileCal requirements only 2 are needed. The ROD

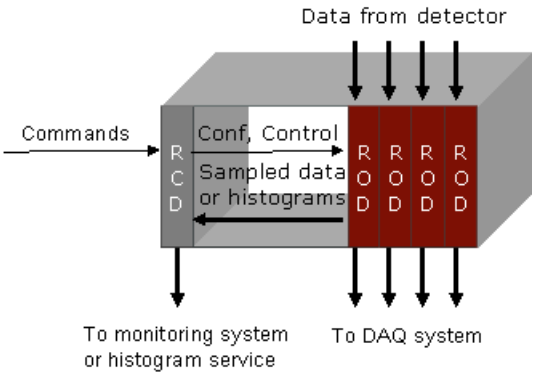

Figure 6: RCD use case.

module sends the data through the backplane P2/J2 and P3/J3 to the TM via high speed differential signals, which transmits them via optical read-out links to the ROS. Due to the limited number of pins in the P2 and custom P3 backplanes, serializers and deserializers are located in the ROD and in the TM respectively.

4. Trigger and Data Acquisition

The ATLAS Trigger and Data Acquisition (TDAQ) system is based on three levels of online trigger selection. Figure 1 shows a simplified view of the components of the system and the expected event rate at each stage. The TDAQ Supervision System is in charge of performing the initialization and shutdown of TDAQ firmware and software, distributing commands to TDAQ elements, synchronizing operations between them, and performing error handling. The building block of the Supervision is the Controller. The supervision will generally contain a number of controllers organized in a hierarchical tree.

4.1. ROD Crate DAQ

The ROD Crate DAQ (RCD) framework [9] is a component of the TDAQ developed due to the need of the sub-detectors for a common Data Acquisition (DAQ) functionality at the level of the back-end electronics. This framework serves as interface between the TileCal hardware and the DAQ system. It is based on a multithreaded read-out application core, the behaviour of which is adapted to the specific requirements through plug-ins that represent the TileCal back-end electronics. One instance of the RCD application is executed in each of the TileCal back-end crates and controlled by the Supervsion System.

The RCD has four different plug-in types. A configuration plug-in loads information from the configuration database. A trigger plug-in handles data requests which are pushed to the output plug-in from the module plug-in which can define data channels.

4.2. ROD configuration and DAQ

For TileCal requirements, the RCD is used for module control and monitoring (Figure 6), where the dataflow is not handled by the RCD itself. The TBM is controlled by a trigger object which doesn't queue data requests to the RCD core. The ROD is controlled by a module plug-in with no data channels. ROD monitoring is controlled by the ROD module via publish statistics and probe. DSP histograms are read-out through VME and published to the Online Histogramming service. Sampled information from the ROD in the form of histograms is also provided.

On configure, the ROD module loads the DSP and the InFPGA code through the VME bus. The TBM trigger configures the busy mask. On prepare for run, the ROD module loads the data format needed for the run to the InFPGAs and the DSPs. Also the OF weights, Muon Tagging thresholds and channel constants for the run are loaded.

4.3. Configuration and Conditions database

The description of the RCD configuration is stored in the configuration databases [10]. The front-end links to the ROD are described as relationships between the ROD module and the front-end modules. The output links of the ROD are described as read-out link relationships from the HOLA cards to the ROBins. The TBM contains a relationship between themselves and the RODs in order to configure the busy mask.

The OF weights needed for the DSP processing is stored in the conditions database. It also contains the bad channel list and the muon identification thresholds. All these values are retrieved from the database at prepare for run via a specific database plug-in which is loaded by the ROD module at configuration time.

5. Data reconstruction

The main operation of the ROD system is the data reconstruction at the ATLAS first level of trigger rate. In addition, the ROD system has to check the integrity of the data received from front-end and the result is packed in a special data fragment included in the bytestream for off-line checking. Furthermore, the ROD has to synchronize the front-end data with the ATLAS global TTC information, provide online monitoring and compute the muon tagging and total transverse energy algorithms for Level 2 triggers. The data processing is performed in the PU within the RODs (Figure 5). The data quality checking is carried out in the InputFPGAs whereas the data reconstruction, TTC synchronization, monitoring and algorithms for Level 2 triggers are performed in the DSPs.

5.1. DSP algortithms

The main component of TileCal RODs are the DSPs responsible for data processing. Each DSP has to process the data of two front-end modules at the ATLAS first level trigger rate. The data processing covers the synchronization of front-end data with TTC information, the energy and phase reconstruction and calibration, a Quality Factor estimation for the energy reconstruction, the Level 2 trigger algorithms and the histogramming and monitoring. In addition, the DSP has to flag known bad channels which should not be used for High Level Trigger algorithms.

5.1.1. Reconstruction algorithm: Optimal Filtering

The Optimal Filtering (OF) algorithm reconstructs the amplitude and phase of a digitized signal by a linear combination of its digital samples. Equations 1 and 2 shows the procedure to compute the energy and phase with the OF algorithm.

$$A = \sum_{i=0}^{n} a_i S_i \tag{1}$$

$$\tau = \sum_{i=0}^{n} b_i S_i \tag{2}$$

where S_i represents the digital sample i and n is the total number of samples. We define the pedestal as the baseline of the signal. The amplitude, A, is the distance from the pedestal to the peak and the phase, τ ,is defined as the time between the central sample and the peak of the pulse (Figure 7). The weights, a and b, are obtained from the pulse shape of the photomultipliers and the noise autocorrelation matrix. The process to calculate them minimizes the effect of the noise in the amplitude and time reconstruction. They are calculated to avoid pedestal subtraction in the samples.

Moreover, Optimal Filtering allows to calculate a Quality Factor (QF) defined as :

$$QF = \sum_{i=0}^{n} (S_i - (Ag_i + A\tau g'_i + p))^2 \tag{3}$$

The QF provides information about the goodness of the reconstruction. This information can be used online to decide to send raw data for single channels.

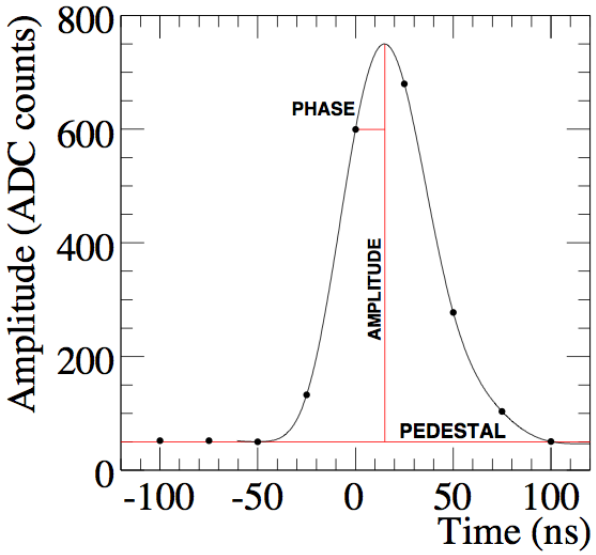

Figure 7: Optimal Filtering magnitudes

Optimal Filtering weights. The TileCal pulse shapes, their derivatives and the noise autocorrelation matrix are used to compute the Optimal Filtering weights within the ATLAS offline software. The pulse shape is different for physics, charge injection (CIS) system and laser calibration runs, differ from high to low gain and have slight differences from channel to channel. Hence, a different set of weights has to be used in the data reconstruction for each channel, run type and gain. For testbeam and commissioning, where the noise contribution is mainly due to the electronics, the Unitary matrix was chosen as the noise autocorrelation matrix. For ATLAS operation the noise autocorrelation matrix will be recomputed to take into account the effect of the pile-up in the data.

Iterative procedure. The performance of the OF algorithm is strongly dependent on a good set of the weights. These are valid within a signal phase deviation of 1 ns, and must be recalculated each time there is a change in the signal otherwise the energy reconstruction shows a parabolic deviation proportional to the phase (Figure 8). During LHC operation samples will have fixed phases given by LHC bunch crossing. However, the ATLAS commissioning has used cosmic rays which asynchronously crossed the detector. In this case, OF can still be applied and it is possible to obtain an accurate reconstruction by applying the proper weights for each event according to the position of samples in the signal. This has been implemented inside the DSP with an iterative procedure provided a set of weights computed for phases from -75 ns to +75 ns in steps of 1 ns. This procedure increases the processing time but improves considerable the reconstruction. Even though the processing time limit for the LHC is 10 μs, for the commissioning the limit on the processing time is not a constrain as the trigger frequency hardly exceeds 100 Hz.

The iterative procedure consists of a first estimation of the initial phase that ascertains the index of the maximum sample. If the maximum sample is the central sample, the rst iteration begins with OF weights calculated for 0ns whereas if the maximum sample differs from the central sample, the weights are calculated for

$$\tau_0 = 25(i_c - i_{max}) \tag{4}$$

being i_{max} and i_c the index of the maximum sample and the central sample respectively. Then, the amplitude, phase and pedestal are calculated in each iteration as:

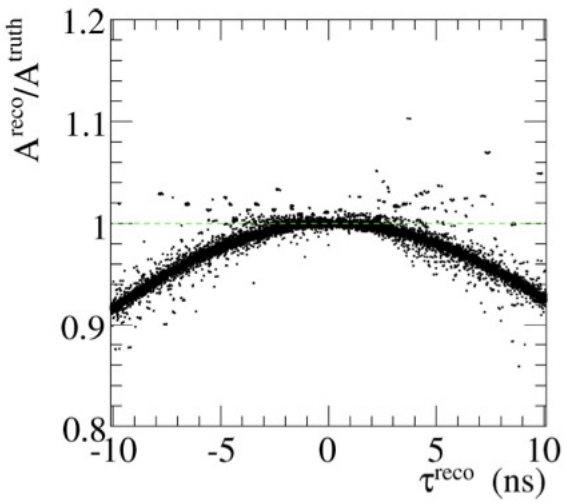

Figure 8: Energy reconstruction with optimal filtering as a function of the phase applying weights for phase 0 ns.

$$A_k = \sum_{i=0}^{n} a_i \Big|_{\tau_{k-1}} S_i \tag{5}$$

$$\tau_k = \frac{1}{A_k} \sum_{i=0}^{n} b_i \Big|_{\tau_{k-1}} S_i \tag{6}$$

where k is the iteration index starting from 1. It has been observed that the amplitude converges within three iterations for OF weights calculated in steps of 1 ns, thus n is 3.

5.1.2. Muon Tagging algorithm

The Muon Tagging algorithm implemented in the DSP uses the projective segmentation of TileCal and the energy reconstructed by the Optimal Filtering to identify and flag soft muons with P_T below 5 GeV not triggered at Level 1. The result is included in the bytestream in a Level 2 dedicated subfragment. This information can be used at level 2 to trigger muons through a fast scan on the calorimeter. The algorithm starts searching deposition of energy compatible with minimum ionizing particles in the outermost layers of TileCal (D cells). The condition required is an energy deposition between and upper and lower thresholds configurable on every start of run. If this condition is comprised the algorithm continues checking in the projective BC and A layers (Figure 9). Two different strategies are followed by the algorithm. It can be required that the energy deposited in all the three layers is compatible with minimum ionizing particles. In addition, events losing a considerable fraction of its energy in one layer are detected if the energy deposited in one layer exceeds the higher threshold.

5.1.3. Total transverse energy computation

Since the DSP computes the energy per channel with the OF algorithm, it is possible to use this result in order to compute the total transverse energy in the module. Furthermore, since the DSP knows the position of the module which is read out, it is also possible to compute the X and Y projections of the total transverse energy. This information is used at the second level trigger to search for missing transverse energy over the whole detector. The algorithm implemented in the DSP to compute the total transverse energy and its X and Y projections. The energy per tower is computed with the energy per channel obtained with the OF algorithm and the corresponding gain per channel. If both the Muon Tagging and the Total transverse energy computation algorithms are enabled, the energy per cell computed in the Muon Tagging function is

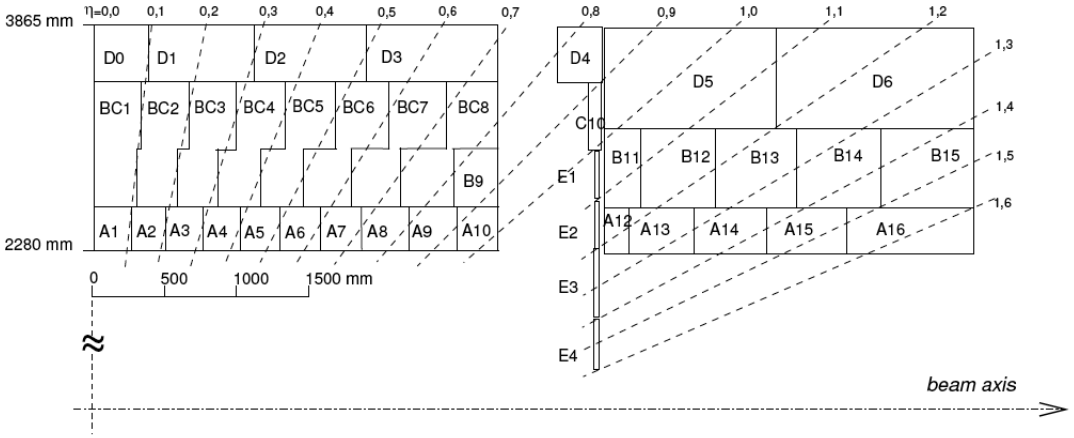

Figure 9: TileCal cells and projective towers.

used by the Total transverse energy algorithm to obtain the energy per tower. The transverse energy per tower is then obtained by applying trigonometric factors. The total transverse energy of the module is the sum of all the towers. Finally, X and Y projections are calculated. In order to make the algorithm run faster, all the relevant trigonometric factors are stored in a look-up-table.

5.1.4. Monitoring at ROD level

The Online monitoring at ROS level (GNAM) samples data at Level 2 trigger at a low rate (Figure 10). Thus not all the events can be monitored by GNAM. In addition, the ROD replaces the raw data received from front-end by reconstructed magnitudes. Hence, GNAM monitors only reconstructed data. The aim of the ROD monitoring is to take advantage of the availability of the raw and reconstructed data at the first level of trigger rate. The ROD monitoring provides different type of information presented through different interfaces.

- ROD Histogramming. The ROD RCD module builds relevant histograms about the performance of the read-out based on the motherboard registers. Relevant histograms are the number of events received and discarded per super-drawer. The histograms are published to the Online Histogramming Service (OHS).
- DSP Histogramming. The DSP builds histograms which are stored in its internal memory. It can be configured to build histograms for the first sample of every event and for the Quality Factor. Histrograms are built separately for every channel. The first sample histogram is used to identify online the channels with high pile-up and/or noisy channels. The monitoring of the QF allows the identification of problematic channels in terms of reconstruction. These histograms are read-out from the DSP through the VME bus and published to the OHS by the ROD RCD module.
- Raw data sampling. It is possible to sample raw data events from the input stage of the ROD. These events are presented in the Event Dump panel under user request. The raw data sent by the front-end electronics is presented and it can be used to detect digital errors.
- ROD Information for Tile Monitoring (RITMO). Provides in-situ information about data synchronization and busy status inside the DSP. This information is published to the OHS.

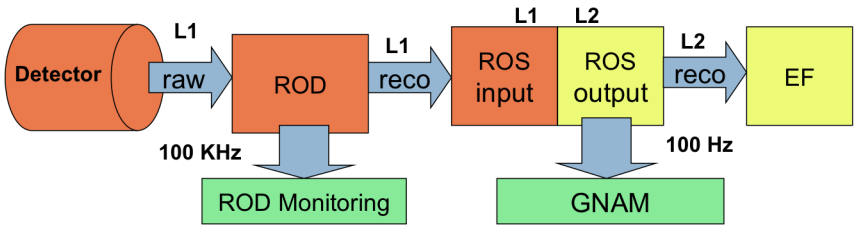

Figure 10: TileCal monitoring levels.

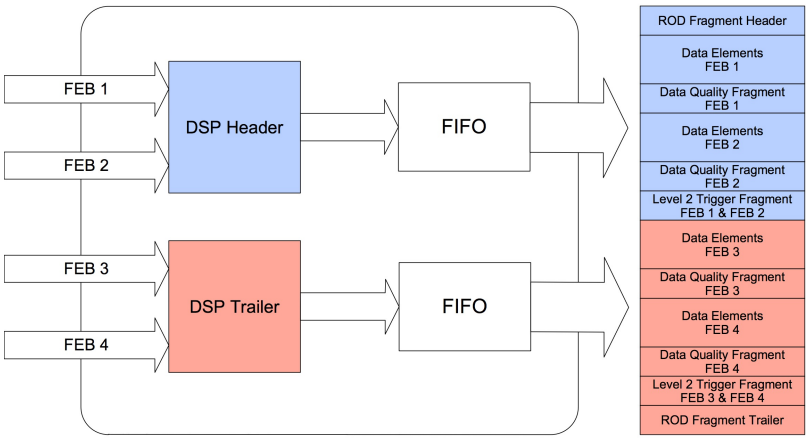

Figure 11: ROD data fragment elements.

5.2. ROD Data format

The ROD can be configured to provide different output data fragments depending on the run type and the data required. The data received in a PU is processed and transmitted to the Output Controller FPGA. Then, for each event the data is packed in a ROD fragment and transmitted to the next level of trigger (Figure 11) . Each ROD fragment contains three main parts:

- Header: the header of the rod fragment contains general fragment information and flags and it is included in the bytestream by the DSP configured as header.
- ROD sub-fragments or data elements: depending on the run type and the data required the ROD can be configured to provide different data elements within the sub-fragments. Each sub-fragment is composed by a header and data elements. The header contains information about the data elements. The data elements contain either the reconstructed magnitudes from the Optimal Filtering algorithm and/or the raw data received from front-end. Besides, additional sub-fragments can be required to ROD such as Muon tagging and/or total transverse energy calculation. Finally, the data quality sub-fragment is always included for each module.
  - Reconstruction sub-fragment: This data element contains the OF reconstructed magnitudes for each channel. There are different OF algorithms implemented inside the DSP but the data

provided is the same in all cases. For each channel the reconstruction sub-frament contains the Energy, Phase and a Quality Factor.

- Raw data sub-fragment: The raw data sub-fragment contains the digital samples as received from front-end. This sub-fragment is required in calibration runs for off-line data analysis. In addition, during the ATLAS commissioning it has been used the raw data together with the reconstruction sub-fragment to calibrate and validate the detector performance. It was possible due to a low event rate during this phase whereas at the ATLAS nominal first level of trigger the output data bandwidth of ROD allows only to send reconstructed data.
- Level 2 Trigger sub-fragment: additionally to data sub-fragment the ROD can be configured to execute a Muon Tagging algorithm and total transverse energy computation per module and include the results in an additional sub-fragment. The data included in this sub-fragment is used in a Level 2 trigger algorithm to identify low transverse energy muons and to implement Missing Et trigger algorithms. The Level 2 trigger sub-fragment includes the information for two consecutive TileCal modules. Hence, only one sub-fragment per DSP is provided.
- Data quality sub-fragment: this sub-fragment is always included in the ROD fragment for each TileCal module and it contains information about digital error checking results performed inside the InFPGA.

- Trailer: the trailer of the ROD fragment is included by the OC and contains the number of data elements and control words for data transmission to the ROS.

References

[1] ATLAS Collaboration, *Expected performance of the ATLAS experiment-detector, trigger and physics.* CERN-OPEN-2008-020, 2008.

[2] ATLAS Collaboration, *ATLAS Tile Calorimeter Technical Design Report.* CERN, LHCC/96-42, 1996.

[3] K.J. Anderson, et al., Nucl. Instr. and Meth. A 551 (2005) 469.

[4] K. Anderson et al. , *ATLAS Tile Calorimeter Interface Card.*, proceedings of the 8th Workshop on Electronics for LHC Experiments, ISBN 92-9083-202-9.

[5] S. Ask et al., *The ATLAS Central Level-1 Trigger Logic and TTC System.*, J. Instrum. 3 (2008) P08002.

[6] Pierre Matricon et al., *TBM (and TTCM): TheTrigger and Busy Module for the ATLAS LARG ROD system*, CERN EDMS Document https://edms.cern.ch/document/653609/(2005)..

[7] E. Fullana et al. *Digital Signal Reconstruction in the ATLAS Hadronic Tile Calorimeter.*, IEEE Trans. Sci, vol.53, no.4, pp.2139-2143, 2006.

[8] B. Salvachua et al. , *Algorithms in the ROD DSP of the ATLAS Hadronic Tile Calorimeter.* Journal of Instrumentation, 2 (02): T02001, 2007.

[9] S. Gameiro, G. Crone et al. , *The ROD crate DAQ software framework of the ATLAS data acquisition system.* IEEE Trans. Nucl. Sci. 53 (2006) 907-911.

[10] I. Soloviev et al. , *The ATLAS DAQ System Online Configurations Database Service Challenge.* J. Phys.: Conf. Ser. 119 (2008) 022004.