

Status and Plans for Xilinx Development

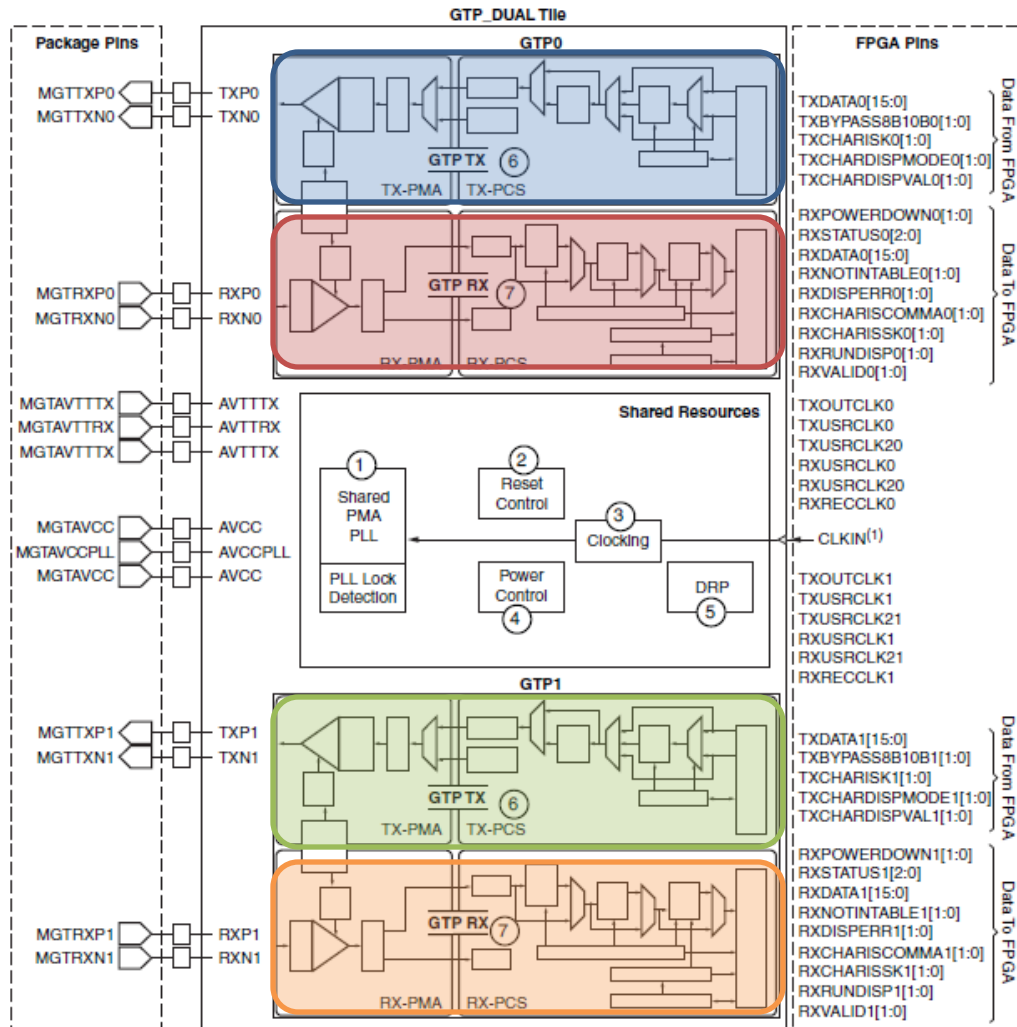
Pablo Moreno (IFIC, Valencia)

Overview

- Design using GTP Transceivers
 - GTP Dual Tile
 - GTP Transmitter
 - GTP Receiver
 - Loopback Modes
 - RocketIO Implementation and Simulation

Design using GTP Transceivers

GTP Dual Tile



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- GTP Dual Tile

- 2 Transceivers

- TX0

- RX0

- TX1

- RX1

- Shared Resources

- Oscillator

- Reset control

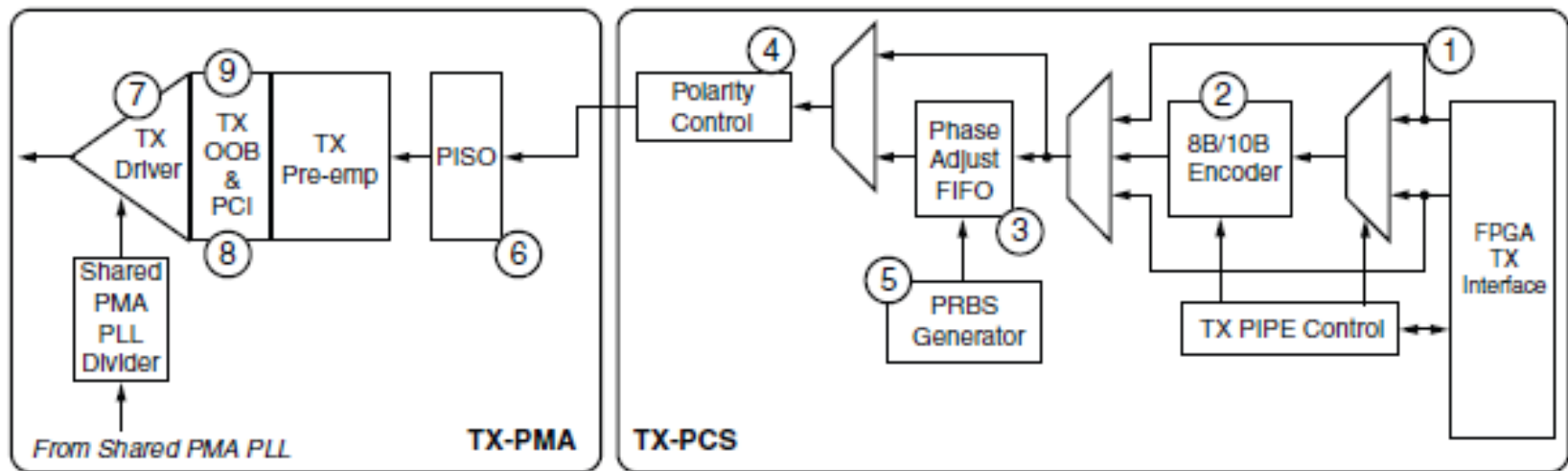
- Power control

- Clocking

- DRP

Design using GTP Transceivers

GTP Transmitter (TX)



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- Physical Coding Sub-layer (PCS), which is the logical sub-layer of the PHY
 - FPGA TX interface
 - 8B/10B encoder
 - TX Buffer and Phase Alignment
 - Polarity Control
 - PRBS Generator
- Physical Media Attachment (PMA), electrical sub-layer of the PHY
 - Parallel In to Serial Out
 - TX Driver

Design using GTP Transceivers

GTP Transmitter (TX) - PCS

- FPGA TX Interface
 - Parallel data input of the transceiver
 - Width of the data port: 1 or 2 bytes
 - Width of the internal datapath:
 - 8 or 10 bits for 1 byte mode
 - 16 or 20 bits for 2 bytes mode
- 8B/10B Encoder
 - Industry standard encoding scheme that trades 2 bits overhead per transmitted byte
 - DC Balance
 - Error Detection
 - Limited Run Lengths
 - Control Characters (K)
 - Block may be bypassed if not needed for reduced latency

Design using GTP Transceivers

GTP Transmitter (TX) - PCS

- TX Buffer, Phase Aligner
 - 2 clock domains inside PCS
 - PMA Parallel Clock
 - PCS Parallel Clock
 - Phase differences between domains must be resolved using one of these methods
 - TX Buffer: Easy to use, robust, poor latency, required when oversampling
 - TX Phase Aligner: complex, fewer latency, required to reduce lane skew when multiple channels operating

Design using GTP Transceivers

GTP Transmitter (TX) - PCS

- Polarity Control
 - Permits polarity of outgoing data to be inverted before serialization and transmission. Avoid HW fixes for swapped TXP/TXN traces on a board
- PRBS Generator
 - 3 different Pseudo Random Bit Sequences are generated here in order to test the signal integrity of high speed links

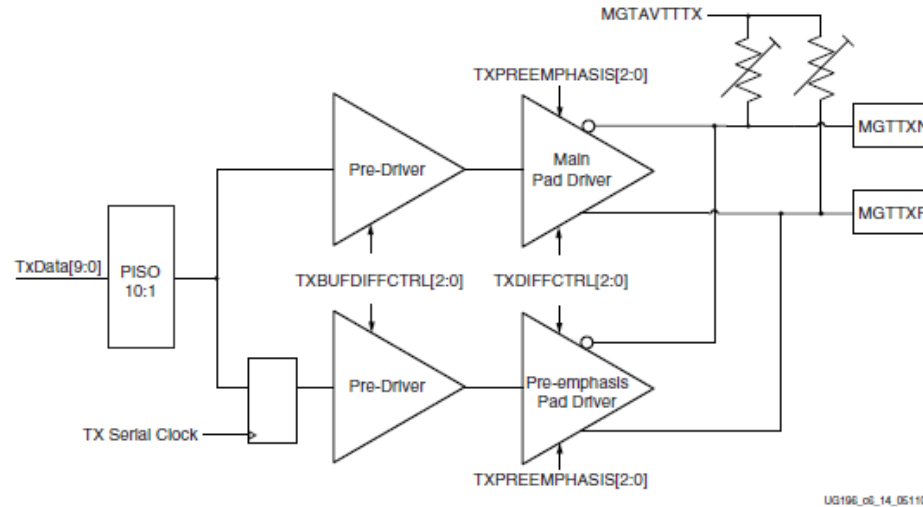
Design using GTP Transceivers

GTP Transmitter (TX) - PMA

- Parallel In to Serial Out
 - Core of the GTP TX data path. Serializes 8 or 10 bits per parallel clock cycle.
 - Line rate depends on
 - PLL clock rate
 - Oversampling mode
 - Clock dividers used

Design using GTP Transceivers

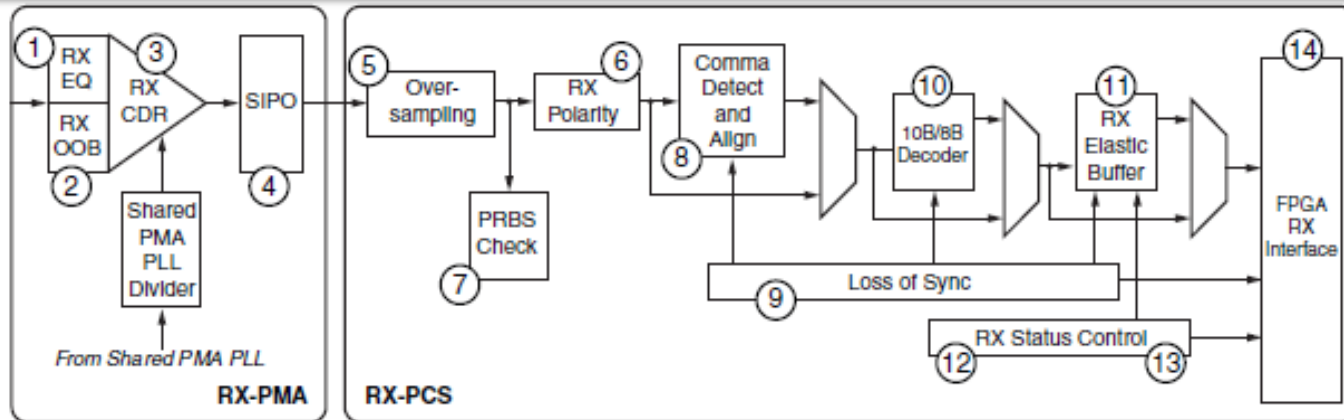
GTP Transmitter (TX) - PMA



- Configurable TX Driver
 - High Speed Current Mode Differential Buffer
 - Differential voltage control
 - Pre-emphasis for equalization of HF loss of high speed traces
 - Configurable termination impedance

Design using GTP Transceivers

GTP Receiver (RX)



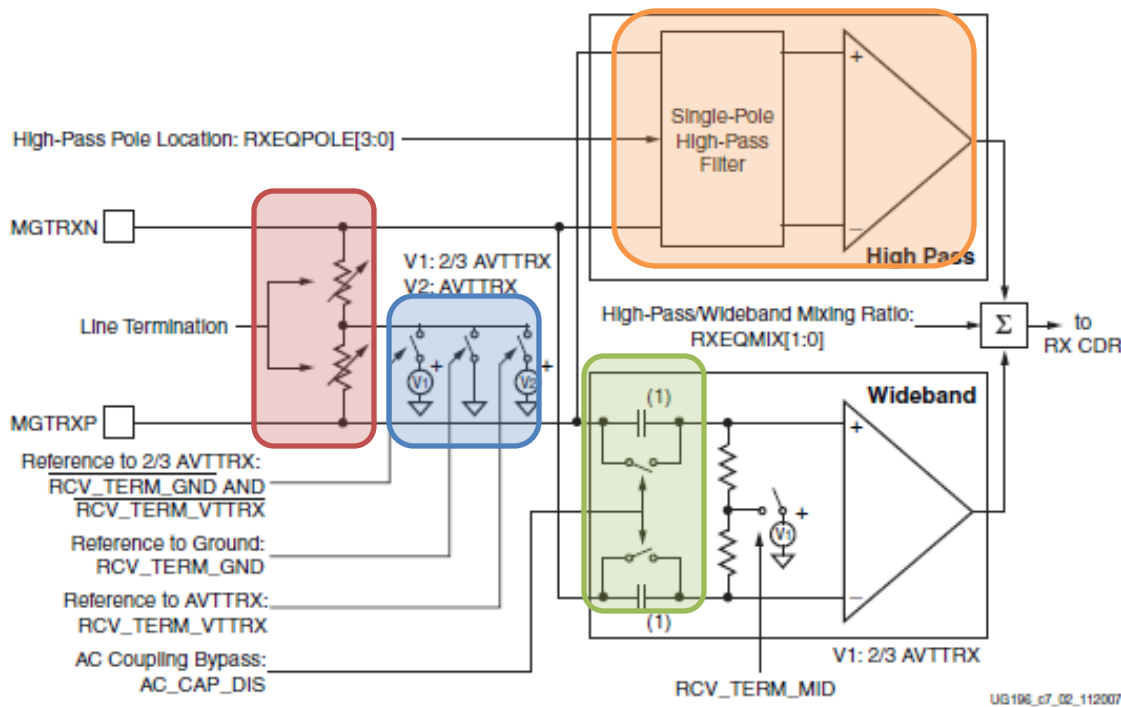
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- Physical Media Attachment (PMA), electrical sub-layer of the PHY
 - Termination and Equalization
 - Clock Data Recovery (CDR)
 - Serial in to Parallel Out
- Physical Coding Sub-layer (PCS), logical sub-layer of the PHY
 - Oversampling
 - RX Polarity Control
 - PRBS Detection
 - Comma Alignment and Detection
 - Loss of Sync State Machine
 - 8B/10B Decoder
 - Elastic Buffer and Phase Aligner
 - CLK correction
 - FPGA RX Interface

Design using GTP Transceivers

GTP Receiver (RX) – PMA

- RX Termination and Equalization



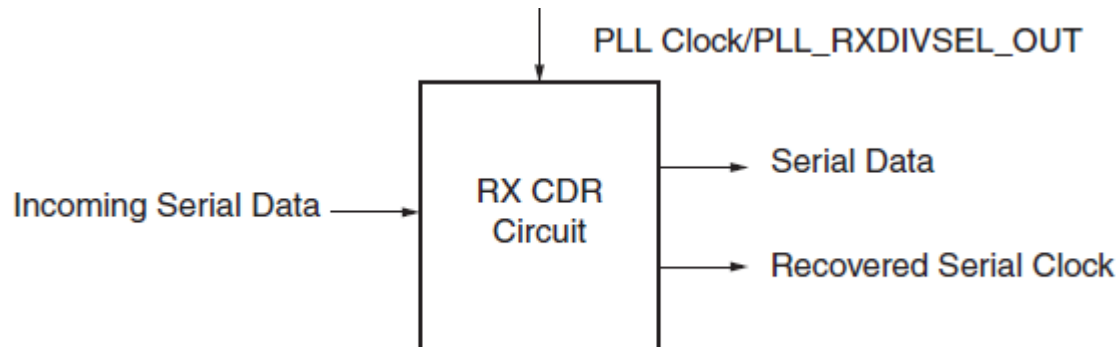
- Current Mode Logic (CML)Receiver
 - Determines the value of the differential input signal
 - Termination Voltage
 - Termination Impedance
- Equalizer
 - AC Coupling
 - Optional Configurable Linear Equalizer for HF loss in high speed traces

Design using GTP Transceivers

GTP Receiver (RX) - PMA

- Clock Data Recovery

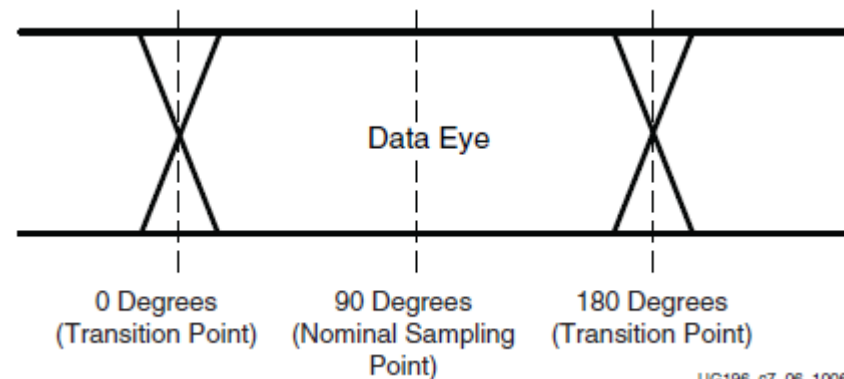
- CDR allows to extract a recovered clock signal from received data (embedded clock)
- Result: clock that matches clock originally used to generate serial stream of data
- Conditions
 - Line rate of recovered clock matches RX line rate within 1000 ppm
 - Sufficient transitions in data



Design using GTP Transceivers

GTP Receiver (RX) - PMA

- Horizontal sample point shift
 - Transition points used to recover frequency of incoming clock
 - Transition points used to find the optimal time to sample data.
 - Configurable data sampling point relative to the first transition



Design using GTP Transceivers

GTP Receiver (RX) - PMA

- Serial In to Parallel Out (SIPO)
 - Heart of RX datapath. Takes the incoming serial sequence and delivers deserialized data words to the PCS
 - Clocks that take part (recovered from CDR)
 - Serial clock (line rate)
 - Parallel clock (one cycle per n-bit word)

Design using GTP Transceivers

GTP Receiver (RX) - PCS

- Oversampling
 - 5x oversampling enables serial rates from 100 Mb/s to 500 Mb/s (CDR must operate 5x the desired rate to stay in regular operation limits)
 - 2 bits of recovered data from 10 received bits
 - Oversampling block enabled in both sides of the channel (TX and RX)

Design using GTP Transceivers

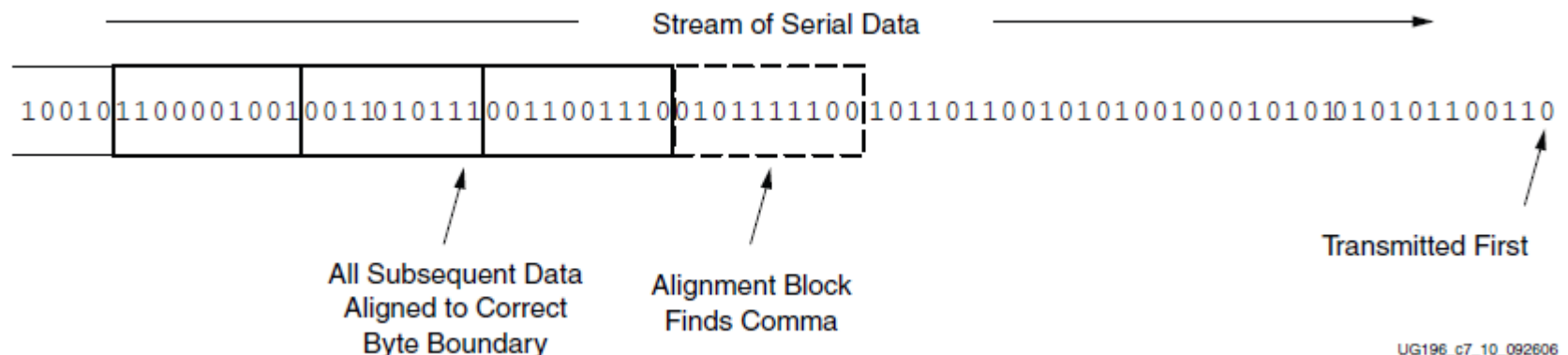
GTP Receiver (RX) - PCS

- RX Polarity Control
 - GTP RX is able to invert incoming data polarity using this block if differential traces are swapped by error.
- PRBS Detection
 - GTP RX includes a built-in Pseudo Random Bit Sequence checker, used for testing the signal integrity of the channel.
 - A register stores the number of received errors, and a flag signal alerts when a certain configurable trigger is exceeded in a counter.

Design using GTP Transceivers

GTP Receiver (RX) - PCS

- Comma Alignment and Detection
 - Serial data must be aligned to symbol boundaries before it can be used as parallel data... Where does a byte starting and ending in a stream of data?
 - TX send a special character (comma)
 - RX searches the pattern of a comma till it is founded. Then received bits are packed from comma boundary



Design using GTP Transceivers

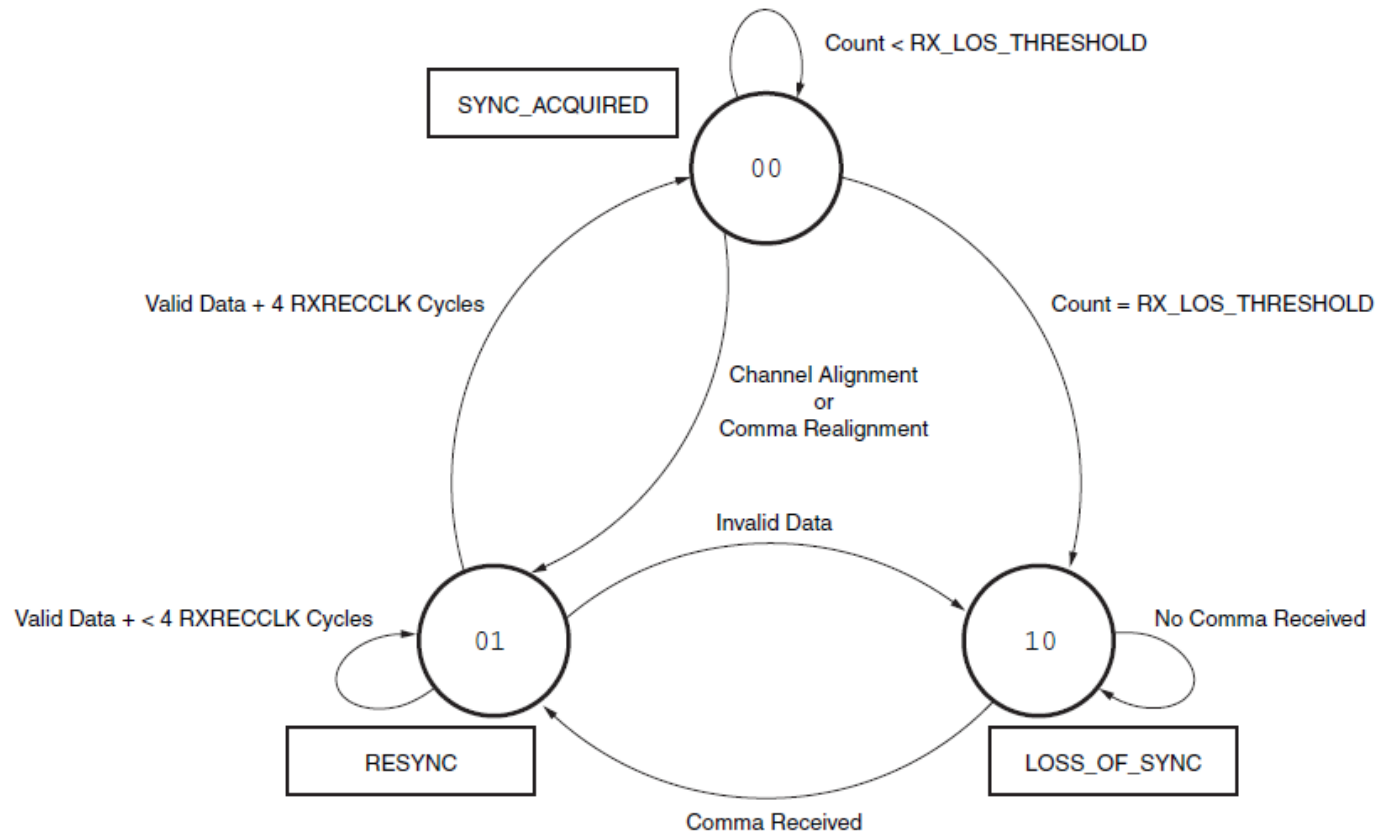
GTP Receiver (RX) - PCS

- Configurable Loss-of-Sync State Machine
 - Some 8B/10B protocols make use of a state machine in order to detect malfunction of the channel
 - GTP RX has this LOS block implemented
 - When not used, its ports can be re-used to monitor incoming data.

Design using GTP Transceivers

GTP Receiver (RX) - PCS

- Configurable Loss-of-Sync State Machine



Design using GTP Transceivers

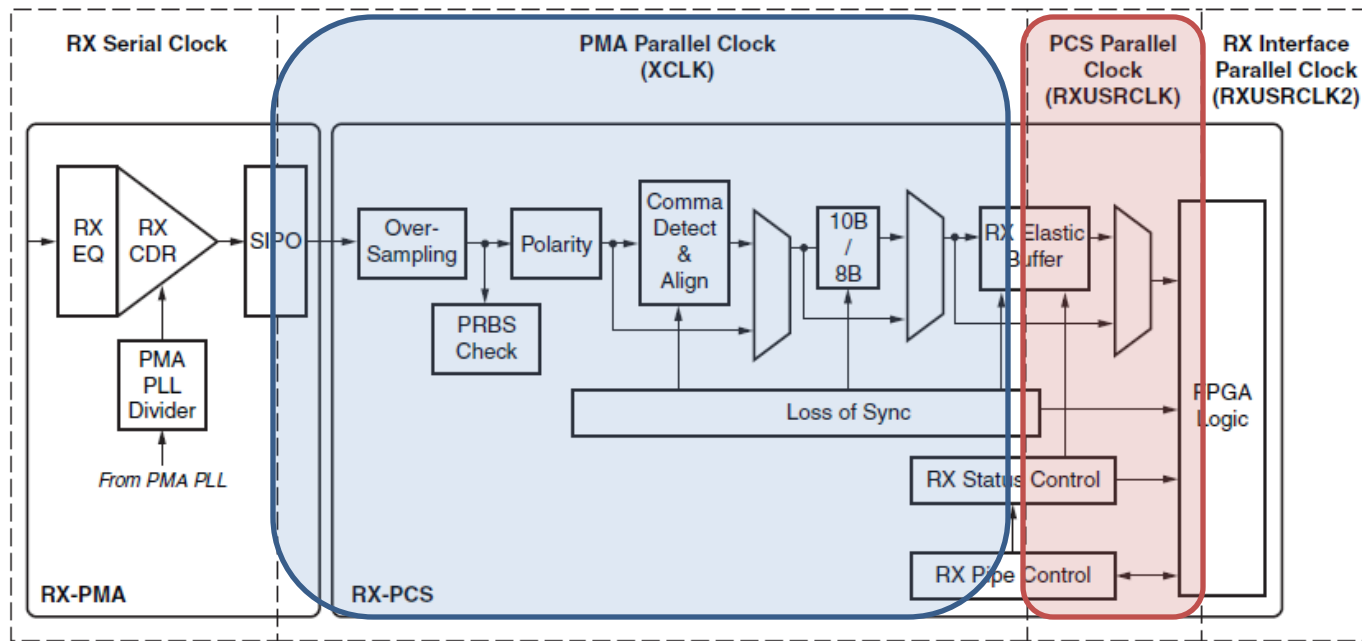
GTP Receiver (RX) - PCS

- Configurable 8B/10B Decoder
 - 8 bit data and control values (K characters) mapped into 10 bit sequences
 - When activated, internal datapath is always 10 bits
 - Running Disparity (1/0 balance) can be observed in a port
 - Error signals notify when disparity or “non in table” errors are produced

Design using GTP Transceivers

GTP Receiver (RX) - PCS

- Configurable Elastic Buffer and Phase Aligner
 - GTP RX has two parallel clock domains



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- Elastic buffer resolves phase differences between the two domains

Design using GTP Transceivers

GTP Receiver (RX) - PCS

- Configurable Elastic Buffer and Phase Aligner
 - Possibilities
 - Elastic Buffer: Works immediately , 8/10 bits internal datapath, permits clock correction
 - Phase Aligner: Needs some clock cycles to stabilize, fewer latency, only 10 bits internal datapath
- Configurable Clock Correction
 - Allows to correct frequency differences between clock domains
 - Performance
 - Replicates idle characters when elastic buffer gets empty
 - Eliminates idle characters when elastic buffer gets full
 - Special clock correction received sequence is needed to proceed

Design using GTP Transceivers

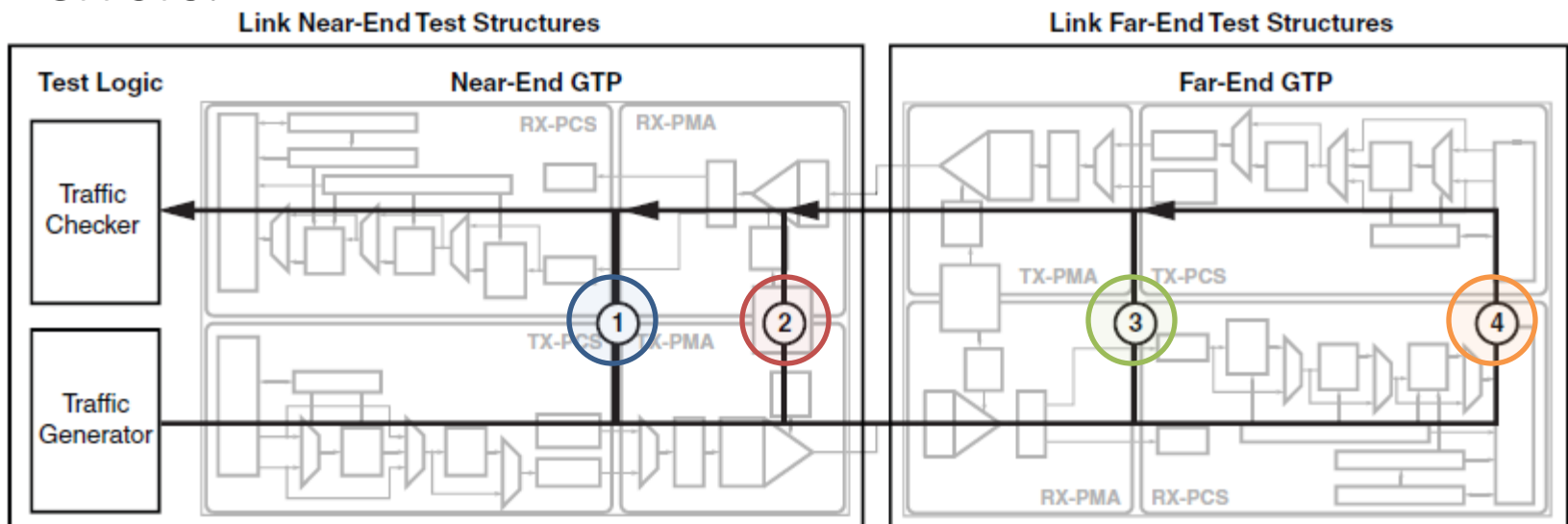
GTP Receiver (RX) - PCS

- FPGA RX Interface
 - The FPGA logic can access to incoming data on the positive edge of the parallel clock using this interface.
 - Received data can be 8/10/16/20 bits long

Design using GTP Transceivers

GTP Loopback Modes

- Specialized configurations of the datapath where the traffic patterns (PRBS) are transmitted and folded back to the source to be compared and check transmission errors.



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Near-end loopback

1. PCS loopback
2. PMA loopback

Far-end loopback

3. PMA loopback
4. PCS loopback

Design using GTP Transceivers

RocketIO Implementation and Simulation

- GTP transceivers IP core has been implemented and configured to XAUI protocol using Xilinx RocketIO GTP Wizard core

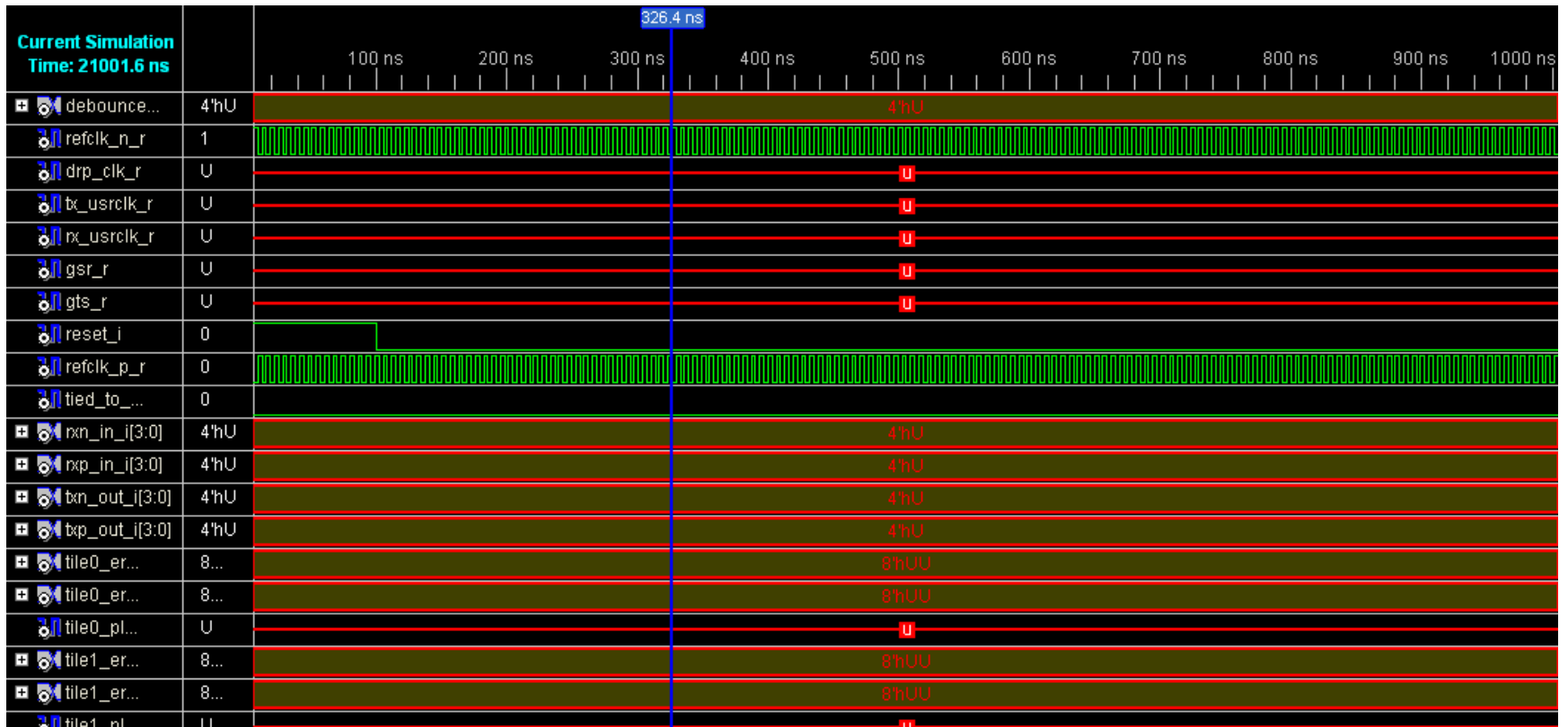
General Settings	
Component Name:	rocketio_wrapper
Configured GTP_DUALS:	2 out of 6
Reference Clock:	156.25 MHz
PLL Clock:	1.5625 GHz

Transmitter Settings	
PCS/PMA Phase Alignment:	Selected
GTP0	
Data Width / Clk Div / Line Rate:	16 / 1 / 3.125
Encoding:	8B/10B
PRBS:	Not enabled
GTP1	
Data Width / Clk Div / Line Rate:	16 / 1 / 3.125
Encoding:	8B/10B
PRBS:	Not enabled

Receiver Settings	
GTP0	
Data Width / Clk Div / Line Rate:	16 / 1 / 3.125
Decoding:	8B/10B
PCS/PMA Phase Alignment:	Not selected
OOB:	Not selected
PRBS:	Not selected
Comma Detect:	Selected
Channel Bonding:	Selected
Clock Correction:	Selected
PCI Express Mode:	Not selected
GTP1	
Data Width / Clk Div / Line Rate:	16 / 1 / 3.125
Decoding:	8B/10B
PCS/PMA Phase Alignment:	Not selected
OOB:	Not selected
PRBS:	Not selected
Comma Detect:	Selected
Channel Bonding:	Selected
Clock Correction:	Selected
PCI Express Mode:	Not selected

Design using GTP Transceivers

RocketIO Implementation and Simulation



Design using GTP Transceivers

RocketIO Implementation and Simulation

