Readout electronics for the silicon micro-strip detector of the ILD concept

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Abstract

Si-strips are the baseline for the Forward Tracker Detector (FTD) of the International Linear Detector (ILD). The main element of the front-end electronics is a multi-channel ASIC for self-triggered detection and processing of low level charge signals. The architecture used in this chip is very similar to the typical structure of a Si-strip readout system presented in previous works. Nevertheless, some design modifications have been included to reduce the Equivalent Noise Charge (ENC).

Keywords: ILD, readout ASIC, ENC, noise

1. Introduction

In particle physics, detectors that can measure the position of particles with high precision are needed. The silicon sensor proposed by the International Linear Detector (ILD) for the tracker region of future linear colliders is based on a micro-strip silicon detector with 128 strips per module (50 µm pitch and 300 µm wide) [1]. The main characteristic of these strips in comparison with other systems is that long strips can be thinned down to 50 µm to obtain a reduced material budget. In addition, noise has to be maintained below 400 electrons for the sensor and its readout electronics.

Typically, the current generated by each channel is read and processed in a dedicated ASIC, which has the necessary signal conditioning, processing and digitalizing circuitry. The processed data is then sent to dedicated computer systems for analysis.

The difficulty associated with these sensors is that there is a huge amount of channels to be read: for example, in the ATLAS experiment at the Large Hadron Collider (LHC), a total of 6.2 million of channels have to be read.

The purpose of this paper is to present the readout electronics for the silicon strip detector of the ILD concept. We will start with the behavioural model of the entire channel and we will finish with the design of the front-end circuits at schematic level.

2. Readout ASIC

The architecture used in this chip is very similar to the typical structure of a silicon strip readout system presented in previous works [2-5].

The input stage of the readout ASIC consists of a Charge Sensitive Amplifier (CSA), also known as preamplifier. This circuit has to be designed taking into account that it determines the dominant contribution of noise. Functionally, the preamplifier can be seen as an integrator.

The preamplifier output goes to a differentiating/integrating amplifier, the shaper. Typical shapers are CR-RC stages of order 1, which

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means that the shaper is a high-pass filter of order 1 followed by a low-pass filter of order 1. Functionally, this stage converts the amplified sensor pulse into a CR-RC shaped pulse with a characteristic shaping time τ. The characteristic shape and time of the shaper has an impact on the noise performance of the detector system.

To detect the existence of a particle hitting the detector, a sparsifier is used. This is basically a trigger decision stage adding several adjacent channels. This minimizes the possibility of a false trigger due to noise when the particle energy is low.

In advanced detectors, the ASIC includes A/D conversion of the shaped pulse, which is sampled in several points. When a hit is detected in the sparsifier, it is possible to reconstruct the pulse shape and calculate the energy of the particle. The sampling of the pulse can be done with an analogue pipeline. The digitalization is done at low speed, usually with a Wilkinson Analogue to Digital Converter (ADC). Figure 1 shows the schematic of one channel of the readout ASIC.

During the design of the readout ASIC, special considerations have to be taken given that the chip resides inside the detector. It must be designed to meet two conflicting requirements: low power and low noise. A low power readout ASIC is required to avoid cooling systems inside the detector area. If the ASIC is not designed to produce the imposed low power dissipation, the generated heat will become unmanageable. A low noise readout ASIC is required to detect particles with low energy and avoid false detections. To achieve these goals, the semiconductor technology to be used must be selected carefully. Deep and ultra-deep submicron CMOS have been the technology of choice for low power applications in the last decade, at least in the digital field of electronics. These technologies also assure the necessary radiation hardness, which is not critical in ILD. In this particular case, the chosen technology is 65 nm from TSMC. Moreover, all modules have to be designed with power-off capabilities and pulsed power mode of operation to match the ILD structure of operation.

3. Design of the readout ASIC

One entire channel of the readout ASIC has been modelled with Verilog-AMS to define the key parameter of the pre-amplifier, the shaper and the sparsifier. Nevertheless, up to now only the pre-amplifier and the shaper have been designed at the schematic level.

3.1. Pre-amplifier design

The pre-amplifier is a CSA designed using a folded cascode amplifier with gain boosting. Figure 2 shows a schematic diagram of the CSA. This stage has been designed to detect from 1 Minimum Ionizing Particle (MIP) to 100 MIPs (1 MIP is equal to 24000 electrons). Schematic simulations report that the pre-amplifier has a gain of 69 dB and a 3 dB-BW of 55 kHz. The power consumption is below 380 µW, provided that the power supply is 1.2 V.

The CSA presents the main noise contribution of the entire channel. The ENC of the channel can be modelled as:

$$ENC = a + b\, C_d,$$

where C_d is the capacitor of the detector. The sizes of the transistors and the bias current have been selected to maintain the noise below 500 electrons.

3.2. Shaper design

The shaper circuit is based on an amplifier with a capacitor in series with a resistor at the input and a resistor in parallel with a capacitor at the feedback. The designed amplifier is also a folded cascode with a gain of 60 dB, 3 dB-BW of 90 kHz and a power consumption of 120 µW.

Care must be taken during the design of the feedback resistor because it can increase the area of each shaper (when using poly-silicon resistors) or the thermal noise (when using active resistors). For this reason, in this work we have designed the feedback resistor using the resistor demagnification technique, which basically consists in using a current mirror to demagnify the current flowing in a resistor R with the purpose to let it behave as a resistor of higher value with respect to its nominal value [6]. The schematic of demagnified resistor is presented in figure 3.

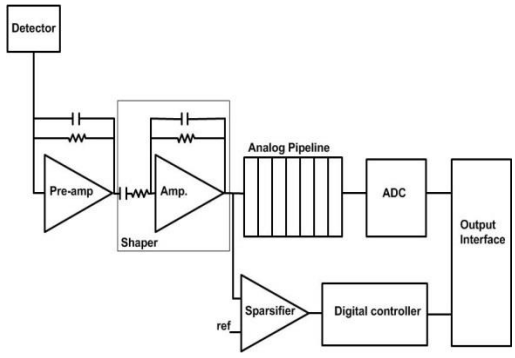

Fig. 1. Schematic of one channel of the readout ASIC.

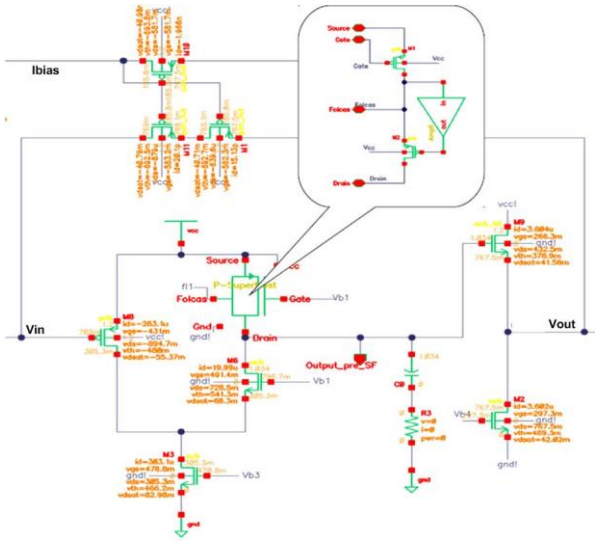

Fig. 2. Schematic diagram of the Current Sense Amplifier.

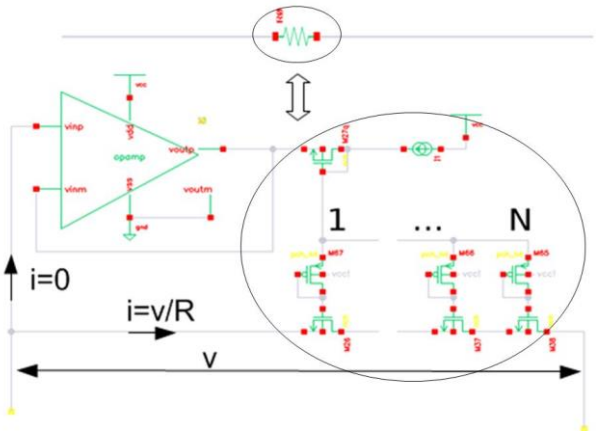

Fig. 3. Schematic of the demagnified resistor used in the shaper circuit.

4. Results

The test-bench of the pre-amplifier and shaper schematics with the behavioural model of the remainder of the channel has revealed that these circuits increase the noise of the channel due to non-ideal current biasing. This issue can be solved by introducing a filter in the reference current or scaling down the current reference (which implies more power consumption).

Once the noise induced by non-ideal sources has been reduced, parameter "a" in the ENC equation is equal to 148 electrons and parameter "b" is equal to 6.7 electrons/pF. This result is compared to other similar readout ASICs in Table 1.

Table 1
ENC comparison to previous works

Readout ASIC	a(e-)	b(e-/pF)	Shaping time
APV25 [3]	246	36	50 ns
Beetle chip [4]	303	33.6	25 ns
KPix[5]	300	35	-
This design	148	6.3	2 us

5. Conclusions

The specifications demanded by ILD and future linear colliders increase the complexity of readout ASICs for Si-strip sensors. In this paper, signal conditioning circuits (pre-amplifier and shaper) have been presented at a schematic level.

The behavioural model of the readout ASIC has allowed to simulate the designed circuits. The results revealed that the presented designs solve the issues related to the use of non-ideal sources and that they meet the low power and low noise specifications.

Acknowledgments

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