Upgrade of the ATLAS Tile Calorimeter Electronics

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Abstract

The Tile Calorimeter (TileCal) is the hadronic calorimeter covering the central region of the ATLAS experiment at LHC. The TileCal readout consists of 9852 channels. The bulk of its upgrade will occur for the High Luminosity LHC phase (Phase II) where the peak luminosity will increase 5× compared to the design luminosity (10^{34} cm^{-2}s^{-1}) at center of mass energy of 14 TeV. The TileCal upgrade aims at replacing the majority of the on- and off-detector electronics to the extent that all calorimeter signals will be digitized and sent to the off-detector electronics in the counting room. To achieve the required reliability, redundancy has been introduced at different levels. Three different options are presently being investigated for the front-end electronic upgrade. Extensive test beam studies will determine which option will be selected. 10.24 Gbps optical links are used to read out all digitized data to the counting room while 4.8 Gbps down-links are used for synchronization, configuration and detector control. For the off-detector electronics a pre-processor (sROD) is being developed, which takes care of the initial trigger processing while temporarily storing the main data flow in pipeline and de-randomizer memories. Field Programmable Gate Arrays are extensively used for the logic functions off- and on-detector. One demonstrator prototype module with the new calorimeter module electronics, but still compatible with the present system, is planned to be inserted in ATLAS at the end of 2015.

Keywords: DAQ, Readout Electronics, ATLAS

1. Introduction

TileCal is the central hadronic calorimeter of the AT-LAS experiment [1] at LHC. It uses steel as absorber medium and plastic scintillating tiles as active material. Charged particles produce light in their interactions with the scintillating tiles. The light is converted to electrical pulses in the corresponding PMTs. These pulses are then digitized and stored in pipeline memories. Upon the reception of a Level 1 trigger acceptance signal the digital samples are transmitted to the back-end electronics for further processing.

In the LHC Phase II (after 2024) the peak luminosity will be increased by a factor of 5 compared to the design luminosity (10^{34} cm^{-2}s^{-1}) [2]. The TileCal Phase II upgrade aims to transfer all digitized data to the back-end before the first level of trigger (Figure 1). This requires an extreme increase of the bandwidth between front and back-end electronics (from 165 Gbps to 80 Tbps). It is foreseen to have full redundancy in the readout channels from PMTs to the back-end to increase the reliability and robustness of the system. Redundancy has also been introduced in the low voltage power supplies. The new front-end electronics needs to be more radiation tolerant due to the luminosity increase.
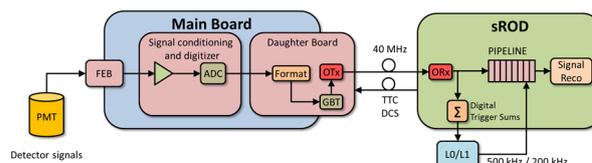

Figure 1: TileCal future architecture.

In order to evaluate and qualify the new electronics for the Phase II upgrade, a demonstrator prototype is being developed. It will be equipped with the new front-end and back-end electronics, but will maintain compatibility with the present analog trigger system. A hybrid slice of the calorimeter is planned to be inserted in AT-LAS during 2015.

2. TileCal Upgrade Demonstrator

2.1. Front-end Boards

Three options are being evaluated for the front-end boards. The 3-in-1 cards are based on the design used in the current system using discrete components (Figure 2). These boards receive and shape the PMT signals, with two different gains (ratio 1:32) and provide calibration capabilities and control [3]. The Charge Integrator and Encoder (QIE) option is an Application Specific Integrated Circuit (ASIC) with a charge integrator based on a current splitter with multiple ranges and a gated integrator plus on-board flash ADCs. It works at 40 MHz with a 17 bit dynamic range compressed to only 10 bits. The FATALIC option uses an ASIC with a current conveyor with a shaping stage with 3 different gains and the TACTIC 12-bit pipelined 40 MHz ADC.
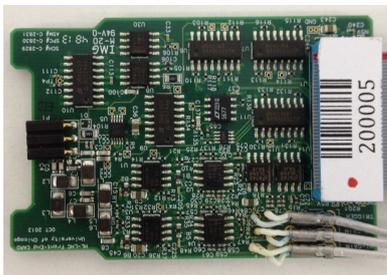

Figure 2: Picture of a 3-in-1 card.

2.2. Main Board

This board is the data and control interface for the modified 3-in-1 cards option (Figure 3). It is in charge of the digitization of the high and low gain signals from 12 PMTs at a rate of 40 MHz using dual channel ADCs serially read-out with 560 Mbps Low Voltage Differential Signal (LVDS). The MainBoard is also responsible for the front-end board control using Altera Cyclone IV Field Programmable Gate Arrays (FPGAs).The Main Board transmits the digitized and serialized data to the Daughter Board through a 400 pin FPGA Mezzanine Connector (FMC). It is divided in two halves to achieve redundancy.

Figure 3: Picture of the Main Board.

2.3. Daughter Board

The Daughter Board provides high speed communication between front-end and back-end electronics (Figure 4) [4]. It is designed to preserve a 2-fold redundancy. Similar to the Main Board, it is separated in two halves that operate independently. Each side of the Daughter Board hosts a Kintex7 FPGA that receives the digitized data from the Main Board ADCs and transmits it to the back-end electronics outside the cavern using a QSFP+ optical link (4 lanes at 10.24 Gbps). QSFP+ transceivers based on modulators (Mach-Zehnder interferometers) have shown the best results operating above 40 Gbps (4 x 10 Gbps lanes) with Bit Error Rate (BER) less than 10^{-18} (1 error in 1000 days). No Single Event Upset (SEU) has been observed after a proton irradiation with a fluence of 8 x 10^{11} p/cm^2.
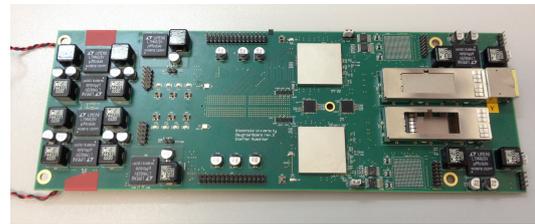

Figure 4: Picture of the Daughter Board.

2.4. sRead-Out Driver (sROD)

The sROD will be the main element of the back-end electronics [5]. It receives and process the digital detector digital data and provides information to the L0/L1 trigger systems. It distributes the Trigger Timing and Control (TTC) signals, the Detector Control System (DCS) commands and monitoring values, and it is the interface with the Data AcQuisition (DAQ) system.

The sROD Demonstrator (Figure 5) is able to read-out one new hybrid module (4 mini-drawers) using 4 QSFP connectors. One Avago MiniPOD TX module is used for communication with the L0/L1 trigger and one RX module is present for evaluation purposes. A Xilinx Virtex7 FPGA with 48 GTX transceivers (10 Gbps) provides the interface with the front-end electronics. A Kintex7 Xilinx FPGA with 28 GTX transceivers is used

to communicate with the L0/L1 trigger system. Both FPGAs are connected to 512 MB DDR3 modules and 1 Gb flash chips. The sROD is compliant with the double mid-size Advanced Mezzanine Card (AMC) form-factor standard (180.6 mm × 148.5 mm) so it can be plugged in an ATCA carrier or a uTCA chassis. The board, designed in the *Universidad de Valencia*, is now manufactured, mounted and is under test.

Figure 5: Picture of the sROD Demonstrator.

2.5. Portable Test-bench

TileCal modules have to be tested inside ATLAS cavern during maintenance periods. PROMETEO (a Portable ReadOut ModulE for Tilecal ElectrOnics) is a standalone test system that will provide full certification of the new front-end electronics. It is based on a Xilinx VC707 evaluation board as the processing core of the system and a QSFP FMC module, for optical interface with the mini-drawers. Custom HV and LED Driver boards are used for testing the PMTs and a custom 16 channel ADC FMC board is used for testing the present system analog trigger outputs of the hybrid version of the proposed Phase II system. The system communication software uses the IPbus protocol [6], which is based on firmware on one hand and on C++ or Python libraries on the other.

3. Read out Test

The Charge Injection feature of the 3-in-1 cards has been used to test the fast readout of the electronics. Propagation of commands from the sROD to the front-end electronics is performed using the 4.8 Gbps downlink. These commands are generated and sent from a laptop to the sROD using the IPbus protocol through an Ethernet connection. The sROD forwards the commands to the Daughter board where they are redirected to the proper FPGA on the Main board, which targets

the 3-in-1 card. The samples of a charge injection pulse is shown in Figure 6, including the characteristic leakage pulse after the pulse.
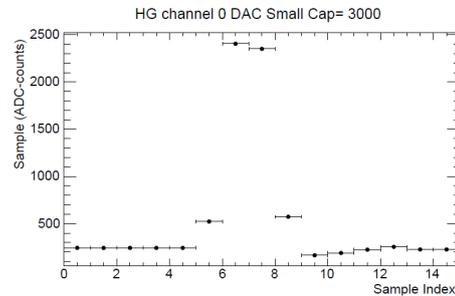

Figure 6: Digital samples of a Charge injection pulse.

The linearity test shows a good agreement between the 3-in-1 configured injected charge and the maximum sample received in the sROD (Figure 7).
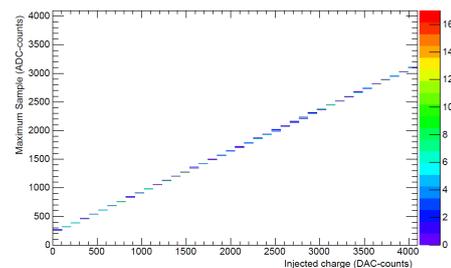

Figure 7: Maximum sample as a function of the injected charge for a single channel.

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