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Nuclear Physics B Proceedings Supplement 00 (2014) 1–7
Nuclear Physics B Proceedings Supplement

The Pixel Detector of the ATLAS Experiment for the Run 2 at the Large Hadron Collider

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Abstract

The Pixel Detector of the ATLAS experiment has shown excellent performance during the whole Run 1 of LHC. Taking advantage of the long shutdown, the detector was extracted from the experiment and brought to surface, to equip it with new service quarter panels, to repair modules and to ease installation of the Insertable B-Layer (IBL). The IBL is a fourth layer of pixel detectors, and has been installed in May 2014 between the existing Pixel Detector and a new smaller radius beam-pipe. To cope with the high radiation and pixel occupancy due to the proximity to the interaction point, a new read-out chip and two different silicon sensor technologies (planar and 3D) have been developed. Furthermore, the physics performance will be improved through the reduction of the pixel size while, targeting for a low material budget, a new mechanical support using lightweight staves and a CO_2 based cooling system have been adopted. The IBL construction and installation in the ATLAS experiment has been completed very successfully. The IBL qualification has shown outstanding detector performance with less then 0.09% of bad pixels. The final commissioning is now on-going and the ATLAS Pixel Detector is ready to join the LHC Run 2 with an improved configuration and a new pixel layer.

Keywords: ATLAS, Pixel, IBL, nSQP, LS1, Upgrade

1. Introduction

The Large Hadron Collider (LHC) has been upgraded to the design energy of 13 to 14 TeV and instantaneous luminosity of 10^{34} $cm^{-2}s^{-1}$ during the first LHC Long Shut-down (LS1, 2013-2014) . At the end of the LHC Phase I (2021), the ATLAS [1] integrated luminosity is foreseen around 300 fb^{-1}, which means an expected fluence of 50 MRad ionizing dose and 10^{15} n_{eq}/cm^2 non-ionizing dose. In these conditions, the high number of interactions per bunch crossing can cause a significant degradation of the ATLAS Detector performance and, in particular, the Pixel Detector [2] will have to cope with a significant radiation damage. A new fourth layer of pixel modules, the Insertable B-Layer (IBL) [3], has been installed and it will improve the performance compensating inefficiency, radiation damage and losses of pixels through redundancy of the 4^{th} layer. The IBL is located closer to the interaction point allowing an improvement of tracking precision and impact parameter resolution, which implies also an improvement of the b-tagging performance. In addition, several upgrades have been successfully accomplished for the three pixel layers already in use during the LHC Run 1. In 2012 with the final LHC running conditions, an integrated luminosity of 20.8 fb^{-1} and a peak luminosity of $7.7{\cdot}10^{33}cm^{-2}s^{-1}$ were achieved. These parameters produced an average pile-up of 20.7 interactions per bunch crossing (BC) with peak values of more than 40. The Pixel Detector readout system had to cope with these conditions, which are already beyond the design specifications. The necessity to increase the readout speed, to repair a few pixel modules, failed during the LHC Run 1, and to move the optical transceivers (Optoboards) to an easier accessible location by replacing the Pixel Ser-

vice Quarter Panels (SQP), lead to the important decision of extracting the Pixel Detector from the ATLAS Experiment during the LS1.

2. ATLAS Pixel Detector before the first LHC Long Shut-down

Before the Long Shut-Down Upgrades, the ATLAS Pixel Detector was made of 1744 modules, which are located in three barrel layers and three end-cap disks on each side for a total of about 80 millions readout channels. It provided three high-resolution measurement points in the pseudo-rapidity region $|\eta| < 2.5$, reaching a resolution of 10 μm in Rϕ and 110 μm in z[1].

An ATLAS Pixel Module has a 250 μm thick n-in-n silicon sensor divided in 47232 pixels with a typical size of 50x400 μm^2. Each of these pixels is bump bonded to one readout cell of a front-end chip (FE-I3). A pixel module has 16 FE-I3 (2880 pixels each) which are combined in one timing, trigger, control and readout by the Module Control Chip (MCC). The data transfer readout is 160 Mbit/s for the innermost layer (B-Layer), 80 Mbit/s both for the Layer 1 and disks and 40 Mbit/s for the Layer 2, due to a different off-detector set-up.

During the LHC Run 1 the number of disabled and problematic modules increased from 1.5% to 5%. Figure 1 [4] shows the number of disabled modules classified by the failure type: half of the modules were disabled because of readout issues (Optoboard, Unable to tune, Clock missing). Several studies demonstrated that readout limitations will degrade the Pixel Detector performance before radiation damage does. A data extrapolation led to the possibility of having about 9.6% of disabled modules at the end of 2019.

Despite the disabled modules, the ATLAS Pixel Detector showed excellent performance over the LHC Run 1: during 2012 the data taking efficiency was 99.9% [2]. The radiation effects observed during the operation are within expectations, the most visible being the change of the leakage current and the depletion voltage. This last parameter was carefully monitored during the operation and already both B-Layer and Layer 1 have a type inversion of the silicon sensor while Layer 2 will type invert shortly after the LS1.

[1] ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the interaction point to the centre of the LHC ring, and the y-axis points upwards. Cylindrical coordinates (r,ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the beam pipe. The pseudorapidity η is defined in terms of the polar angle θ as $\eta = -\ln\tan(\theta/2)$.

[2] Data delivered with stable beams for 21.3 fb^{-1} of pp-collisions and considered as good for physics by the data quality.

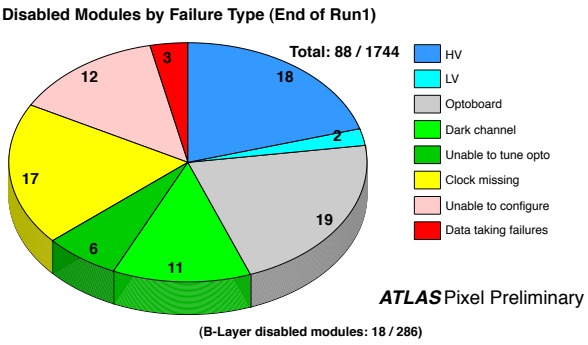

Figure 1: Number of disabled modules of the Pixel Detector at the end of Run1 classified by the type of failure [4].

3. ATLAS Pixel Detector Upgrades

The Pixel Detector was extracted from the ATLAS Experiment in April 2013 for an intensive upgrade and a consolidation campaign. The major upgrade is the installation of the new innermost layer IBL, which is described in Section 4. The extraction of the Pixel Detector permitted two other important upgrades: the installation of new Service Quarter Panels (nSQPs) and the extended campaign to classify and repair non-working pixel modules. In parallel, thanks to the Pixel Detector easy access, it was possible to install a new Diamond Beam Monitoring and an additional hardware to double the readout speed of the Pixel Detector Layers 1 and 2.

The nSQP project was conceived with the aim of bringing the Optoboards to an accessible location outside the Inner Detector since from 2011 several failures in the VCSELs[3] of the off-detector optical transmitters caused problems. Furthermore, the Pixel Detector extraction has made possible to increase the Layer 1 readout speed to 160 Mbit/s by providing two fibres per module on the outlink. With the Pixel Detector on surface, the old service quarter panels were dismounted and an investigation of the modules failures was performed at several levels (Figure 1). The eight nSQPs were successfully installed and failing pixel modules were repaired when possible.

The recovery of modules is outstanding: about 75% of disabled modules were recovered on the surface. The Pixel Detector was re-installed into the ATLAS Experiment in December 2013 and all services were reconnected in May 2014. After reconnection, few new mod-

[3] Vertical Cavity Surface Emitting Laser, which converts the data into an optical signal.

ules found faulty due to opening of HV or LV lines as well as the impossibility of data readout, as it is summarized in Figure 2. At the beginning of the LHC Run 2, the total disabled modules of the 1744 Pixel modules will be 33, about 1.9%.

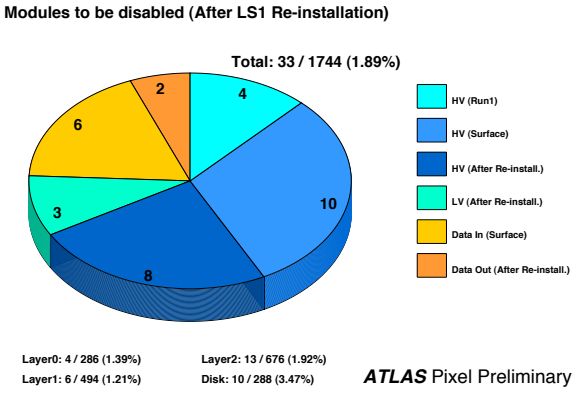

Figure 2: Number of modules of the Pixel Detector to be disabled after re-installation in the ATLAS Experiment classified by the failure mode (HV/ LV/ Data In/ Data Out) and the phase of causing problems (Run1/ Surface / After re-installation). Modules having issues but being operable are not included [4].

4. IBL: the new fourth layer of the ATLAS Pixel Detector

The Insertable B-Layer is the fourth layer added to the Pixel Detector between the new beam pipe (radius of 2.35 cm) and the current innermost Pixel layer (B-layer). Thanks to IBL, the Pixel Detector became closer to the interaction point, moving from 5.05 cm to 3.27 cm.

IBL improves the overall performance of the Pixel and ATLAS Detector by enhancing the quality of the impact parameter reconstruction for tracks and thereby improving the vertexing and b-tagging performance. Furthermore, even in case of a complete B-layer failure, IBL can restore the full b-tagging efficiency. The addition of the fourth layer will also help in mitigating luminosity effects as the increase of event pile-up, which leads to high occupancy and readout inefficiency, and the large radiation doses accumulation.

The IBL Detector can fulfill all requirements and motivations thanks to its layout and new sensor and readout technologies implemented.

4.1. IBL layout and technology

The IBL Detector consists of a cylindrical layer formed by 14 staves arranged around the new ATLAS beam-pipe and tilted by 14° to ensure the complete coverage in ϕ and to compensate for the Lorentz angle in the 2 T solenoidal magnetic field of the ATLAS Detector (Figure 3). An IBL stave is 64 cm long, made of carbon foam and it integrates a titanium pipe for CO_2 cooling. Each stave holds 20 IBL modules, each one consisting of a silicon sensor bump bonded to one or two readout chips [5]. Two different sensor technologies are used in

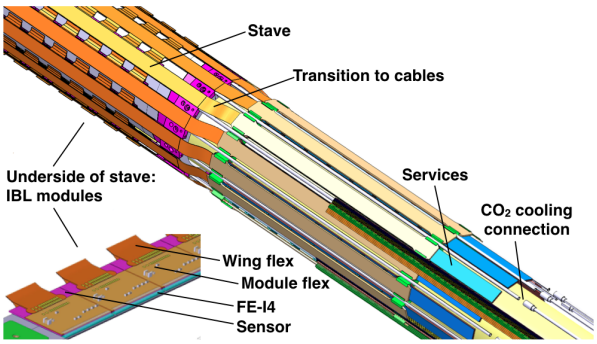

Figure 3: A longitudinal view of IBL mounted on the beam-pipe with connections to services and a sketch of an IBL stave with IBL modules loaded.

each stave: 12 Double Chip planar sensors cover the region $|\eta| < 2$ and 4 Single Chip 3D sensors are located at both ends of the stave for a total of 32 FE-I4 chips [6]. A flexible Printed Circuit Board (PCB), called module flex, is glued on each sensor and wire bonds connect it to the FE-I4, allowing the data and services transmission.

The IBL Detector is the first large scale application of the 3D sensor technology. IBL 3D sensors are 230 μm thick produced with the Double-side Double Type Columns process with n^+ columns from the front side and p^+ columns from the back side. The sensors have been developed in cooperation with two different companies, CNM[4] and FBK[5]. In CNM sensors, columns do not traverse the substrate but stop at a short distance from the surface of the opposite side, whereas FBK sensors have traversing columns.

The IBL planar sensor is an electron-collecting n^+-in-n silicon sensor design fabricated by CiS[6]. It has a lower thickness (200 μm) than the other ATLAS Pixel sensors and the inactive edge has been minimized to 200 μm by shifting 13 guard rings into the active pixel region under elongated 500 μm wide edge pixels. As for 3D sensors, each pixel size is 250x50 μm^2.

[4]Centro National de Microelectronica, Barcelona, Spain
[5]Fondazione Bruno Kessler, Trento, Italy.
[6]CiS Forschungsinstitut fur Mikrosensorik und Photovoltaik GmbH, Germany.

A new Front-End read-out chip (FE-I4) has been developed for IBL. It has 26880 pixel cells with a pixel size of 250x50 μm^2 distributed over 80 columns and 336 rows which are connected to the sensors by bump bonding each individual cell. The FE-I4 uses a 130 nm feature size bulk CMOS process and it is well matched to the IBL requirements, as for example a radiation hardness up to 250 MRad. A major innovation of the FE-I4 integrated circuit is the local memory-based architecture: the data storage is made locally at the pixel level until triggering and subsequent propagation of the trigger inside the pixel array. The pixel matrix is organized in four pixel digital readout units providing local hit processing and distributed trigger latency buffering.

4.2. IBL construction phases

The IBL detector components were built, assembled and tested in several institutes. Two parallel starting workflows can be considered: production, construction and testing of IBL modules, production and quality control of mechanical parts (mainly carbon staves and flexes). Once all components have been qualified, they are shipped to an assembly point where the qualified IBL modules are loaded into bare staves and wing flexes are connected to IBL modules.

One of the key steps in the IBL construction is the Quality Control (QC) of IBL modules. The first step in the module production chain is the flip-chip bump-bonding of a silicon sensor to one (3D sensor) or two (planar sensor) FE-I4 chips in a dedicated company. This so-called bare module becomes an IBL module by gluing a flexible PCB (module flex) on each sensor and wire bonds are made between module flex and FE-I4. Each of these IBL modules has to pass through several tests during the different stages of the assembly procedure. A final qualification test is performed after 10 thermal cycles (between -40°C and +40°C): the performance of each module is checked through current versus voltage (IV) curves, electrical tests and ^{241}Am source scan. A ranking procedure and module selection has been established referring on the sensor and FE-I4 performance. The IBL requirement is less than 1% of pixel defects per front-end. Figure 4 shows the yield of IBL module production for sensor types. A high failure rate of IBL modules is present in the first batches due to huge areas or single bump defects distributed over the module. The problem was addressed adopting an alternative bump-bonding technique with the flux-free flip chip. Beyond the bump-bonding issue, about 15% of the modules presented problems on the FE-I4 chips, which were unable to be checked before the assembly. The average bad module fraction for planar sensor is 25% while it is about 40% for 3D sensors.

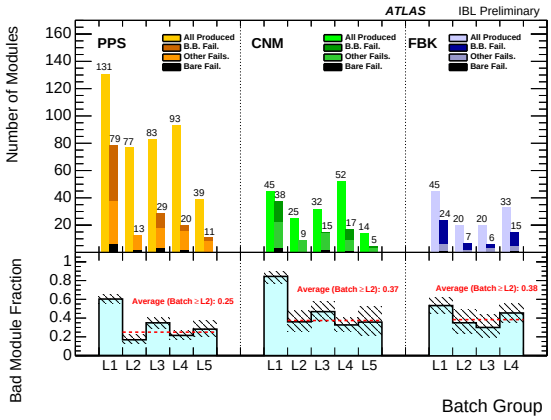

Figure 4: Yield of IBL module production for sensor types of Planar (PPS) and 3D (CNM, FBK) per production batch group. In the top panel for failure modules, B.B. Fail. stands for the large bump-bonding failure, Bare Fail. stands for the module not assembled due to mainly mechanical damages, and Other Fails. stands for both electrical and sensor failures discovered after the assembly [4].

After the qualification, the IBL modules are loaded into the bare stave through a very delicate procedure split into several steps. The most critical steps are the IBL module loading, which is performed by gluing with a thermal grease the module on the stave, and the wire bonding between the stave flex and the module flex. After the assembly, a first stave quality check is performed at the production site with the optical inspection, IV curves, electrical tests and global stave response. A total of 20 staves have been produced, meaning 400 modules loaded.

4.3. IBL stave quality assurance

A dedicated test-stand was prepared at CERN for the IBL Quality Assurance (QA) to define the IBL staves acceptance before the final integration [7]. The set-up has the capability to operate two IBL staves simultaneously at warm (22°C) and cold (-12°C) temperatures in an environmentally controlled box equipped with the N_2 flushing and CO_2 cooling system[7]. The IBL staves pass through a well-defined and detailed QA procedure, which includes an optical inspection, electrical functionality and reception tests, calibration in different environmental conditions, data taking with radioactive

[7]The cooling system, named TRACI (Transportable Refrigeration Apparatus for CO_2 Investigation) uses CO_2 as a main refrigerant, which will also be used for the final IBL cooling system.

sources as well as a classification of pixel failures. The detector calibration and tuning ensure the operability of IBL modules and they are the only tests performed at 22°C and -12°C (ATLAS Pixel Detector operating temperature) in order to test the calibration capabilities of the IBL chips in the operation environment. The threshold tuning is performed using the efficiency method, where the threshold is defined to be the charge for which the hit efficiency is 50%. The discriminator threshold for each pixel is controlled via two global 8 bit digital to analog convertors (DACs) at the chip level that allow shifting of the threshold for all pixels at the same time and a 5 bit DAC at the pixel level for fine tuning per pixel. The second parameter to be tuned is the Time Over Threshold (ToT), which is the time in which signal is above threshold and it is proportional to the deposited charge. ToT is measured in units of bunch crossings, i.e. 25 ns. Similar to the discriminator threshold, the preamplifier feedback current is controlled via an 8 bit global DAC for all pixels in a chip and a 4 bit DAC per pixel. The module tuneability is tested for reference thresholds of 3000 e^- at 22°C and 1500 e^- at -12°C. The ToT is tuned to 10 BC for a reference mip charge of 16000 e^-. The key parameter in the tuning is the threshold over noise, which determines the quality of the IBL modules with respect to their operability at a given discriminator setting. The bigger this factor is the less contamination of noise hits in the sample of physics hits will be recorded during collisions. Figure 5 shows the threshold over noise distributions of pixels for 1500 e^- tunings: a threshold over noise value higher than 5 would ensure that the noise contamination in physics hits from IBL would be less than 0.1%. The fraction of noisy IBL pixels is less than 0.03% for the 1500 e^- tuning, a factor two less than that for the current Pixel Detector. As it is visible in Figure 5, the threshold over noise mean value is different between planar and 3D sensors. This behaviour can also be seen in Figure 6 where threshold noise distributions averaged over all 18 production staves are plotted as a function of the chip number. Noise on the outer 3D modules is generally higher than that on the planar modules. A slightly higher noise is observed on the A-side of the setup. This is due to a combination of the increased noise on the HV lines of this side to which both 3D sensors are sensitive and the fact that FBK modules, which show a higher mean noise than CNM modules, were more frequently chosen for loading on this side.

A second important step in the IBL stave QA is the detector response to radiation by means of radioactive source scans, which are used to identify disconnected bumps and to check the charge calibration of each chip.

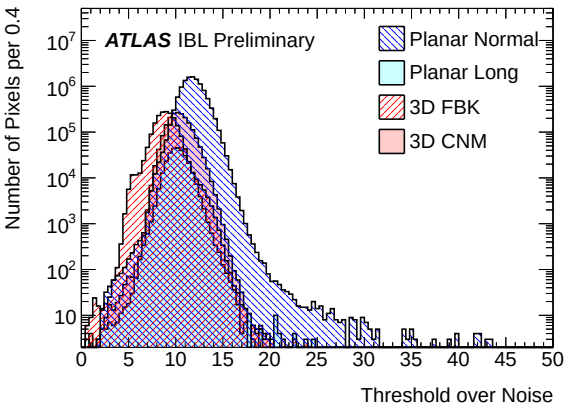

Figure 5: Threshold over noise distribution of pixels for 1500 e^- threshold tunings at -12°C module temperatures for 18 staves. The bump around a threshold to noise value of 5 is caused by a noise on HV lines of the setup and the sensitivity of FBK modules to such noise. The fraction of noisy IBL pixels is less than 0.03% [7].

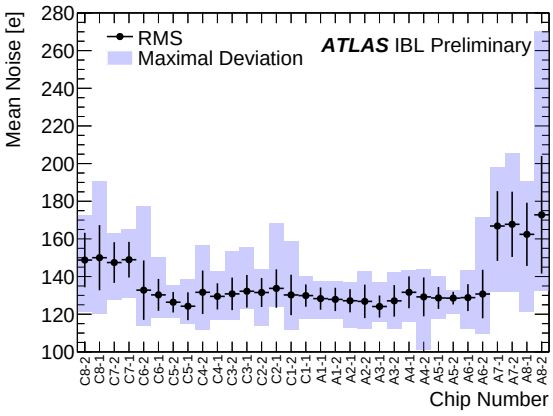

Figure 6: Average threshold noise distribution among the 18 production staves after tuning all pixels to a target threshold of 1500 e^- and to a 10 ToT target response for 16000 e^- at -12°C module temperature. The error bars show the RMS spread, while the solid boxes show the minimum and maximum values [7].

Source scans are performed at 22°C with a 3000 e^- threshold and 10 BCs ToT at 16000 e^- tuning in self-trigger mode[8] using ^{90}Sr source, which electrons deposit a charge of 16000 e^- in the sensor simulating a mip particle. Figure 7 shows the average cluster ToT value obtained from a Landau-Gauss fit of the clustered ToT distribution for each chip: there is no dependance on the position on the stave or sensor type and the mean most probable ToT value is 10.5±0.3 BC, which is con-

[8] In the selftrigger mode the HitBus signal of the FE-I4 acts as an input to the command decoder for automatic triggering.

sistent with the given tuning of 10 ToT BC for 16000 e$^-$ charge.

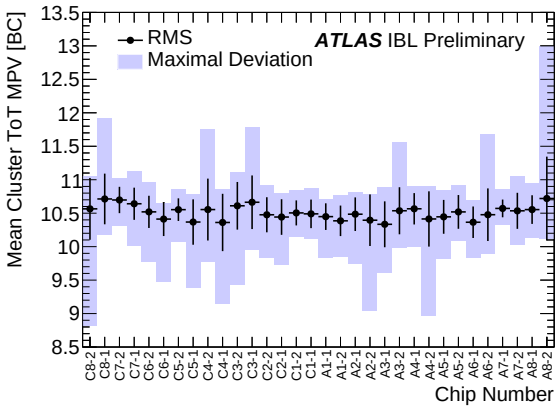

Figure 7: The average most probable cluster ToT value obtained from a Landau-Gauss fit as a function of the chip number for source scans performed at 22°C with a 3000 e$^-$ threshold and 10 BCs ToT at 16000 e$^-$ tuning [7].

A combined analysis of calibration and source scan results allows the classification of each failing pixel into several categories related to defects pertaining to front-end, sensor or bump bonding. The IBL target was required to have less than 0.37% pixel defect for each chip. The IBL QA shows that 73% of all chips loaded onto staves have less then 0.1% bad pixels of which a half is due to disconnected bumps while the other 50% are distributed between a pixel being analog dead or its tuning being impossible.

Once the staves have passed the QA, the 14 best staves to arrange around the new ATLAS beam-pipe have to be selected. The main concern for the stave selection is the coverage efficiency of the geometrical acceptance. The choice of the best staves and their location around the beam-pipe is done following several criteria: number of bad pixels per stave, uniform $\eta - \phi$ distribution of bad pixels for $|\eta| < 2.5$ and engineering constraints as, for example, the stave planarity. Figure 8 shows the bad pixel fraction in the $\eta - \phi$ region for the selected 14 staves. The total bad pixel ratio of the integrated IBL staves is 0.07% for $|\eta| < 2.5$ and 0.09% when considering the full eta range. The corresponding numbers for the four not installed staves are 0.16% and 0.18%, respectively.

4.4. IBL Integration and installation in the ATLAS Experiment

The integration of the 14 best IBL staves around the beam-pipe is a delicate engineering task composed of several steps. As a preparatory action, the titanium cooling pipe is extended to 7 m long by brazing. This stave length has to cope with an integration clearance of less than 1 mm between each stave. Furthermore, all staves and services are packed inside a 12 mm envelope along the 7 m long structure. The staves are mounted on the Inner Positioning Tube around the beam-pipe using a multi-purpose loading device and then all the service cables are connected. After the integration of each stave, a connectivity test is performed to assure that the IBL modules and service cables are working correctly. On May 2014 the IBL detector was inserted into the ATLAS experiment by means of an electrical motor with an insertion speed of about 5-10 cm/min and the IBL volume was completely sealed and flushed with N_2. The cooling pipes have been connected to the cooling services which is the first CO_2 based cooling system for the ATLAS experiment. It is a two Phase Accumulator Controlled Loop using evaporation CO_2 with a cooling capacity of 3 kW able to reach a minimum temperature of -40°C. The initial commissioning of the IBL started at the beginning of July with all IBL modules working properly: a comparison with data obtained during the QA shows that the IBL detector has not experienced damages during the installation and it can be operated very stably at the room temperature as well as at -12°C.

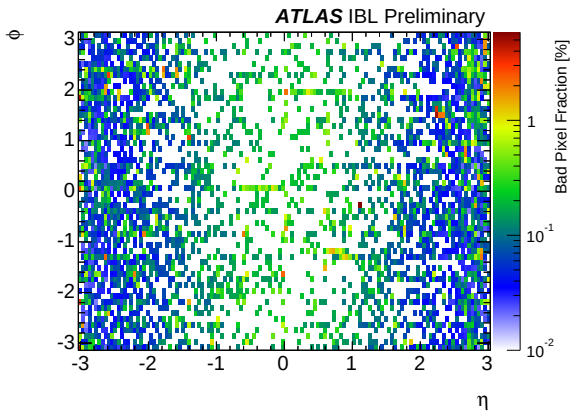

Figure 8: The bad pixel fraction in the $\eta - \phi$ plane for the 14 IBL staves. It represents the inefficiency map of the IBL as it is installed [7].

5. Conclusion: the ATLAS Pixel Detector towards LHC Run 2

The ATLAS Pixel Detector has completed two major achievements during the first LHC long shutdown: improvement of the existing Pixel Detector and installation

of the IBL.

The Pixel Detector has been upgraded very successfully with the installation of nSQP services and with the repair of several failing modules obtaining 98% of fully working modules.

The IBL Detector has been successfully installed and it can be considered as the fourth layer of the Pixel Detector. Many interesting challenges were solved during its production an construction driven by the implementation of new technologies, strong constraints and project specifications. IBL is the first large scale application of 3D silicon sensors and it exploits the new FE-I4 front end chip, which has been developed for the IBL project and for LHC Phase 2 Upgrades. Given the smaller radius of IBL, a requirement for more radiation hard technology for sensors and electronics as well as a low material budget were two key points in the IBL design and construction. The QA and commissioning have shown that the IBL Detector works very well with 100% of FE-I4 chips operable and 99.9% of functional channels in the modules.

The ATLAS Pixel Detector will join the LHC Run 2 with a new layer and an improved configuration ensuring the best possible tracking performance for the ATLAS Experiment.

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