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Vertex detector R&D for CLIC

A future CLIC vertex detector must satisfy the precision physics needs and be compatible with the challenging beam structure at CLIC. As a result the pixel detector is required to have excellent spatial resolution, precise time-tagging, full geometrical coverage, extremely low mass, low occupancy and sufficient heat removal from sensors and readout. A vertex detector concept based on two hybrid pixel-detector options (with silicon sensors or with a HV-CMOS sensor pre-stage) forms the basis of an active integrated R&D effort that pushes technology to its limits. It comprises fast, low-power and small-pitch readout ASICs implemented in 65 nm CMOS technology (CLICpix) coupled to ultra-thin sensors via low-mass interconnects. The power dissipation of the readout chips is reduced by means of power pulsing, allowing for a cooling system based on forced gas flow. In this presentation the CLIC vertex-detector requirements are reviewed and the current status of R&D on sensors, readout and detector integration, including results of recent beam tests are presented.

Summary

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