CMS TRIGGER IMPROVEMENTS TOWARDS RUN II

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Two levels:

- **Level-1**: custom electronics to reduce event rate from 20-40 MHz to no more than 100 kHz for the detector readout electronics, with 4 μs latency.

- **High Level Trigger (HLT)**: event filter farm comprised of commercial CPUs running software to further reduce event rate to storage to an average of ~1 kHz for Run 2.
Run 2 Trigger Improvements

- Trigger rates for Run 2 of the LHC are driven by the increase in luminosity, the center-of-mass energy, and by higher pile-up
  - Lumi and $\sqrt{s}$ lead to a factor ~4 increase
- Nevertheless the physics program compels us to maintain sensitivity for electroweak scale physics and for TeV scale searches similar to that of LHC Run 1
- Mitigate L1 Trigger rates with an upgrade to improve:
  - $e/\gamma$ and $\tau$ cluster footprints and isolation
  - muon $p_T$ resolution and muon isolation
  - jets with PU subtraction
  - L1 menu sophistication (#lines, complexity)
- Improve HLT rates and CPU time by improving
  - Tracking performance
  - Object reconstruction
  - Isolation
L1 Trigger Upgrade

- Detailed design and motivation documented in a Technical Design Report
  - https://cds.cern.ch/record/1556311

- Essentially a complete replacement of the existing system
  - Increase system flexibility with high bandwidth optical links and large FPGAs
  - Further standardization across systems using µTCA telecomm platform
  - Build and commission upgrade in parallel with current trigger

- Target deployment in 2016
  - Preparations already during current LHC LS1 (i.e. signal splitting)
  - Limited deployment of calo trigger improvements in 2015
Two-layer calorimeter trigger with calorimeter tower-level precision and pile-up subtraction

Integrated muon trigger combining all 3 muon systems in track-finding with a more sophisticated $p_T$ measurement
Calorimeter L1 Trigger Transition

- Upgrade commissioning designed to take place in parallel
  - Duplicate ECAL signals with active optical components
  - Split HCAL optical inputs to HCAL back-end electronics
  - Both during the current Long Shutdown 1 (LS1)
Calorimeter L1 Trigger Transition

- Replacement of copper cable connections with optical connections from ECAL trigger primitive boards to both existing and upgraded calorimeter trigger systems
  - Production is done
  - Installation of fibers and mezzanine cards is complete
  - Commissioning is underway
L1 Calo Trigger Upgrade Architecture: “Time Multiplexing”

Full range of $\phi$, All 72 towers (each card spans $\frac{1}{2} \eta$ and 4 towers $\phi$)

36 cards, each receiving 30 links at 4.8 - 6.4Gb/s from Calorimeter TPGs

36 Layer-1 Cards

Each L1 card transmits 24 links @ 10G

72 input links per L2 card

2 output links per L2 card @ 10Gb/s

Event serving to Layer-2 processors for jet-finding, etc. like High Level Trigger
Calo Trigger Upgrade Hardware Status

✦ **Calo Layer 1 ("CTP7" card)**
  - Receive data from calorimeters, precluster and format for global processing
  - 2 prototypes built and tested
  - Excellent results with processor system, power supplies, clock system and optical/backplane links (Tested 4.8 - 10 Gbps)
  - Tested successfully with ECAL and HCAL inputs
  - Production to start in October

✦ **Calo layer 2 ("MP7" card)**
  - Global processing layer (jets, E sums, isolation,...)
  - 72 Rx and 72 Tx @ 10 Gbps fully tested
  - Delivery and testing of initial production cards has started

✦ **Optical patch panels**
  - Specifications complete and orders out
Partial Calo Trigger Upgrade in 2015

- The copper outputs of the legacy Regional Calorimeter Trigger are converted to 10 Gbps optical signals which can drive a couple new Layer-2 MP7 processors.

- Algorithms running on two MP7 Cards provide better electron isolation, better tau trigger, and jet PU subtraction early in 2015.

  - New optical interfaces successfully tested.
  - Production launched.
  - Firmware development is in progress.

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Branches:
- MP7 (new)
- Algorithm Card(s) (1-3)
- Imperial HW + Core FW/SW
- USCMS Algorithm FW/SW

Global Trigger (existing)
GT Inputs remain unchanged

CTP7 (new)
Single Readout Card
In Situ RCT Test / Monitor
USCMS HW/FW/SW

DAQ-AMC 13 (new)
CMS Muon System and Trigger

**Barrel:**
Drift-Tubes (DT) and Resistive Plate Chambers (RPC)

**Endcap:**
Cathode Strip Chambers (CSC) and RPC

**Overlap:**
DT, RPC, CSC

All self-triggering
Muon Detector Improvements during LS1

- Add fourth layer of CSC and RPC coverage in endcaps for robustness and higher efficiency, along with new outermost shielding wall
- Improve the triggering and readout for $2.1 < |\eta| < 2.4$ for the first CSC layer in endcaps (new front-end and trigger electronics)

See also L.Guiducci’s talk, Friday 15:00
Muon Trigger Upgrade Transition

- Install parallel and higher bandwidth optical paths
  - Full split of endcap CSC signals with modified Muon Port Cards installed in cavern during LS1 (and sends all CSC segments)
  - DT trigger electronics moved from cavern to counting room
  - Split RPC signals and a slice of the DT to commission the new trigger

- Build up new Muon Track Finders in 2015 and commission in parallel

- Ready for physics by 2016
Muon Track Finder Upgrade

- Improve upon successful features of current muon trigger
  - Enlarge LUT memory for $p_T$ assignment from MBs to GBs, allowing use of more angles in “fit”
  - Larger FPGA to handle more hits from pile-up, additional chambers

- Use the redundancy of the three muon detection systems earlier in trigger chain
  - Create a higher resolution and more robust muon trigger rather than combine lower resolution ones

- Add calorimeter isolation

- Report more muons and increase precision
  - Improved isolation, b-tagging, invariant mass, etc. at the Global Trigger
Muon Trigger Upgrade Status

🌟 Muon trigger link concentration and fan-out
  - First assembled prototypes just received for DT/RPC barrel optical links
  - CSC MPC mezzanines ready for installation and commissioning

🌟 “MTF7” Processor Status
  - Intended for muon endcap and barrel/endcap overlap
  - Dual-card design with 1 GB memory
  - Extensively tested at 3.2 Gbps and 10 Gbps asynch.
  - 3 prototypes built, one at CERN ready for integration tests
  - Production to start in October
Global Muon Trigger & Global Trigger

🌟 Hardware platform is the MP7 (Calo) processor for both

🌟 μGMT algorithm logic has been developed:

➢ New: Sorting all 108 muons from Track-Finders to final 8 muons, absorbing a separate muon sorting layer to save latency

➢ New: Calorimeter-based isolation (incl. extrapolation + pile-up subtraction)

➢ Baseline firmware implemented, algorithm development on track

🌟 μGT

➢ New: remove limitation on # triggers (>128), and offer more complex relations between objects (e.g. invariant mass)

➢ Object interfaces and data formats defined

➢ First version of μGT menu is available

➢ Firmware development and testing underway
Performance: Trigger Thresholds

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CERN-LHCC-2013-011

Single e/µ:
- e: 50 GeV → 30 GeV
- µ: 40 GeV → 20 GeV

Multijet:
- Single iso e/µ + Jet
- Single Mu + Jet
- Single iso e/µ + H_{Tmiss}
- Single Mu + H_{Tmiss}
- $H_T \times 1/10$

CMS Simulation $\sqrt{s} = 14$ TeV, $L = 2.2 \times 10^{34}$ cm$^{-2}$s$^{-1}$, 25 ns
**L1 Upgrade Tau Trigger Performance**

- Hadronic tau trigger with tower level granularity
  - Efficiency significantly improved over Run 1

\[ \mu + \tau \text{ trigger:} \]
30% rate reduction and higher efficiency

![Graph showing efficiency vs. transverse energy (E_T) for L1 tau trigger.](image)

- CMS Preliminary 2014 pp, \( \sqrt{s} = 8 \) TeV
- L1 \( \tau \) trigger: \( \tau^{\pm}/\tau^{0} \) pair from Z
- L1 Taus:
  - ● Barrel Run 1
  - ○ Barrel Upgrade

- Background Reduction vs. 50% Efficiency \( p_T \) Threshold [GeV]

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HIGH LEVEL TRIGGER
Tracking Improvements

- HLT uses regional tracking of strip and pixel hits in an iterative approach for different track categories.
- In order to mitigate effects from pile-up, the CPU processing time has been reduced:
  - Optimization of code
  - Primary vertex constraint in all iterations
  - Optimization of region $p_T$ cuts
  - Removal of last two tracking iterations (of 5) except for displaced track triggers
- Overall a factor ~4 reduction in CPU time.
Vertexing Improvements

- Improvements have been made to the fast pixel primary vertex finding algorithm, which works from pixel clusters before the iterative track reconstruction is performed.

- The HLT b-tagging discriminant for jets has improved with the improvements to the iterative tracking.

15% reduction in CPU time, \( tt \) sample.
Electron Clustering and Isolation

- New electron superclustering algorithm from Particle Flow objects built from tracks, ECAL and HCAL clusters

- New isolation built from Particle Flow objects, including pile-up subtraction
  - Similar performance as with offline isolation

30% better background rejection

Improved pile-up dependence of efficiency
Muon Tracking and Isolation

- Improvements to the muon track reconstruction algorithm to improve the pile-up dependence of the efficiency plus additional quality cuts
  - Rate increment is only 4.3% for isolated muons with $P_T \geq 24$ GeV
- Impact of a very loose track-based isolation cut applied to both legs of double muon triggers has been assessed
  - 56% rate reduction for <1% inefficiency

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**Efficiency vs. Number of offline vertices**

- 2012 Configuration
- Proposed improvements for 2015 w/o quality cuts
- Proposed improvements for 2015 w/ quality cuts

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**M_{ll} [GeV] vs. Events / 5 GeV**

- 2012 (Non-Iso) Trigger, Opposite-sign Muons
- 2012 (Non-Iso) Trigger, Same-sign Muons
- 2015 (Iso) Trigger, Opposite-sign Muons
- 2015 (Iso) Trigger, Same-sign Muons
The L1 Trigger upgrade project is well underway
- A considerable part of the hardware is in production
- The rest of the hardware has been successfully prototyped and should be ready to commence production within 2014
- Performance significantly improved for Run 2

The High Level Trigger algorithms significantly improved for Run 2
- Iterative tracking CPU timing dramatically reduced without compromising performance, benefiting many triggers using tracking
- Lepton isolation is improved, with better pile-up dependence

Trigger menus for 2015 LHC operations at 13 TeV are in progress
BACK-UP
<table>
<thead>
<tr>
<th>Process (x2 improvement highlighted)</th>
<th>$1.1 \times 10^{34}$ cm$^{-2}$ s$^{-1}$</th>
<th>$2.2 \times 10^{34}$ cm$^{-2}$ s$^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Current</td>
<td>Upgrade</td>
</tr>
<tr>
<td>W($ev$), H($bb$)</td>
<td>57.7%</td>
<td>87.0%</td>
</tr>
<tr>
<td>W($\mu\nu$), H($bb$)</td>
<td>95.9%</td>
<td>100%</td>
</tr>
<tr>
<td>VBF H($\tau\tau(\mu\tau)$)</td>
<td>42.6%</td>
<td>51.3%</td>
</tr>
<tr>
<td>VBF H($\tau\tau(\tau\tau)$)</td>
<td>24.4%</td>
<td>44.3%</td>
</tr>
<tr>
<td>VBF H($\tau\tau(\tau\tau)$)</td>
<td>17.2%</td>
<td>53.7%</td>
</tr>
<tr>
<td>H(WW($ee$))</td>
<td>91.4%</td>
<td>97.8%</td>
</tr>
<tr>
<td>H(WW($\mu\mu$))</td>
<td>99.9%</td>
<td>99.9%</td>
</tr>
<tr>
<td>H(WW($e\mu$))</td>
<td>97.6%</td>
<td>99.4%</td>
</tr>
<tr>
<td>H(WW($\mu e$))</td>
<td>99.6%</td>
<td>99.5%</td>
</tr>
<tr>
<td>Stop$\rightarrow$bWc$\rightarrow$e, jets (600 – 450 GeV)</td>
<td>55.8%</td>
<td>68.2%</td>
</tr>
<tr>
<td>Stop$\rightarrow$bWc$\rightarrow$\mu, jets (600 – 450 GeV)</td>
<td>78.1%</td>
<td>81.6%</td>
</tr>
<tr>
<td>RPV Stop$\rightarrow$jets (200 GeV)</td>
<td>70.1%</td>
<td>99.9%</td>
</tr>
<tr>
<td>RPV Stop$\rightarrow$jets (300 GeV)</td>
<td>93.7%</td>
<td>99.9%</td>
</tr>
</tbody>
</table>

Average Improvement: 17% (Low Lumi) & 40% (High Lumi)
Tests of L1 Calo Trigger Upgrade

**Time-multiplexing**

- **Setup:**
  - Two layer 1 pre-processors, one layer 2 main processing node, and a de-multiplexing card

- **Objectives:**
  - Reliable transmission of data at 10 Gb/s
  - Successful alignment of all links
  - Implementation of an algorithm and successful transmission of data through it
  - Verification of latency

- **Results:**
  - All objectives successfully met
L1 Muon Track-Finder Integration tests

- Mimicking real system setup:
  - Sending data from 2 MPCs to MTF6
  - Each MPC clocked by separate CCB
  - MTF6 receives clock from AMC13
  - CCBs and AMC13 receive clock from common source

- Types of tests:
  - PRBS, and random data via test FIFOs

- Result:
  - No errors.

- Also tested successfully the PT LUT, and PCI express interface

5 July 2014

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